User's Manual

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R8C/LA6A Group, R8C/LA8A Group

User's Manual: Hardware

RENESAS MCU
R8C Family / R8C/Lx Series

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/LA6A Group and R8C/LA8A Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview	R8C/LA3A Group, R8C/LA5A Group, R8C/LA6A Group, R8C/LA8A Group Shortsheet	REJ03B0305
User's Manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/LA6A Group, R8C/LA8A Group User's Manual: Hardware	This User's Manual
User's Manual: Software	Description of CPU instruction set	R8C/Tiny Series User's Manual: Software	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from the Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	XXX4	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—	Reserved bit	Set to 0.	R/W
b4	XXX4	XXX bit	Function varies according to the operating mode.	R/W
b5	XXX5			W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2

*3

*1

R/W: Read and write.
R: Read only.
W: Write only.
–: Nothing is assigned.

*2

- Reserved bit

  Reserved bit. Set to specified value.

*3

- Nothing is assigned.

  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value.

  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.

  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input / Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver / Transmitter
VCO	Voltage Controlled Oscillator

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0005h	Processor Mode Register 1	PM1	201
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Note:
1. Blank spaces are reserved. No access is allowed.

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00A5h	UART0 Transmit/Receive Control Register 1	U0C1	357
00A6h	UART0 Receive Buffer Register	U0RB	358
00A7h			
00A8h	UART2 Transmit/Receive Mode Register	U2MR	378
00A9h	UART2 Bit Rate Register	U2BRG	378
00AAh	UART2 Transmit Buffer Register	U2TB	379
00ABh			
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	380
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	381
00AEh	UART2 Receive Buffer Register	U2RB	382
00AFh			
00B0h	UART2 Digital Filter Function Select Register	URXDF	383
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	383
00BCh	UART2 Special Mode Register 4	U2SMR4	384
00BDh	UART2 Special Mode Register 3	U2SMR3	385
00BEh	UART2 Special Mode Register 2	U2SMR2	385
00BFh	UART2 Special Mode Register	U2SMR	386

Address	Register	Symbol	Page
00C0h	A/D Register 0	AD0	494
00C1h			
00C2h	A/D Register 1	AD1	494
00C3h			
00C4h	A/D Register 2	AD2	494
00C5h			
00C6h	A/D Register 3	AD3	494
00C7h			
00C8h	A/D Register 4	AD4	494
00C9h			
00CAh	A/D Register 5	AD5	494
00CBh			
00CCh	A/D Register 6	AD6	494
00CDh			
00CEh	A/D Register 7	AD7	494
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	495
00D5h	A/D Input Select Register	ADINSEL	496
00D6h	A/D Control Register 0	ADCON0	497
00D7h	A/D Control Register 1	ADCON1	498
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh	A/D Control Register 2	ADCON2	499
00DEh			
00DFh			
00E0h	Port P0 Register	P0	72
00E1h	Port P1 Register	P1	72
00E2h	Port P0 Direction Register	PD0	71
00E3h	Port P1 Direction Register	PD1	71
00E4h	Port P2 Register	P2	72
00E5h	Port P3 Register	P3	72
00E6h	Port P2 Direction Register	PD2	71
00E7h	Port P3 Direction Register	PD3	71
00E8h	Port P4 Register	P4	72
00E9h	Port P5 Register	P5	72
00EAh	Port P4 Direction Register	PD4	71
00EBh	Port P5 Direction Register	PD5	71
00ECh	Port P6 Register	P6	72
00EDh	Port P7 Register	P7	72
00EEh	Port P6 Direction Register	PD6	71
00EFh	Port P7 Direction Register	PD7	71
00F0h	Port P8 Register	P8	72
00F1h	Port P9 Register	P9	72
00F2h	Port P8 Direction Register	PD8	71
00F3h	Port P9 Direction Register	PD9	71
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

Note:
1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
0100h			
0101h			
0102h			
0103h			
0104h			
0105h			
0106h			
0107h			
0108h	Timer RB0 Control Register	TRB0CR	214
0109h	Timer RB0 One-Shot Control Register	TRB0OCR	214
010Ah	Timer RB0 I/O Control Register	TRB0IOC	215, 218, 222, 225, 229
010Bh	Timer RB0 Mode Register	TRB0MR	215
010Ch	Timer RB0 Prescaler Register	TRB0PRE	216
010Dh	Timer RB0 Secondary Register	TRB0SC	216
010Eh	Timer RB0 Primary Register	TRB0PR	217
010Fh			
0110h	Timer RH Second Data Register / Counter Data Register	TRHSEC	288, 320
0111h	Timer RH Minute Data Register / Compare Data Register	TRHMIN	289, 320
0112h	Timer RH Hour Data Register	TRHHR	290
0113h	Timer RH Day-of-the-Week Data Register	TRHWK	291
0114h	Timer RH Date Data Register	TRHDY	292
0115h	Timer RH Month Data Register	TRHMON	293
0116h	Timer RH Year Data Register	TRHYR	294
0117h	Timer RH Control Register	TRHCR	295, 321
0118h	Timer RH Count Source Select Register	TRHCSR	298, 322
0119h	Timer RH Clock Error Correction Register	TRHADJ	299
011Ah	Timer RH Interrupt Flag Register	TRHIFR	300, 324
011Bh	Timer RH Interrupt Enable Register	TRHIER	301, 325
011Ch	Timer RH Alarm Minute Register	TRHAMN	302
011Dh	Timer RH Alarm Hour Register	TRHAHR	303
011Eh	Timer RH Alarm Day-of-the-Week Register	TRHAWK	304
011Fh	Timer RH Protect Register	TRHPRC	305, 325
0120h	Timer RC Mode Register	TRCMR	237
0121h	Timer RC Control Register 1	TRCCR1	238, 260, 269, 275
0122h	Timer RC Interrupt Enable Register	TRCIER	238
0123h	Timer RC Status Register	TRCSR	239
0124h	Timer RC I/O Control Register 0	TRCIOR0	240, 255, 261
0125h	Timer RC I/O Control Register 1	TRCIOR1	240, 256, 262
0126h	Timer RC Counter	TRC	241
0127h			
0128h	Timer RC General Register A	TRCGRA	241
0129h			
012Ah	Timer RC General Register B	TRCGRB	241
012Bh			
012Ch	Timer RC General Register C	TRCGRC	241
012Dh			
012Eh	Timer RC General Register D	TRCGRD	241
012Fh			

Address	Register	Symbol	Page
0130h	Timer RC Control Register 2	TRCCR2	242, 263, 270, 276
0131h	Timer RC Digital Filter Function Select Register	TRCDF	243, 277
0132h	Timer RC Output Master Enable Register	TRCOER	244
0133h	Timer RC Trigger Control Register	TRCADCR	244
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			

Note:
1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			
0180h	Timer RJ Pin Select Register	TRJSR	73, 336
0181h	Timer RB Pin Select Register	TRBSR	74, 217, 337
0182h	Timer RC Pin Select Register 0	TRCPSR0	75, 245
0183h	Timer RC Pin Select Register 1	TRCPSR1	76, 246
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	77, 359
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	78, 386
018Bh	UART2 Pin Select Register 1	U2SR1	79, 387
018Ch	SSU/IIC Pin Select Register	SSUIICSR	80, 425, 457
018Dh	Timer RH Second Interrupt Control Register	TRHICR	306
018Eh	INT Interrupt Input Pin Select Register	INTSR	81, 175
018Fh	I/O Function Pin Select Register	PINSR	82, 457

Note:
1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	426
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register	SSTDR/ICDRT	426, 458
0195h	SS Transmit Data Register H	SSTDRH	
0196h	SS Receive Data Register L / IIC bus Receive Data Register	SSRDR/ICDRR	427, 458
0197h	SS Receive Data Register H	SSRDRH	
0198h	SS Control Register H / IIC bus Control Register 1	SSCRH/ICCR1	427, 459
0199h	SS Control Register L / IIC bus Control Register 2	SSCRL/ICCR2	428, 460
019Ah	SS Mode Register / IIC bus Mode Register	SSMR/ICMR	429, 461
019Bh	SS Enable Register / IIC bus Interrupt Enable Register	SSER/ICIER	430, 462
019Ch	SS Status Register / IIC bus Status Register	SSSR/ICSR	431, 463
019Dh	SS Mode Register 2 / Slave Address Register	SSMR2/SAR	432, 464
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	552
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	554
01B5h	Flash Memory Control Register 1	FMR1	557
01B6h	Flash Memory Control Register 2	FMR2	558
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h	Address Match Interrupt Register 0	RMAD0	185
01C1h			
01C2h			
01C3h	Address Match Interrupt Enable Register 0	AIER0	185
01C4h	Address Match Interrupt Register 1	RMAD1	185
01C5h			
01C6h			
01C7h	Address Match Interrupt Enable Register 1	AIER1	185
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			

Address	Register	Symbol	Page
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	82
01E1h	Port P1 Pull-Up Control Register	P1PUR	82
01E2h	Port P2 Pull-Up Control Register	P2PUR	82
01E3h	Port P3 Pull-Up Control Register	P3PUR	82
01E4h	Port P4 Pull-Up Control Register	P4PUR	82
01E5h	Port P5 Pull-Up Control Register	P5PUR	82
01E6h	Port P6 Pull-Up Control Register	P6PUR	82
01E7h	Port P7 Pull-Up Control Register	P7PUR	82
01E8h	Port P8 Pull-Up Control Register	P8PUR	82
01E9h	Port P9 Pull-Up Control Register	P9PUR	82
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P7 Drive Capacity Control Register	P7DRR	83
01F1h	Port P8 Drive Capacity Control Register	P8DRR	83
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	84
01F6h	Input Threshold Control Register 1	VLT1	85
01F7h	Input Threshold Control Register 2	VLT2	86
01F8h	Comparator B Control Register 0	INTCMP	520
01F9h			
01FAh	External Input Enable Register 0	INTEN	176, 520
01FBh	External Input Enable Register 1	INTEN1	177
01FCh	INT Input Filter Select Register 0	INTF	177, 521
01FDh	INT Input Filter Select Register 1	INTF1	178
01FEh	Key Input Enable Register 0	KIEN	182
01FFh	Key Input Enable Register 1	KIEN1	183

Note:

1. Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Page
0200h	LCD Control Register	LCR0	529
0201h			
0202h	LCD Option Clock Control Register	LCR2	529
0203h	LCD Clock Control Register	LCR3	530
0204h	LCD Display Control Register	LCR4	530
0205h			
0206h	LCD Port Select Register 0	LSE0	531
0207h	LCD Port Select Register 1	LSE1	531
0208h	LCD Port Select Register 2	LSE2	532
0209h	LCD Port Select Register 3	LSE3	532
020Ah	LCD Port Select Register 4	LSE4	533
020Bh	LCD Port Select Register 5	LSE5	533
020Ch			
020Dh			
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	534
0211h		LRA1L	534
0212h		LRA2L	534
0213h		LRA3L	534
0214h		LRA4L	534
0215h		LRA5L	534
0216h		LRA6L	534
0217h		LRA7L	534
0218h		LRA8L	534
0219h		LRA9L	534
021Ah		LRA10L	534
021Bh		LRA11L	534
021Ch		LRA12L	534
021Dh		LRA13L	534
021Eh		LRA14L	534
021Fh		LRA15L	534
0220h		LRA16L	534
0221h		LRA17L	534
0222h		LRA18L	534
0223h		LRA19L	534
0224h		LRA20L	534
0225h		LRA21L	534
0226h		LRA22L	534
0227h		LRA23L	534
0228h		LRA24L	534
0229h		LRA25L	534
022Ah		LRA26L	534
022Bh		LRA27L	534
022Ch		LRA28L	534
022Dh		LRA29L	534
022Eh		LRA30L	534
022Fh		LRA31L	534
0230h		LRA32L	534
0231h		LRA33L	534
0232h		LRA34L	534
0233h		LRA35L	534
0234h		LRA36L	534
0235h		LRA37L	534
0236h		LRA38L	534
0237h		LRA39L	534
:			
FFDBh	Option Function Select Register 2	OFS2	37, 197, 204
:			
FFFFh	Option Function Select Register	OFS	36, 55, 196, 203, 550

1. Overview

1.1 Features

The R8C/LA6A Group and R8C/LA8A Group of single-chip MCUs incorporate the R8C CPU core, which implements a powerful instruction set for a high level of efficiency and supports a 1 Mbyte address space, allowing execution of instructions at high speed. In addition, the CPU core integrates a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions, including multifunction timer and serial interface, helps reduce the number of system components.
The R8C/LA6A Group and R8C/LA8A Group have data flash (1 KB × 2 blocks).

1.1.1 Applications

Household appliances, office equipment, audio equipment, consumer products, etc.

1.1.2 Differences between Groups

Table 1.1 lists the differences between the groups, Table 1.2 lists the I/O ports provided for each group, and Table 1.3 lists the LCD Display Function Pins Provided for Each Group. Figures 1.3 and 1.4 show the pin assignment for each group, and Tables 1.7 and 1.8 list product information.
The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/LA6A Group	R8C/LA8A Group
I/O Ports	Programmable I/O ports	56 pins	72 pins
	High current drive ports	8 pins	10 pins
Timers	Timer RJ0 pins	1 pin (I/O: 1, output: none)	2 pins (I/O: 1, output: 1)
	Timer RJ1 pins	1 pin (I/O: 1, output: none)	2 pins (I/O: 1, output: 1)
	Timer RJ2 pins	None	2 pins (I/O: 1, output: 1)
Serial interface	UART2	None	1 pin
A/D Converter	Analog input pins	8 pins	12 pins
LCD Drive Control Circuit	Segment output pins	Max. 32 pins	Max. 40 pins
Packages		64-pin LQFP	80-pin LQFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
   Refer to Tables 1.9 to 1.11, Pin Name Information by Pin Number, for details.

Table 1.2 Programmable I/O Ports Provided for Each Group

Programmable I/O Port	R8C/LA6A Group Total: 56 I/O pins								R8C/LA8A Group Total: 72 I/O pins							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P1	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P4	✓	✓	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P6	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:
1. The symbol "✓" indicates a programmable I/O port.
2. The symbol "—" indicates the settings should be made as follows:
   - Set 1 to the corresponding PDi (i = 0 to 9) register. When read, the content is 1.
   - Set 0 to the corresponding Pi (i = 0 to 9) register. When read, the content is 0.
   - Set 0 to the corresponding P7DRR or P8DRR register. When read, the content is 0.

Table 1.3 LCD Display Function Pins Provided for Each Group

Shared I/O Port	R8C/LA6A Group Common output: Max. 4 Segment output: Max. 32								R8C/LA8A Group Common output: Max. 4 Segment output: Max. 40							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	—	—	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	—	—	—	—	—	—	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	—	VL3(2)	VL2(2)	VL1(2)	COM 0	COM 1	COM 2	COM 3	—	VL3(2)	VL2(2)	VL1(2)	COM 0	COM 1	COM 2	COM 3

Notes:
1. The symbol "–" indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE0 to LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

1.1.3 Specifications

Tables 1.4 to 1.6 list the specifications.

Table 1.4 Specifications (1)

Item	Function		Specification
CPU	Central processing unit		R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V) 125 ns (f(XIN) = 8 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM/RAM Data flash		Refer to Tables 1.7 to 1.8 Product Lists.
Power Supply Voltage Detection	Voltage detection circuit		• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	R8C/LA6A Group	• CMOS I/O ports: 56, selectable pull-up resistor (1) • High current drive ports: 8
		R8C/LA8A Group	• CMOS I/O ports: 72, selectable pull-up resistor (1) • High current drive ports: 10
Clock	Clock generation circuits		4 circuits: XIN clock oscillation circuit XCIN clock oscillation circuit (32 kHz) High-speed on-chip oscillator (with frequency adjustment function) Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Division ratio selectable from 1, 2, 4, 8, and 16 • Low-power-consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode
			Real-time clock (timer RH)
Interrupts			• Number of interrupt vectors: 69 • External Interrupt: 16 (INT × 8, key input × 8) • Priority levels: 7 levels
Watchdog Timer			• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for watchdog timer

Note:
1. No pull-up resistor is provided in the pins P5_4 to P5_6.

Table 1.5 Specifications (2)

Item	Function		Specification	
Timer	Timer RB0 Timer RB1		8 bits × 2 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode	
	Timer RC		16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)	
	Timer RH		Real-time clock mode (counting of seconds, minutes, hours, day of the week, date, month, year), output compare mode	
	Timer RJ0 Timer RJ1	R8C/LA6A Group	Timer RJ0, Timer RJ1	16 bits × 3 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RJ2	R8C/LA8A Group	Timer RJ0, Timer RJ1, Timer RJ2	
Serial Interface	UART0		1 channel Clock synchronous serial I/O/UART	
	UART2		1 channel Clock synchronous serial I/O/UART, I^2C mode (I^2C-bus), multiprocessor communication function Only the R8C/LA8A Group has UART2.	
Synchronous Serial Communication Unit (SSU)			1 (shared with I^2C-bus)	
I^2C bus			1 (shared with SSU)	
A/D Converter		R8C/LA6A Group	10-bit resolution × 8 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 °C to 85°C)	
		R8C/LA8A Group	10-bit resolution × 12 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 °C to 85°C)	
Comparator B			2 circuits (comparator B1, comparator B3)	
LCD Drive Control Circuit		R8C/LA6A Group	Common output: Max. 4 pins Segment output: Max. 32 pins	• Bias: 1/2, 1/3 • Duty: static, 1/2, 1/3, 1/4
		R8C/LA8A Group	Common output: Max. 4 pins Segment output: Max. 40 pins	

Table 1.6 Specifications (3)

Item	Specification
Flash Memory	• Programming and erasure voltage: VCC = 1.8 V to 5.5 V (data flash VCC = 1.8 V to 5.5 V) • Programming and erasure endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/ Supply Voltage	f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 8 MHz (VCC = 1.8 V to 5.5 V)
Current Consumption	4.7 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 2.3 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 1.7 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.5 μA (VCC = 3.0 V, stop mode) 1.5 μA (VCC = 3.0 V, power-off 2 mode, timer RH enabled) 0.01 μA (VCC = 3.0 V, power-off 0 mode, timer RH disabled)
Operating Ambient Temperature	–20 to 85°C (N version) –40 to 85°C (D version) (1)

Note:
1. Specify the D version if D version functions are to be used.

1.2 Product Lists

Tables 1.7 and 1.8 list product information for each group. Figures 1.1 and 1.2 show the Correspondence of Part No., with Memory Size and Package for each group.

Table 1.7 Product List for R8C/LA6A Group **Current of Jul 2010**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA64ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	N Version
R5F2LA64ANFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA66ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	
R5F2LA66ANFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA67ANFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA67ANFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA68ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA68ANFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA64ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	D Version
R5F2LA64ADFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA66ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	
R5F2LA66ADFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA67ADFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA67ADFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA68ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA68ADFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	

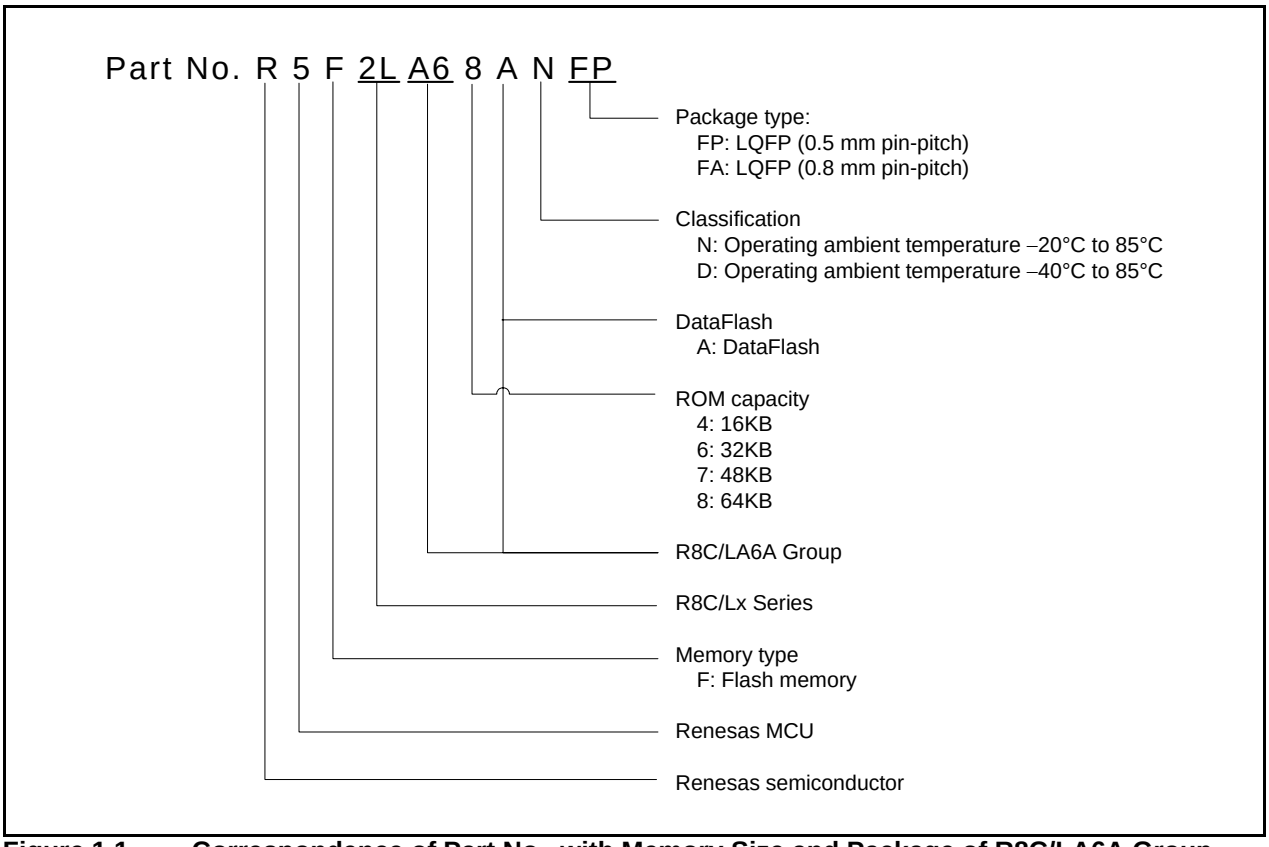


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/LA6A Group

Table 1.8 Product List for R8C/LA8A Group **Current of Jul 2010**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA84ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	N Version
R5F2LA84ANFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA86ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	
R5F2LA86ANFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA87ANFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA87ANFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA88ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA88ANFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA84ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	D Version
R5F2LA84ADFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA86ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	
R5F2LA86ADFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA87ADFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA87ADFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA88ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA88ADFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	

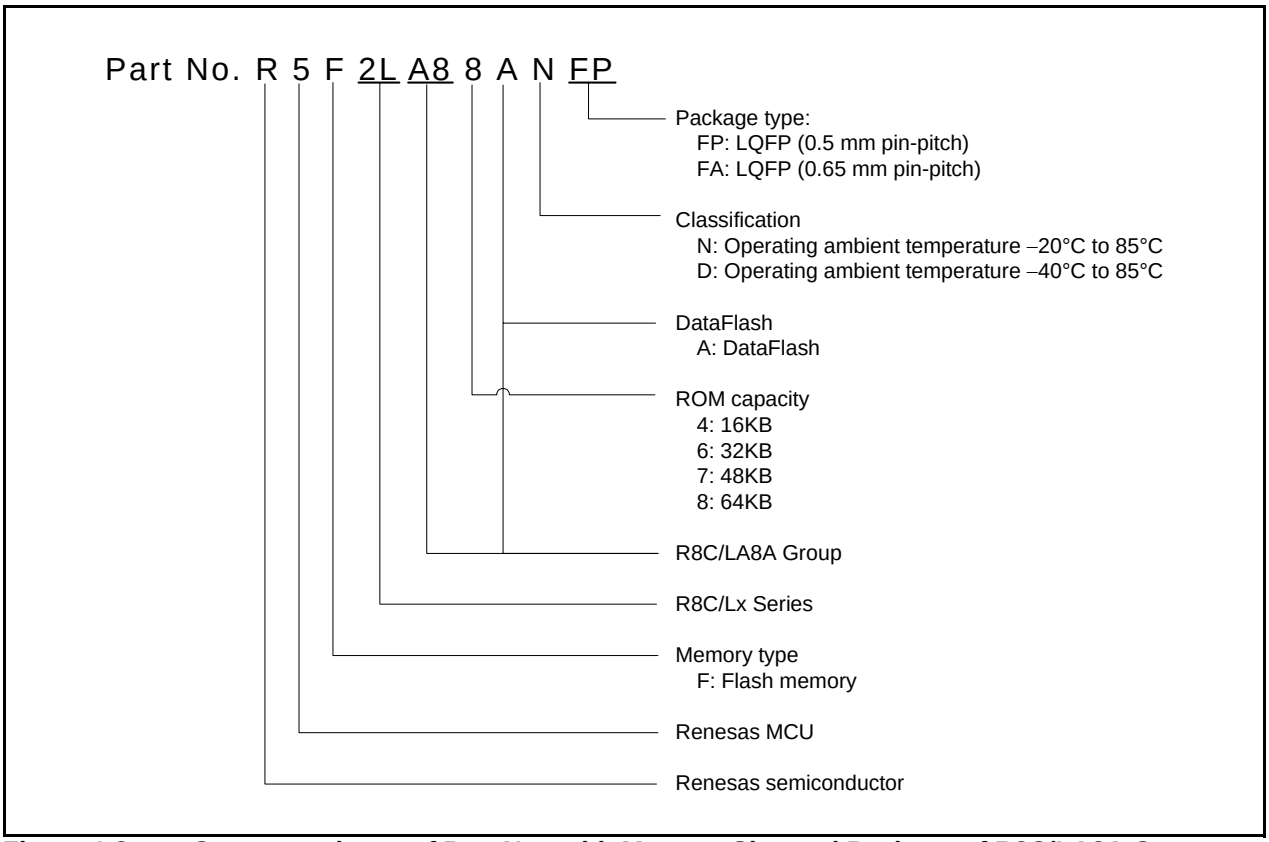


Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/LA8A Group

1.3 Block Diagrams

Figure 1.3 shows a Block Diagram of R8C/LA6A Group. Figure 1.4 shows a Block Diagram of R8C/LA8A Group.

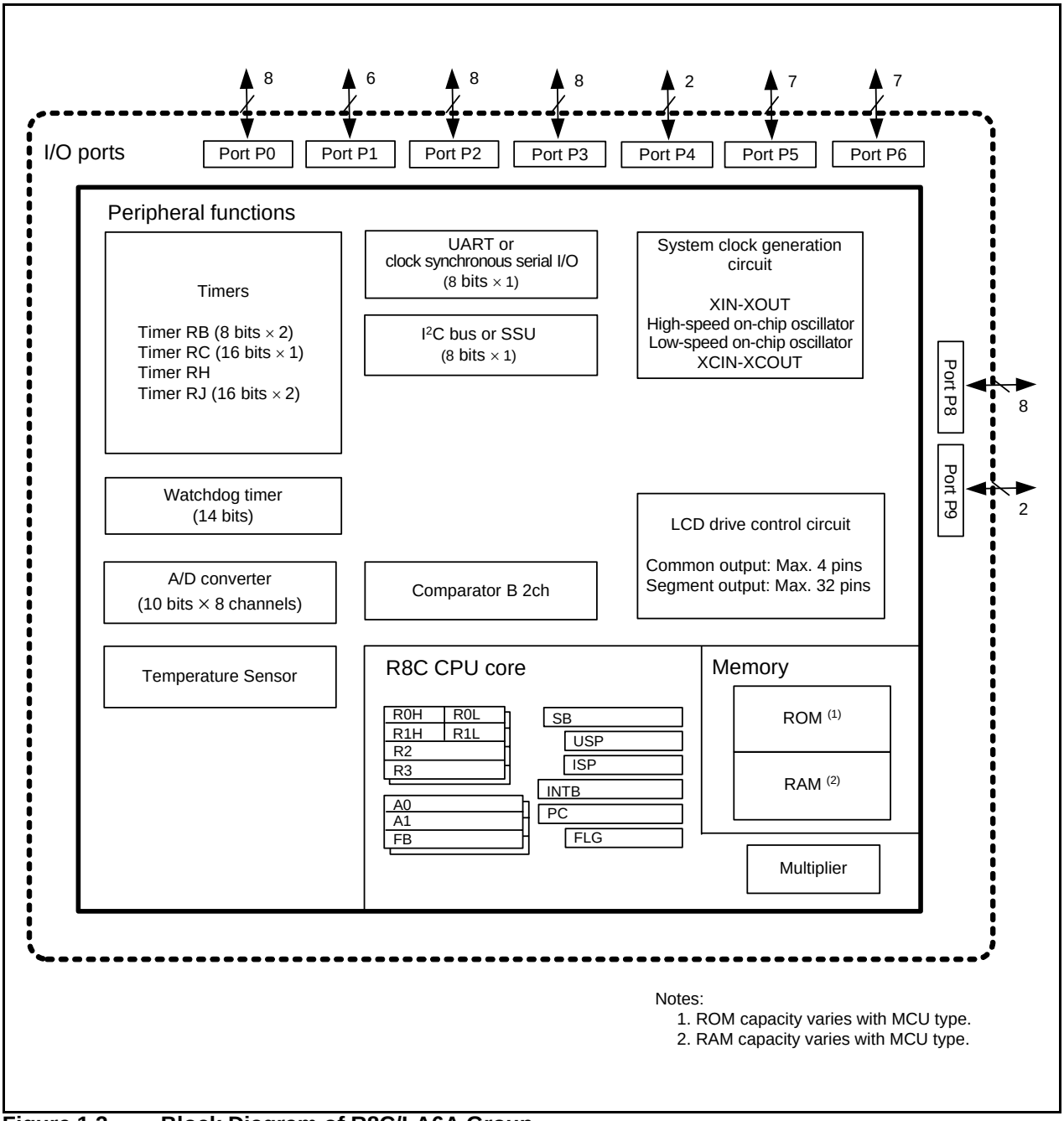


Figure 1.3 Block Diagram of R8C/LA6A Group

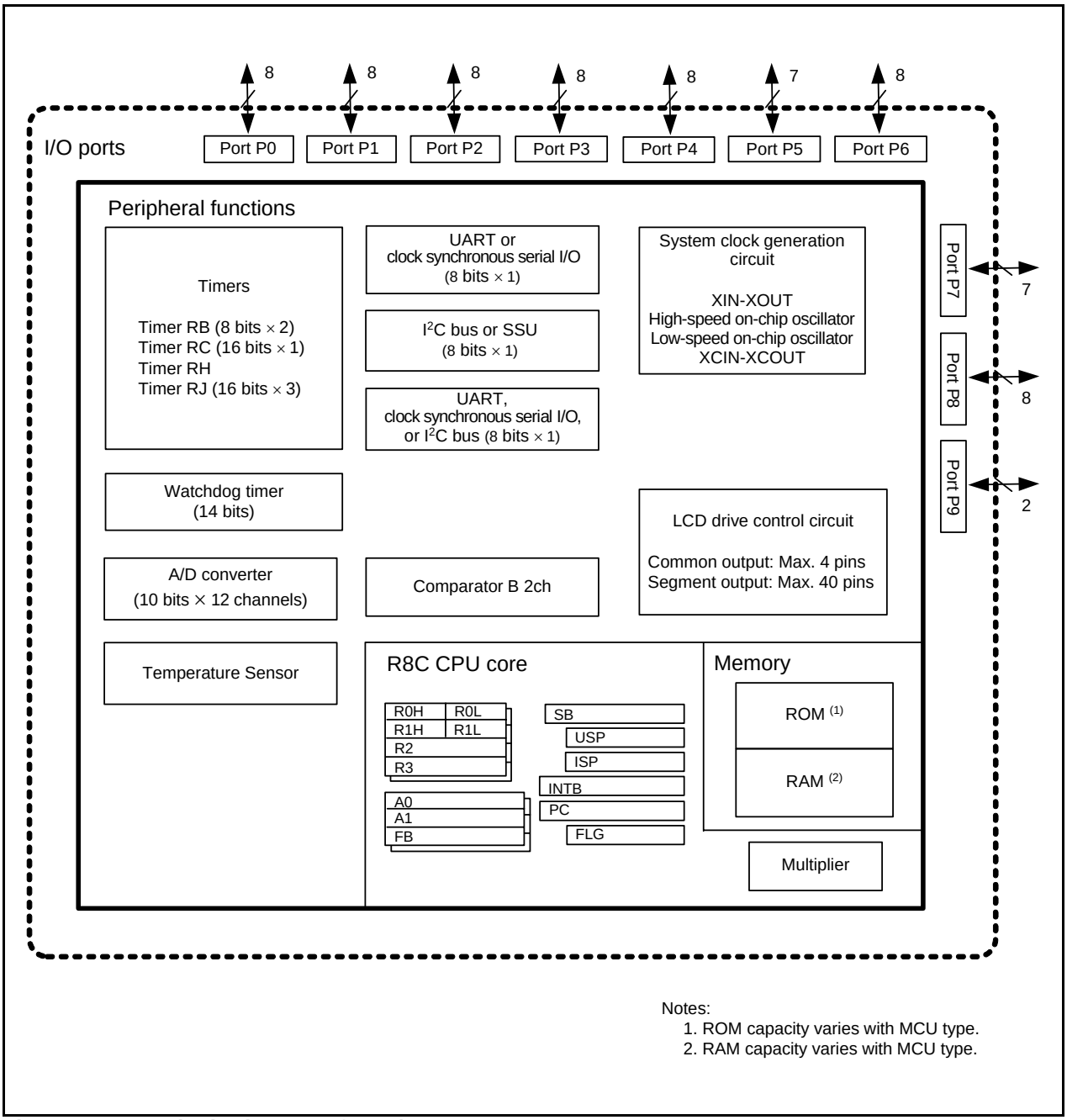
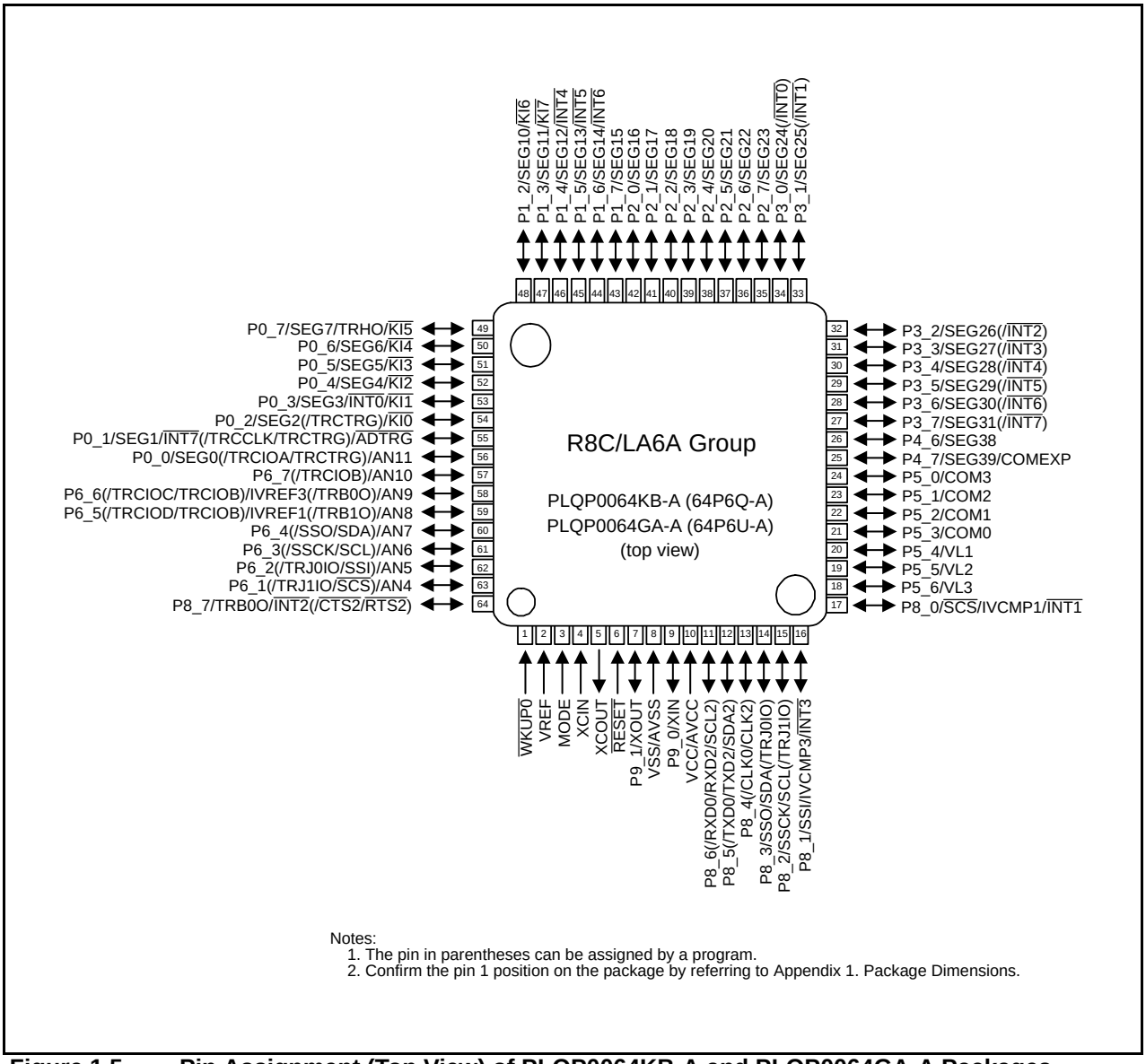


Figure 1.4 Block Diagram of R8C/LA8A Group

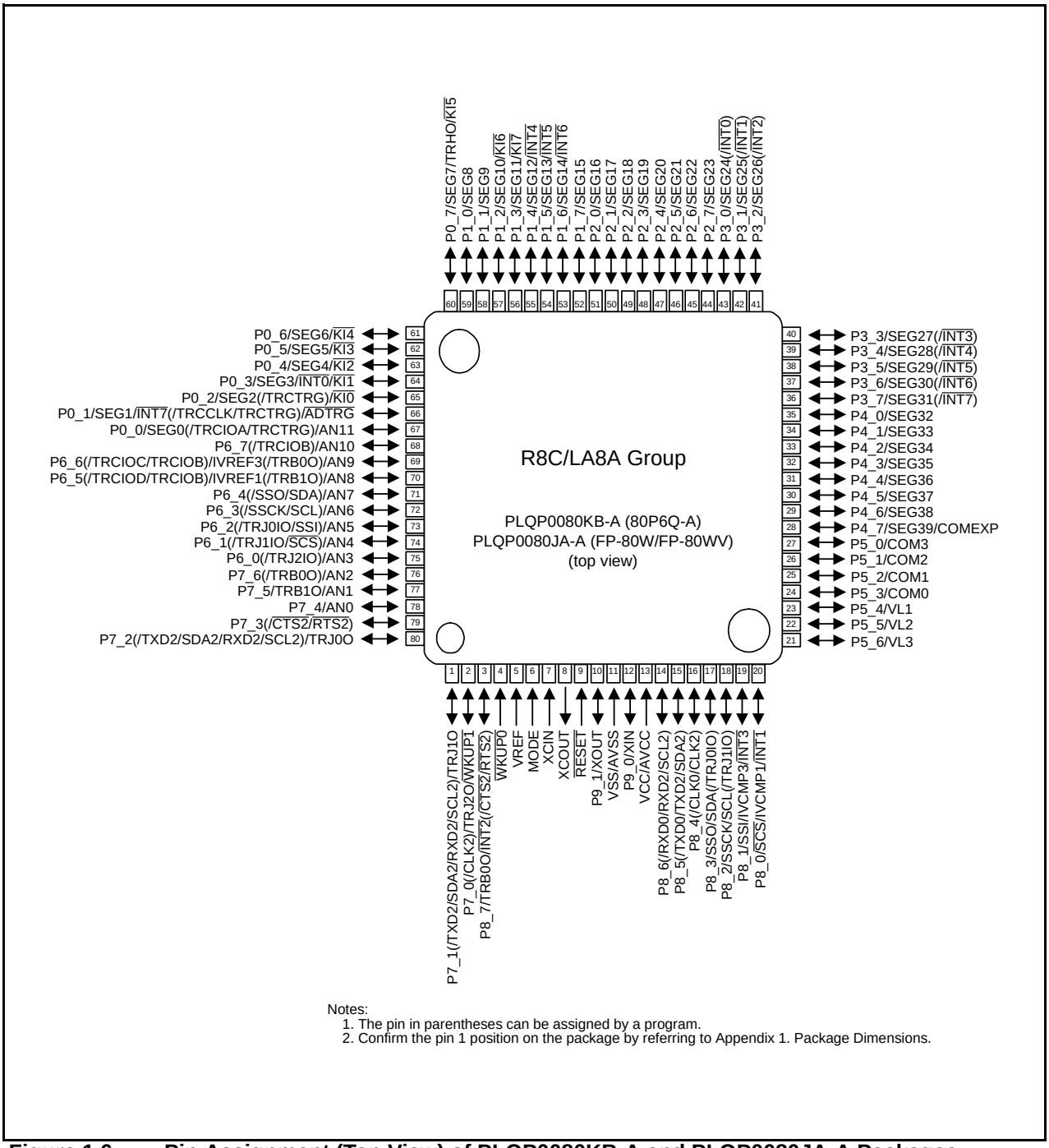
1.4 Pin Assignments

Figures 1.3 and 1.4 show pin assignments (top view). Tables 1.9 to 1.11 list the pin name information by pin number.



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to Appendix 1. Package Dimensions.

Figure 1.5 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to Appendix 1. Package Dimensions.

Figure 1.6 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

Table 1.9 Pin Name Information by Pin Number (1)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, Comparator B, Voltage Detection Circuit	LCD drive control circuit
1			P7_1		TRJ1O	(TXD2/SDA2/ RXD2/SCL2)				
2		$\overline{\text{WKUP1}}$	P7_0		TRJ2O	(CLK2)				
3	64		P8_7	$\overline{\text{INT2}}$	TRB0O	($\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$)				
4	1	$\overline{\text{WKUP0}}$								
5	2	VREF								
6	3	MODE								
7	4	XCIN								
8	5	XCOUT								
9	6	$\overline{\text{RESET}}$								
10	7	XOUT	P9_1							
11	8	VSS/ AVSS								
12	9	XIN	P9_0							
13	10	VCC/ AVCC								
14	11		P8_6			(RXD0/RXD2/ SCL2)				
15	12		P8_5			(TXD0/TXD2/ SDA2)				
16	13		P8_4			(CLK0/CLK2)				
17	14		P8_3		(TRJ0IO)		SSO	SDA		
18	15		P8_2		(TRJ1IO)		SSCK	SCL		
19	16		P8_1	$\overline{\text{INT3}}$			SSI		IVCMP3	
20	17		P8_0	$\overline{\text{INT1}}$			$\overline{\text{SCS}}$		IVCMP1	
21	18		P5_6							VL3
22	19		P5_5							VL2
23	20		P5_4							VL1
24	21		P5_3							COM0
25	22		P5_2							COM1
26	23		P5_1							COM2
27	24		P5_0							COM3
28	25		P4_7							SEG39/ COMEXP
29	26		P4_6							SEG38
30			P4_5							SEG37

Note:
1. The pin in parentheses can be assigned by a program.

Table 1.10 Pin Name Information by Pin Number (2)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, Comparator B, Voltage Detection Circuit	LCD drive control circuit
31			P4_4							SEG36
32			P4_3							SEG35
33			P4_2							SEG34
34			P4_1							SEG33
35			P4_0							SEG32
36	27		P3_7	($\overline{INT7}$)						SEG31
37	28		P3_6	($\overline{INT6}$)						SEG30
38	29		P3_5	($\overline{INT5}$)						SEG29
39	30		P3_4	($\overline{INT4}$)						SEG28
40	31		P3_3	($\overline{INT3}$)						SEG27
41	32		P3_2	($\overline{INT2}$)						SEG26
42	33		P3_1	($\overline{INT1}$)						SEG25
43	34		P3_0	($\overline{INT0}$)						SEG24
44	35		P2_7							SEG23
45	36		P2_6							SEG22
46	37		P2_5							SEG21
47	38		P2_4							SEG20
48	39		P2_3							SEG19
49	40		P2_2							SEG18
50	41		P2_1							SEG17
51	42		P2_0							SEG16
52	43		P1_7							SEG15
53	44		P1_6	$\overline{INT6}$						SEG14
54	45		P1_5	$\overline{INT5}$						SEG13
55	46		P1_4	$\overline{INT4}$						SEG12
56	47		P1_3	$\overline{KI7}$						SEG11
57	48		P1_2	$\overline{KI6}$						SEG10
58			P1_1							SEG9
59			P1_0							SEG8
60	49		P0_7	$\overline{KI5}$	TRHO					SEG7
61	50		P0_6	$\overline{KI4}$						SEG6
62	51		P0_5	$\overline{KI3}$						SEG5
63	52		P0_4	$\overline{KI2}$						SEG4
64	53		P0_3	$\overline{KI1}$ $\overline{INT0}$						SEG3
65	54		P0_2	$\overline{KI0}$	(TRCTRG)					SEG2
66	55		P0_1	$\overline{INT7}$	(TRCTRG/ TRCCLK)				$\overline{ADTRG}$	SEG1
67	56		P0_0		(TRCIOA/ TRCTRG)				AN11	SEG0
68	57		P6_7		(TRCIOB)				AN10	

Note:
1. The pin in parentheses can be assigned by a program.

Table 1.11 Pin Name Information by Pin Number (3)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, Comparator B, Voltage Detection Circuit	LCD drive control circuit
69	58		P6_6		(TRB0O/ TRCIOB/ TRCIOC)				AN9/IVREF3	
70	59		P6_5		(TRB1O/ TRCIOB/ TRCIOD)				AN8/IVREF1	
71	60		P6_4				(SSO)	(SDA)	AN7	
72	61		P6_3				(SSCK)	(SCL)	AN6/IVCMP1	
73	62		P6_2		(TRJ0IO)		(SSI)		AN5	
74	63		P6_1		(TRJ1IO)		($\overline{SCS}$)		AN4	
75			P6_0		(TRJ2IO)				AN3	
76			P7_6		(TRB0O)				AN2	
77			P7_5		TRB1O				AN1	
78			P7_4						AN0	
79			P7_3			($\overline{CTS2}$/$\overline{RTS2}$)				
80			P7_2		TRJ0O	(RXD2/SCL2/ TXD2/SDA2)				

Note:
1. The pin in parentheses can be assigned by a program.

1.5 Pin Functions

Tables 1.12 and 1.13 list pin functions.

Table 1.12 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off 0 mode exit input	$\overline{\text{WKUP0}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.
	$\overline{\text{WKUP1}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins
Timer RB	TRB0O, TRB1O	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RH	TRHO	O	Timer RH output pin
Timer RJ	TRJ0IO, TRJ1IO, TRJ2IO	I/O	Timer RJ I/O pins
	TRJ0IO, TRJ1IO, TRJ2IO	O	Timer RJ output pins
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD2	I	Serial data input pins
	TXD0, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 1.13 Pin Functions (2)

Item	Pin Name	I/O Type	Description
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{SCS}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter
A/D converter	AN0 to AN11	I	A/D converter analog input pins
	$\overline{ADTRG}$	I	AD external trigger input pin
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_6, P6_0 to P6_7 P7_0 to P7_6, P8_0 to P8_7, P9_0, P9_1	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Ports P7_0, P7_1 and P8 can be used as LED drive ports.
Segment output	SEG0 to SEG39	O	LCD segment output pins
Common output	COM0 to COM3, COMEXP	O	LCD common output pins
LCD power supply	VL1	I	Apply the following voltage: 1 V ≤ VL1 ≤ VCC and VL1 ≤ VL2.
	VL2	I	Apply the following voltage: VL2 ≤ 5.5 V and VL1 ≤ VL2 ≤ VL3.
	VL3	I	Apply the following voltage: VL3 ≤ 5.5 V and VL2 ≤ VL3.

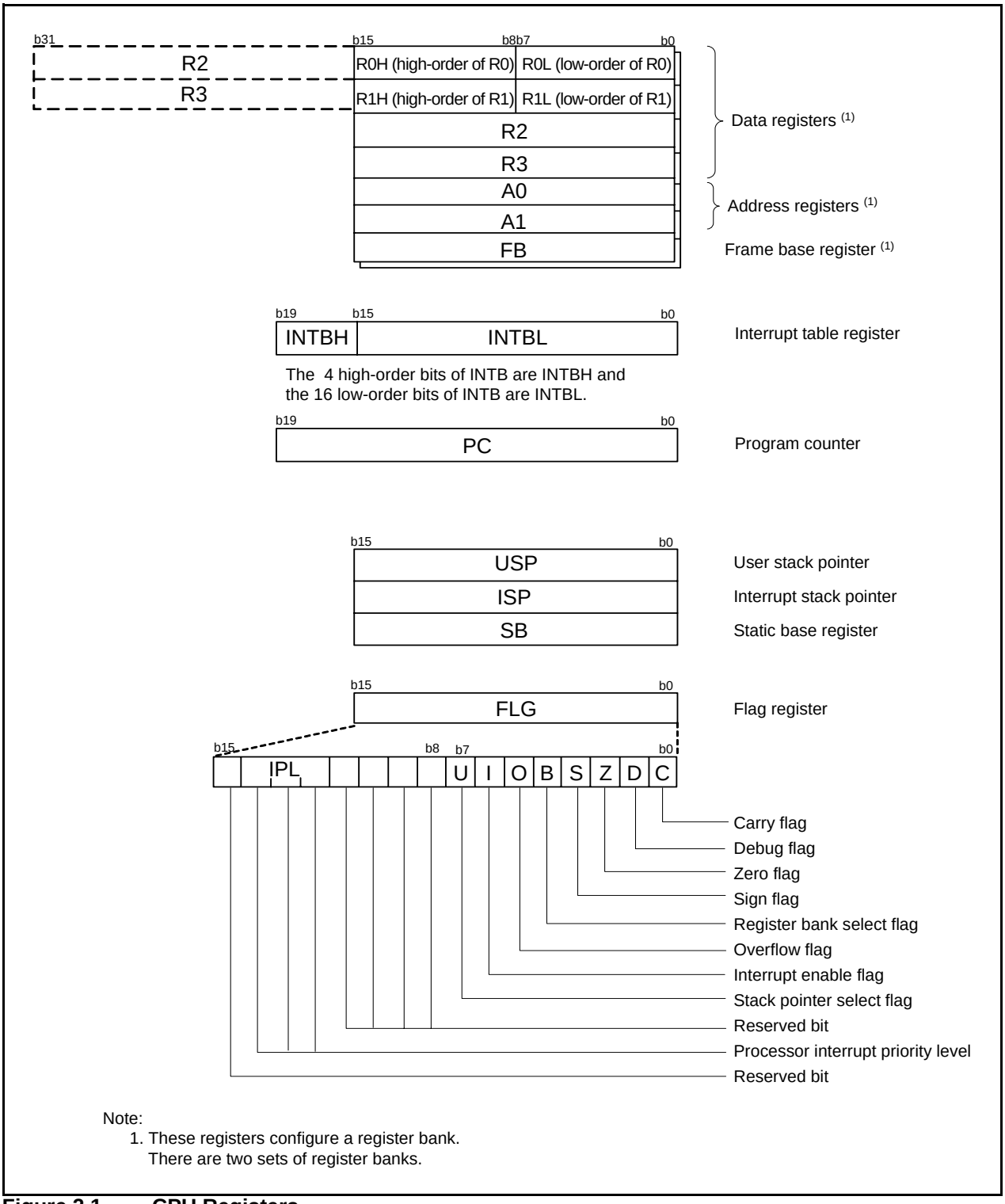
I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.



Note:
1. These registers configure a register bank.
There are two sets of register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

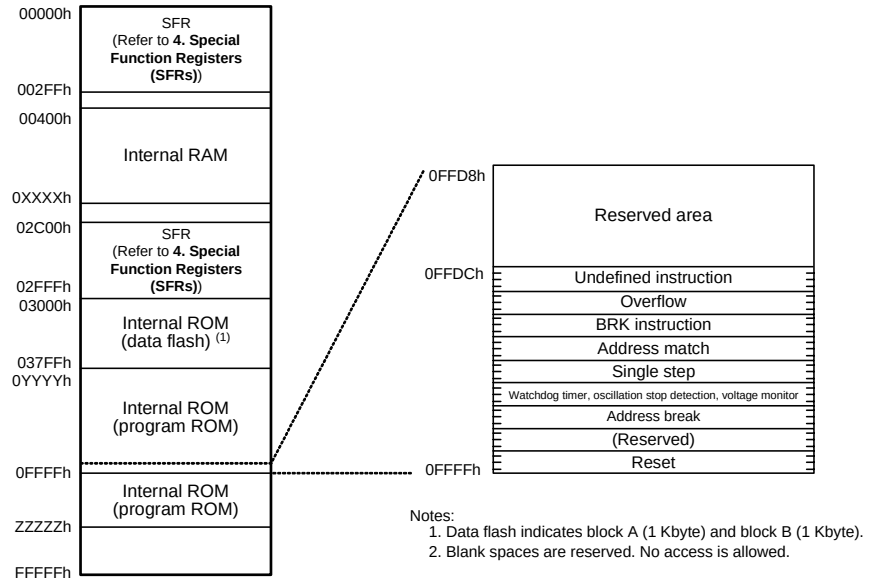
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

Figure 3.1 is a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 037FFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 3.5-Kbyte internal RAM area is allocated addresses 00400h to 011FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Part Number	Internal ROM			Internal RAM		Data Flash
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh	
R5F2LA64ANFP, R5F2LA64ANFA, R5F2LA64ADFP, R5F2LA64ADFA, R5F2LA84ANFP, R5F2LA84ANFA, R5F2LA84ADFP, R5F2LA84ADFA	16 Kbytes	0C000h	0FFFFh	2 Kbytes	00BFFh	Available
R5F2LA66ANFP, R5F2LA66ANFA, R5F2LA66ADFP, R5F2LA66ADFA, R5F2LA86ANFP, R5F2LA86ANFA, R5F2LA86ADFP, R5F2LA86ADFA	32 Kbytes	08000h	0FFFFh	2 Kbytes	00BFFh	
R5F2LA67ANFP, R5F2LA67ANFA, R5F2LA67ADFP, R5F2LA67ADFA, R5F2LA87ANFP, R5F2LA87ANFA, R5F2LA87ADFP, R5F2LA87ADFA	48 Kbytes	04000h	0FFFFh	3.5 Kbytes	011FFh	
R5F2LA68ANFP, R5F2LA68ANFA, R5F2LA68ADFP, R5F2LA68ADFA, R5F2LA88ANFP, R5F2LA88ANFA, R5F2LA88ADFP, R5F2LA88ADFA	64 Kbytes	04000h	13FFFh	3.5 Kbytes	011FFh	

Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.9 list SFR information and Table 4.10 lists the ID Code Areas and Option Function Select Area. The description offered in this chapter is based on the R8C/LA8A Group.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h 00000100b (2)
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register 0	MSTCR0	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh (3)
000Ch	Oscillation Stop Detection Register	OCD	00000100b (4) 00h (4)
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h	Module Standby Control Register 1	MSTCR1	00h
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (5)
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	XXXXXX00b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Frequency Control Register 0	FRC0	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator 18 MHz Set Value Register 0	FR18S0	XXh
002Ah	High-Speed On-Chip Oscillator 18 MHz Set Value Register 1	FR18S1	XXh
002Bh			
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Frequency Control Register 1	FRC1	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (6) 00100000b (7)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (6) 1100X011b (7)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:
1. Blank spaces are reserved. No access is allowed.
2. The CSPRO bit in the CSPR register is set to 1.
3. The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
4. The reset value differs depending on the mode.
5. The CSPROINI bit in the OFS register is set to 0.
6. The LVDAS bit in the OFS register is set to 1.
7. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h	INT7 Interrupt Control Register	INT7IC	XX00X000b
0044h	INT6 Interrupt Control Register	INT6IC	XX00X000b
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RH Interrupt Control Register	TRHIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RJ0 Interrupt Control Register	TRJ0IC	XXXXX000b
0057h	Timer RB1 Interrupt Control Register	TRB1IC	XXXXX000b
0058h	Timer RB0 Interrupt Control Register	TRB0IC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RJ1 Interrupt Control Register	TRJ1IC	XXXXX000b
005Ch	Timer RJ2 Interrupt Control Register	TRJ2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	LCD Interrupt Control Register	LCDIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h	Timer RJ2 Control Register	TRJ2CR	00h
0091h	Timer RJ2 I/O Control Register	TRJ2IOC	00h
0092h	Timer RJ2 Mode Register	TRJ2MR	00h
0093h	Timer RJ2 Event Pin Select Register	TRJ2ISR	00h
0094h	Timer RJ2 Register	TRJ2	FFh
0095h			FFh
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh	A/D Control Register 2	ADCON2	00h
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h	Port P8 Register	P8	XXh
00F1h	Port P9 Register	P9	XXh
00F2h	Port P8 Direction Register	PD8	00h
00F3h	Port P9 Direction Register	PD9	00h
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h			
0101h			
0102h			
0103h			
0104h			
0105h			
0106h			
0107h			
0108h	Timer RB0 Control Register	TRB0CR	00h
0109h	Timer RB0 One-Shot Control Register	TRB0OCR	00h
010Ah	Timer RB0 I/O Control Register	TRB0IOC	00h
010Bh	Timer RB0 Mode Register	TRB0MR	00h
010Ch	Timer RB0 Prescaler Register	TRB0PRE	FFh
010Dh	Timer RB0 Secondary Register	TRB0SC	FFh
010Eh	Timer RB0 Primary Register	TRB0PR	FFh
010Fh			
0110h	Timer RH Second Data Register / Counter Data Register	TRHSEC	XXh 00h (2)
0111h	Timer RH Minute Data Register / Compare Data Register	TRHMIN	XXh 00h (2)
0112h	Timer RH Hour Data Register	TRHHR	00XXXXXXb 00h (2)
0113h	Timer RH Day-of-the-Week Data Register	TRHWK	00000XXXb 00h (2)
0114h	Timer RH Date Data Register	TRHDY	00XXXXXXb 00000001b (2)
0115h	Timer RH Month Data Register	TRHMON	000XXXXXb 00000001b (2)
0116h	Timer RH Year Data Register	TRHYR	XXh 00h (2)
0117h	Timer RH Control Register	TRHCR	XXX00X0Xb 000XX1X0b (2)
0118h	Timer RH Count Source Select Register	TRHCSR	X0001000b 0XXXXXXXb (2)
0119h	Timer RH Clock Error Correction Register	TRHADJ	XXh 00h (2)
011Ah	Timer RH Interrupt Flag Register	TRHIFR	00000XXXb 000XX000b (2)
011Bh	Timer RH Interrupt Enable Register	TRHIER	XXh 00h (2)
011Ch	Timer RH Alarm Minute Register	TRHAMN	XXh 00h (2)
011Dh	Timer RH Alarm Hour Register	TRHAHR	XXh 00h (2)
011Eh	Timer RH Alarm Day-of-the-Week Register	TRHAWK	X0000XXXb 00h (2)
011Fh	Timer RH Protect Register	TRHPRC	00h X0000000b (2)
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RJ Pin Select Register	TRJSR	00h
0181h	Timer RB Pin Select Register	TRBSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh	Timer RH Second Interrupt Control Register	TRHICR	X0XXXXXXb 00000001b (3)
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	000000X0b
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h	Port P1 Pull-Up Control Register	P1PUR	00h
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h	Port P4 Pull-Up Control Register	P4PUR	00h
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h	Port P6 Pull-Up Control Register	P6PUR	00h
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h	Port P8 Pull-Up Control Register	P8PUR	00h
01E9h	Port P9 Pull-Up Control Register	P9PUR	00h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P7 Drive Capacity Control Register	P7DRR	00h
01F1h	Port P8 Drive Capacity Control Register	P8DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h			
0202h	LCD Option Clock Control Register	LCR2	00h
0203h	LCD Clock Control Register	LCR3	00h
0204h	LCD Display Control Register	LCR4	00h
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h	LCD Port Select Register 3	LSE3	00h
020Ah	LCD Port Select Register 4	LSE4	00h
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch			
020Dh			
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh		LRA27L	XXh
022Ch		LRA28L	XXh
022Dh		LRA29L	XXh
022Eh		LRA30L	XXh
022Fh		LRA31L	XXh
0230h		LRA32L	XXh
0231h		LRA33L	XXh
0232h		LRA34L	XXh
0233h		LRA35L	XXh
0234h		LRA36L	XXh
0235h		LRA37L	XXh
0236h		LRA38L	XXh
0237h		LRA39L	XXh
:			
2FFFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.10 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Resets

The following resets are available: hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources and Figure 5.1 shows the Reset Circuit Block Diagram.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	The input voltage to the $\overline{\text{RESET}}$ pin is held low.
Power-on reset	VCC rises.
Voltage monitor 0 reset	VCC falls. (Monitor voltage: Vdet0)
Watchdog timer reset	Underflow of the watchdog timer
Software reset	Write 1 to the PM03 bit in the PM0 register.

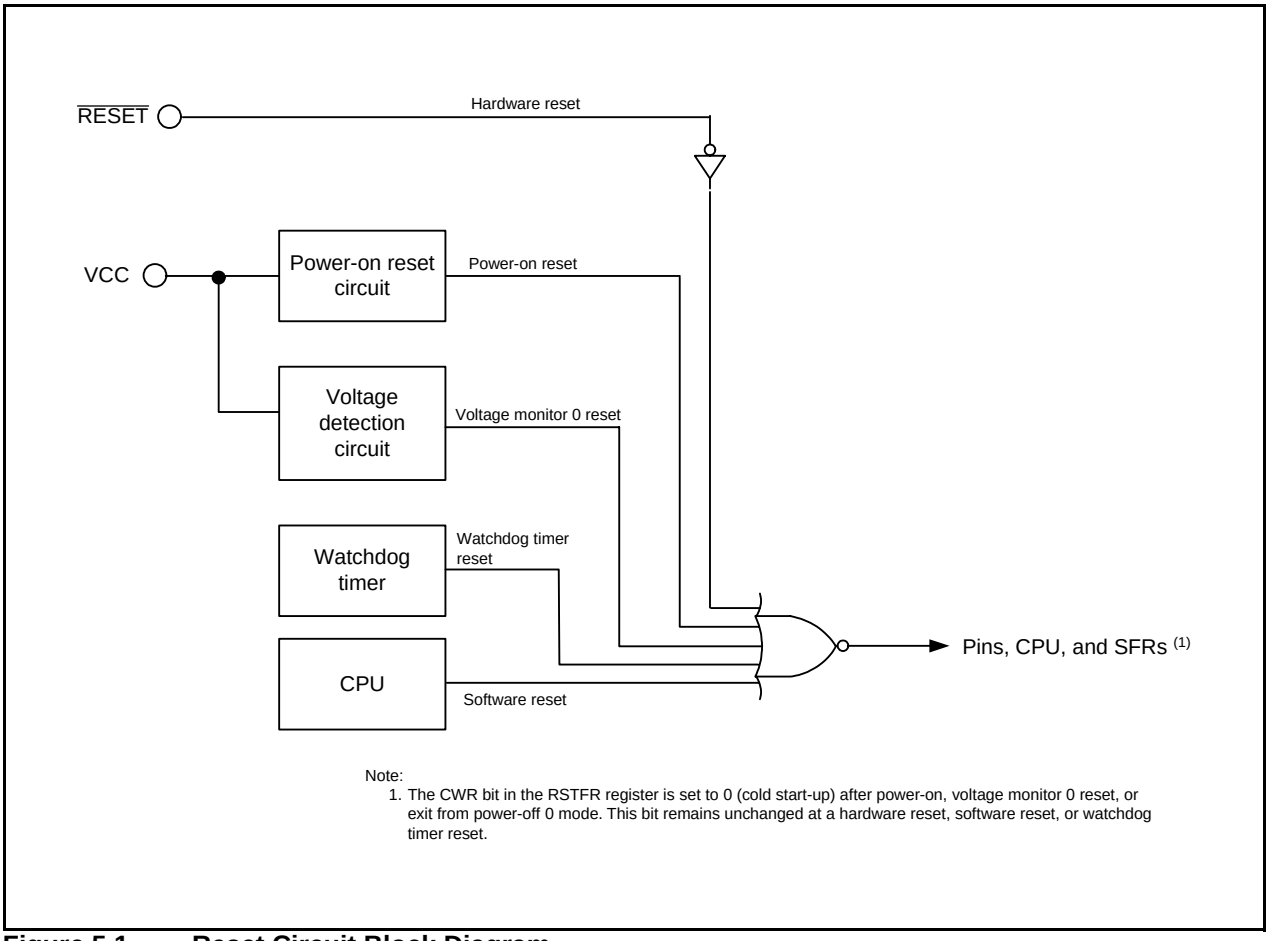

RESET
Hardware reset
VCC
Power-on reset circuit
Power-on reset
Voltage detection circuit
Voltage monitor 0 reset
Watchdog timer
Watchdog timer reset
CPU
Software reset
Pins, CPU, and SFRs (1)
Note:
1. The CWR bit in the RSTFR register is set to 0 (cold start-up) after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.

Figure 5.1 Reset Circuit Block Diagram

Table 5.2 shows the Pin Status while $\overline{\text{RESET}}$ Pin Level is Low. Figure 5.2 shows the CPU Register Status after Reset and Figure 5.3 shows the Reset Sequence.

Table 5.2 Pin Status while $\overline{\text{RESET}}$ Pin Level is Low

Pin Name	Pin Status
P0 to P4, P5_0 to P5_6, P6, P7_0 to P7_6, P8, P9_0 to P9_1	High impedance
$\overline{\text{WKUP0}}$	High impedance
XCIN, XCOUT	Undefined
VL1 to VL3	High impedance

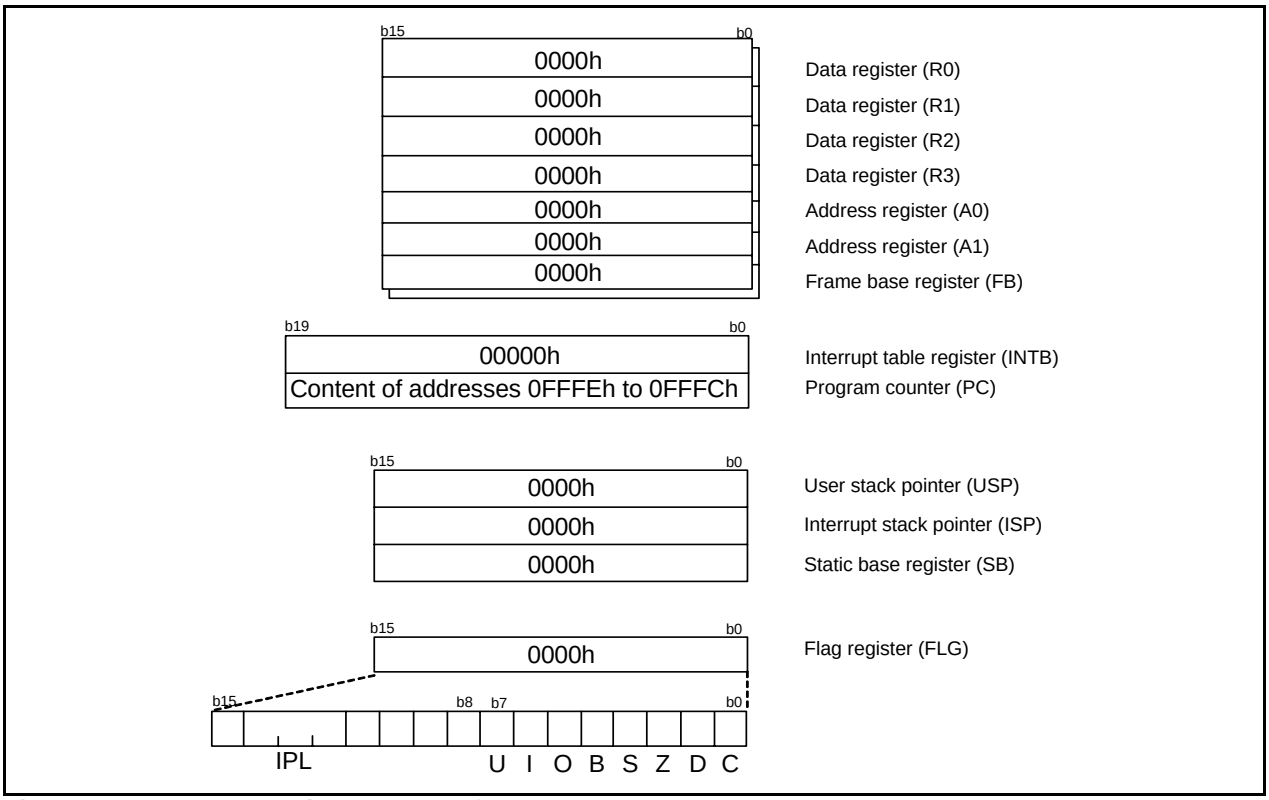
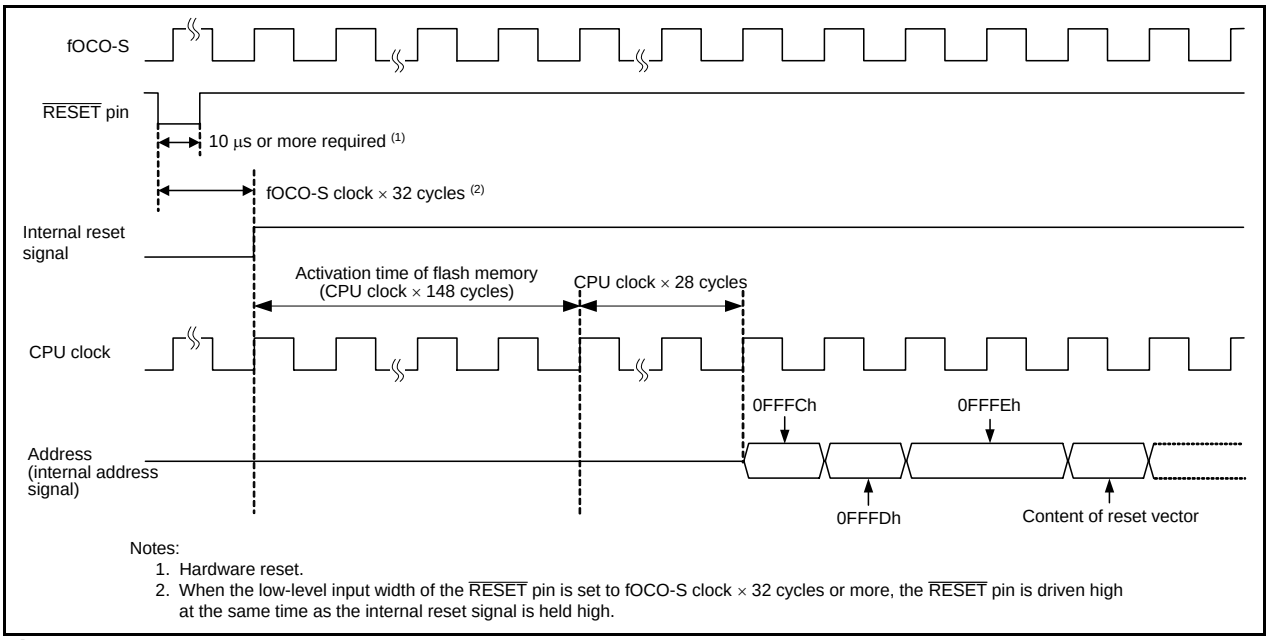


Figure 5.2 CPU Register Status after Reset



Notes:
1. Hardware reset.
2. When the low-level input width of the $\overline{\text{RESET}}$ pin is set to fOCO-S clock × 32 cycles or more, the $\overline{\text{RESET}}$ pin is driven high at the same time as the internal reset signal is held high.

Figure 5.3 Reset Sequence

5.1 Registers

5.1.1 Processor Mode Register 0 (PM0)

Address 0004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	Setting this bit to 1 resets the MCU. When read, the content is 0.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

5.1.2 Reset Source Determination Register (RSTFR)

Address 000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDR	SWR	HWR	CWR	
After Reset	X	X	X	X	X	X	X	X	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag (2, 3)	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag (4)	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Reserved bits	When read, the content is undefined.	R
b5	—			
b6	—			
b7	—			

Notes:
1. The CWR bit is set to 0 (cold start-up) after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
2. When 1 is written to the CWR bit by a program, it is set to 1. (Writing 0 does not affect this bit.)
3. When the VW0C0 bit in the VW0C register is set to 0 (voltage monitor 0 reset disabled), the CWR bit value is undefined.
4. A hardware reset or an exit from power-off 0 mode is detected.

5.1.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

5.1.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **14.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

5.2 Hardware Reset

A reset is applied using the $\overline{\text{RESET}}$ pin. When a low-level signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, the pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Status while $\overline{\text{RESET}}$ Pin Level is Low**, **Figure 5.2 CPU Register Status after Reset**, and **Table 4.1** to **Table 4.10 SFR Information**).

When the input level applied to the $\overline{\text{RESET}}$ pin changes from low to high, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after reset.

The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled low while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.

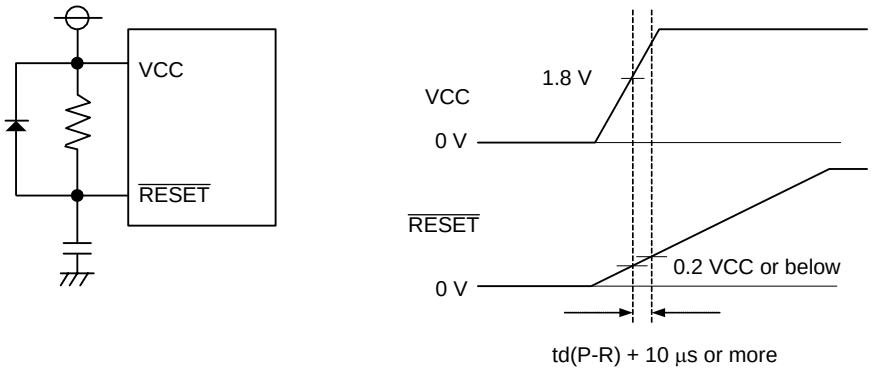
Figure 5.4 shows an Example of Hardware Reset Circuit and Operation and Figure 5.5 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.2.1 When Power Supply is Stable

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.

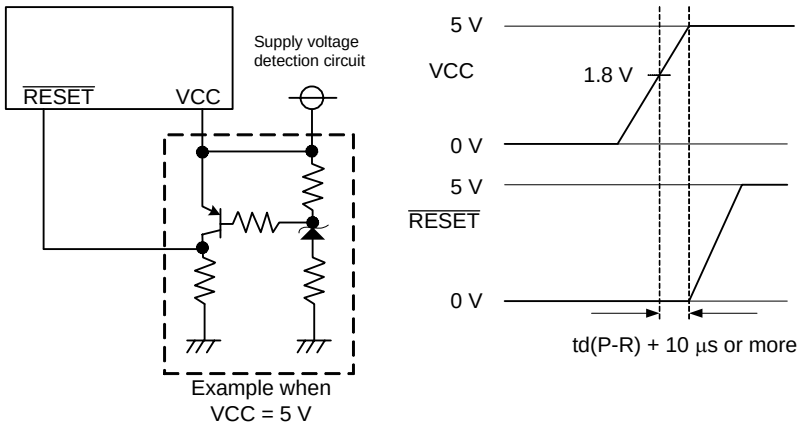
5.2.2 Power On

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **30. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.



Note:
1. Refer to **30. Electrical Characteristics**.

Figure 5.4 Example of Hardware Reset Circuit and Operation



Note:
1. Refer to **30. Electrical Characteristics**.

Figure 5.5 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.3 Power-On Reset Function

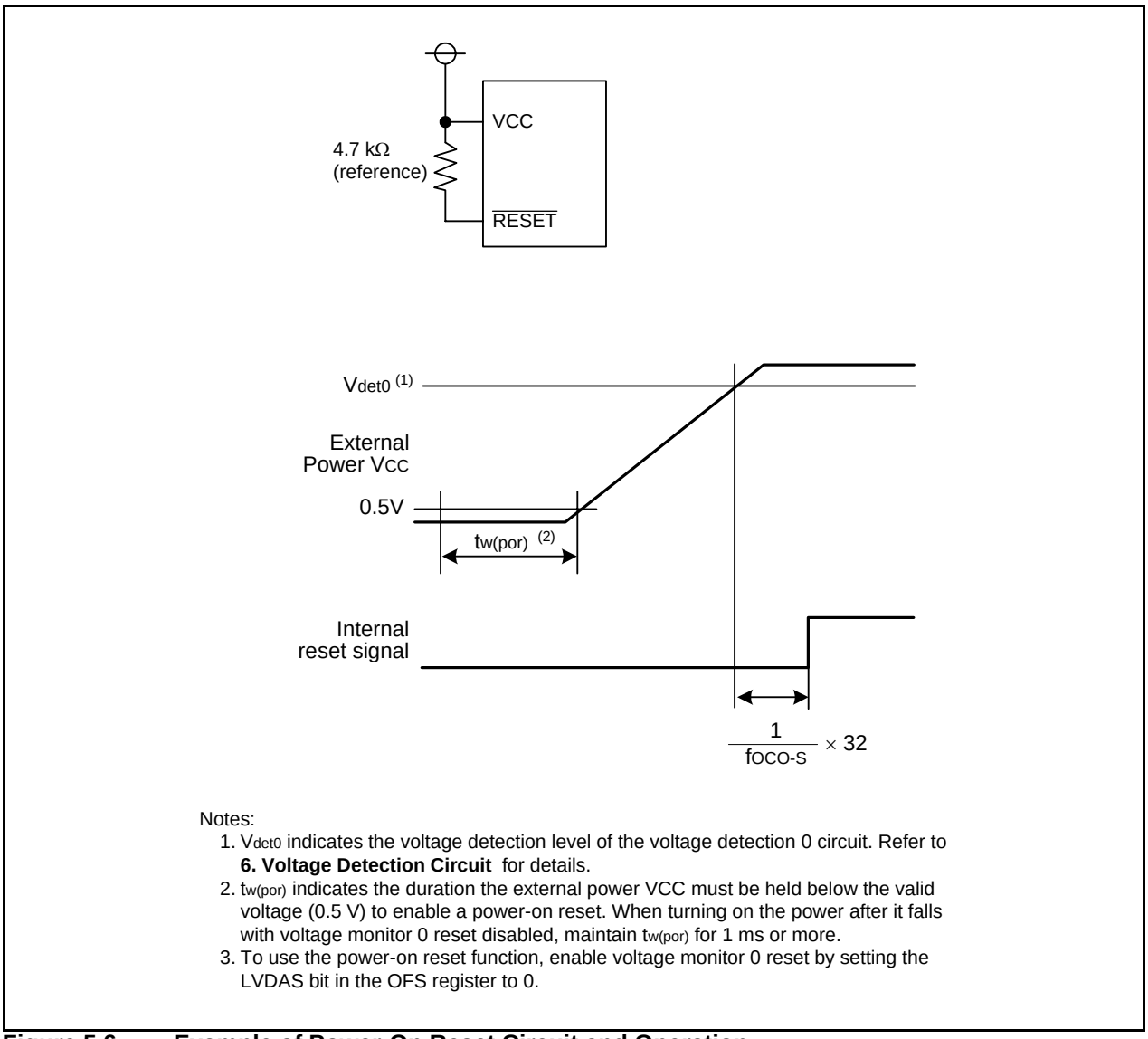
When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises, the power-on reset function is enabled and the pins, CPU, and SFRs are reset. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8 VCC or above.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held high and the MCU enters the reset sequence (refer to Figure 5.3). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after power-on reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 shows an Example of Power-On Reset Circuit and Operation.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 Example of Power-On Reset Circuit and Operation

5.4 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0. To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset). The Vdet0 voltage detection level can be changed by the settings of bits VDSEL0 and VDSEL1 in the OFS register.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFRs are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held high and the MCU enters the reset sequence (refer to Figure 5.3). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after a reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Bits VDSEL0 to VDSEL1 and LVDAS cannot be changed by a program. To set these bits, write values to b4 to b6 of address 0FFFFh using a flash programmer.

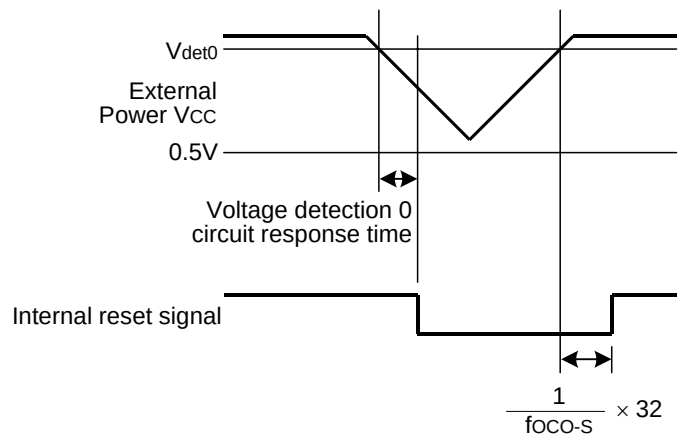
Refer to **5.1.3 Option Function Select Register (OFS)** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

Figure 5.7 shows an Example of Voltage Monitor 0 Reset Circuit and Operation.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.7 Example of Voltage Monitor 0 Reset Circuit and Operation

5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFRs when the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after watchdog timer reset.
The internal RAM is not reset. When the watchdog timer underflows while writing to the internal RAM is in progress, the contents of internal RAM are undefined.
The underflow period and refresh acknowledge period for the watchdog timer can be set by bits WDTUFS0 and WDTUFS1 and bits WDTRCS0 and WDTRCS1 in the OFS2 register, respectively.
Refer to **15. Watchdog Timer** for details of the watchdog timer.

5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFRs. The program beginning with the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock with no division is automatically selected for the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after software reset.
The internal RAM is not reset.

5.7 Cold Start-Up/Warm Start-Up Determination Function

The cold start-up/warm start-up determination function uses the CWR bit in the RSTFR register to determine cold start-up (reset process) at power-on and warm start-up (reset process) when a reset occurred during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 at a voltage monitor 0 reset or an exit from power-off 0 mode. When 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm start-up determination function uses voltage monitor 0 reset.
Figure 5.8 shows an Operating Example of Cold Start-Up/Warm Start-Up Function

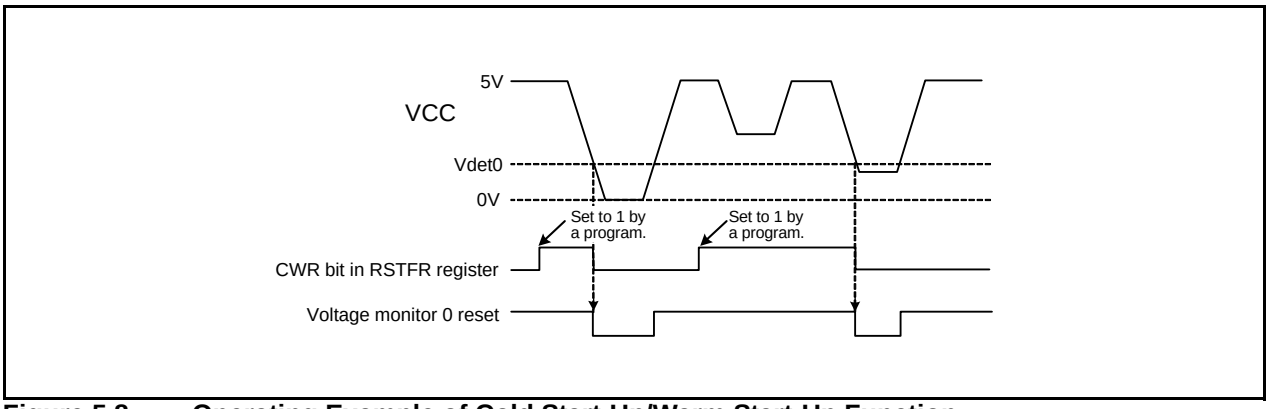


Figure 5.8 Operating Example of Cold Start-Up/Warm Start-Up Function

5.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset or an exit from power-off 0 mode occurs, the HWR bit is set to 1 (detected).
If a software reset occurs, the SWR bit is set to 1 (detected).
If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6. Voltage Detection Circuit

The voltage detection circuit monitors the voltage input to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program.

6.1 Introduction

The detection voltage of voltage detection 0 can be selected among four levels using the OFS register.
The detection voltage of voltage detection 1 can be selected among 16 levels using the VD1LS register.
The voltage monitor 0 reset, and voltage monitor 1 interrupt and voltage monitor 2 interrupt can also be used.

Table 6.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1	Voltage Monitor 2
VCC monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by falling	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
	Detection voltage	Selectable among 4 levels using the OFS register.	Selectable among 16 levels using the VD1LS register.	VCC
	Monitor	None	The VW1C3 bit in the VW1C register	The VCA13 bit in the VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC or LVCMP2 input voltage is higher or lower than Vdet2
Process at voltage detection	Reset	Voltage monitor 0 reset	None	None
		Reset at Vdet0 > VCC; CPU operation restarts at VCC > Vdet0		
	Interrupts	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request at: Vdet1 > VCC and/or VCC > Vdet1	Interrupt request at: Vdet2 > VCC and/or VCC > Vdet2
Digital filter	Switching enable/ disable	No digital filter function	Supported	Supported
	Sampling time	—	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8

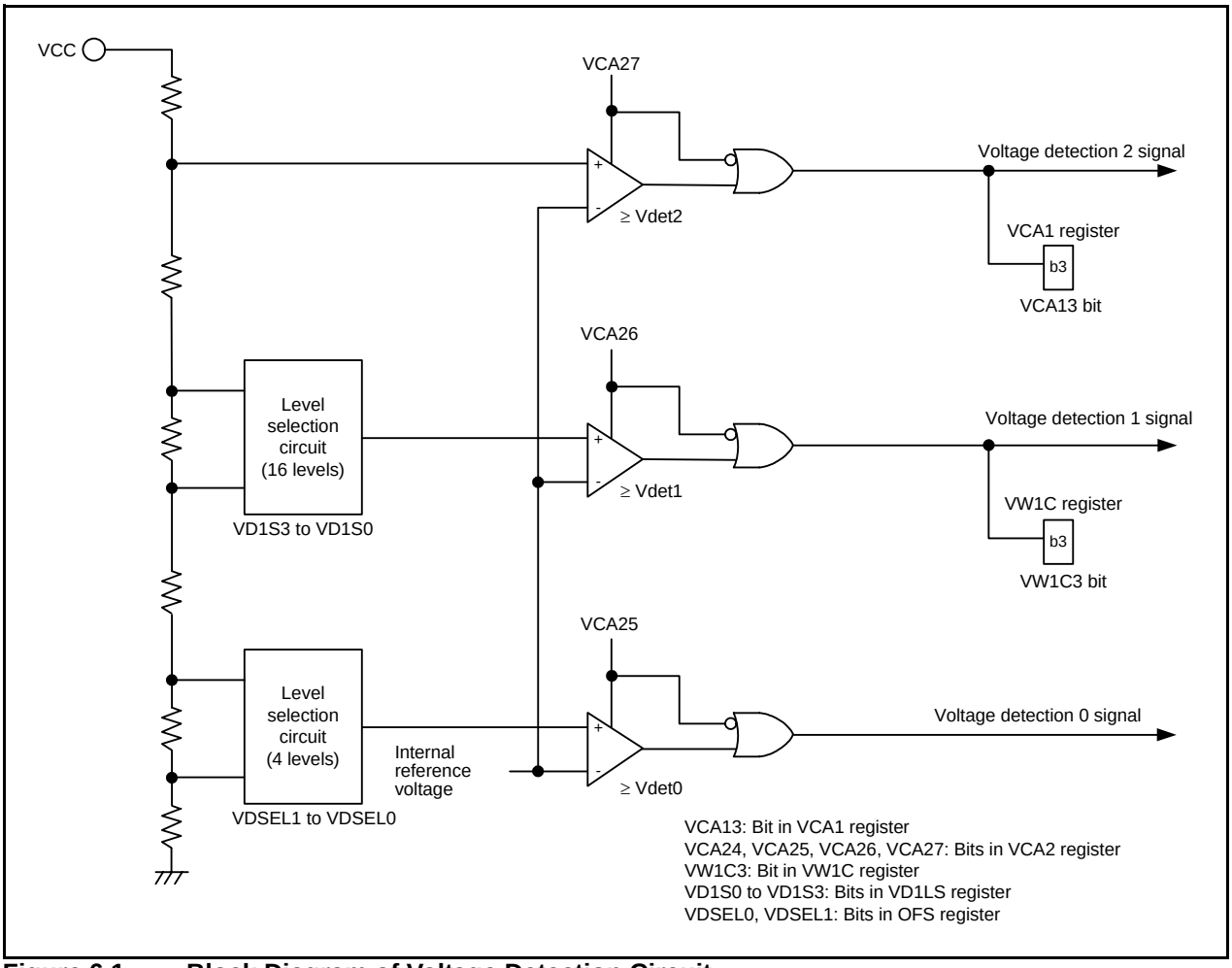


Figure 6.1 Block Diagram of Voltage Detection Circuit

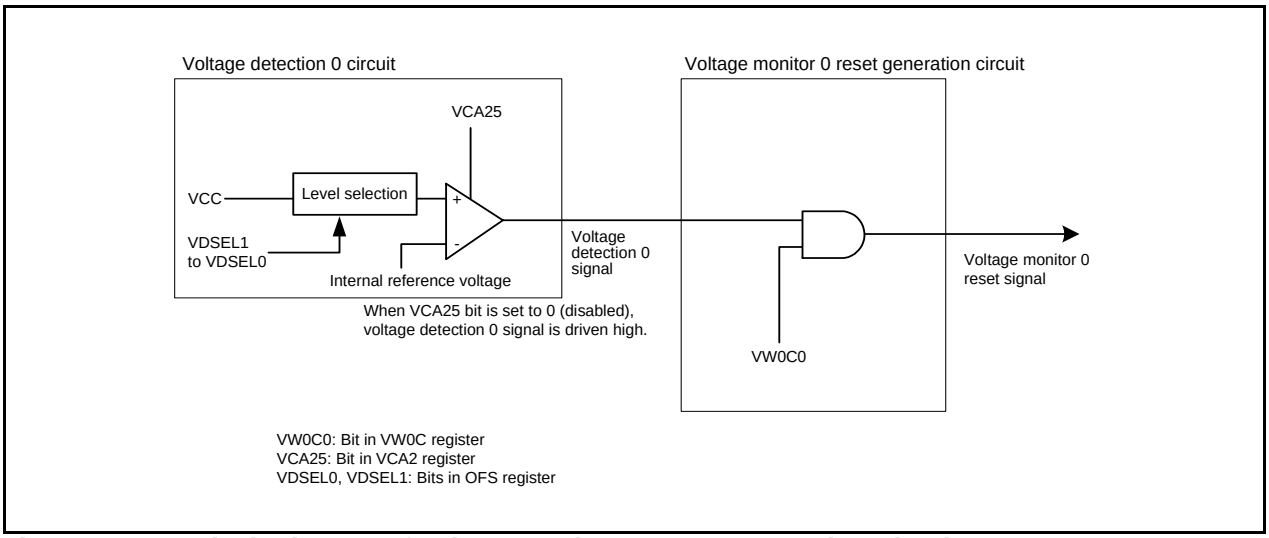


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

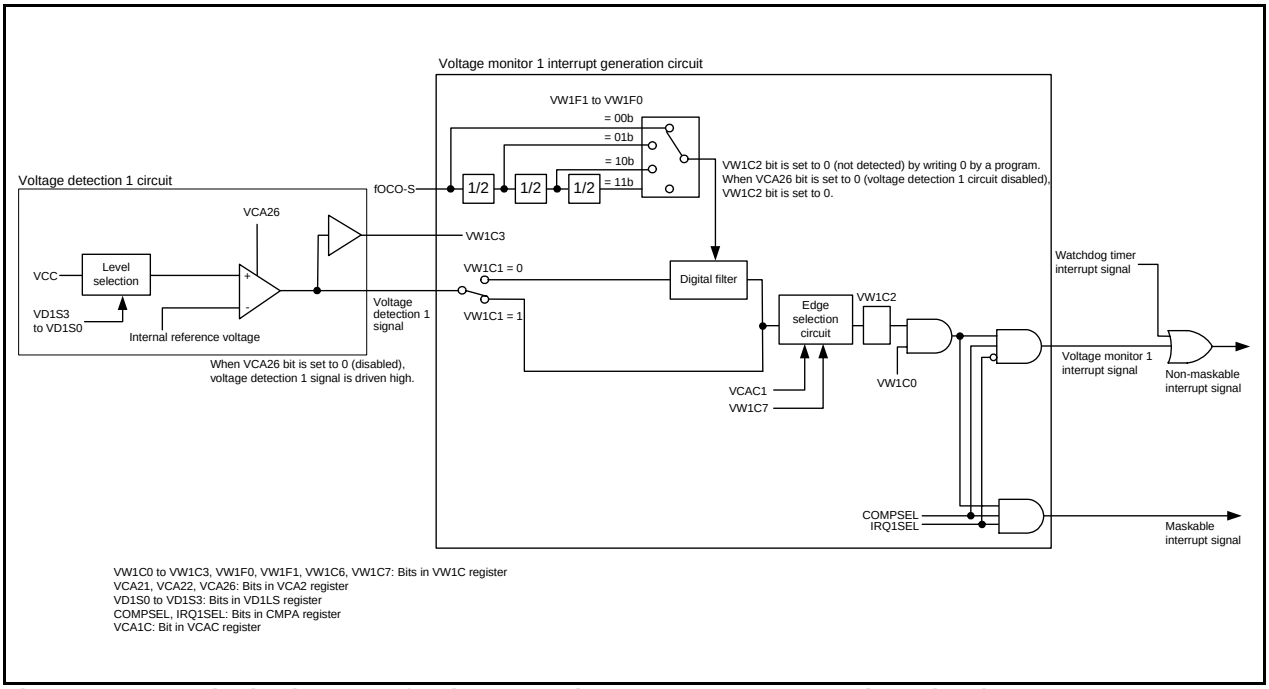


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt Generation Circuit

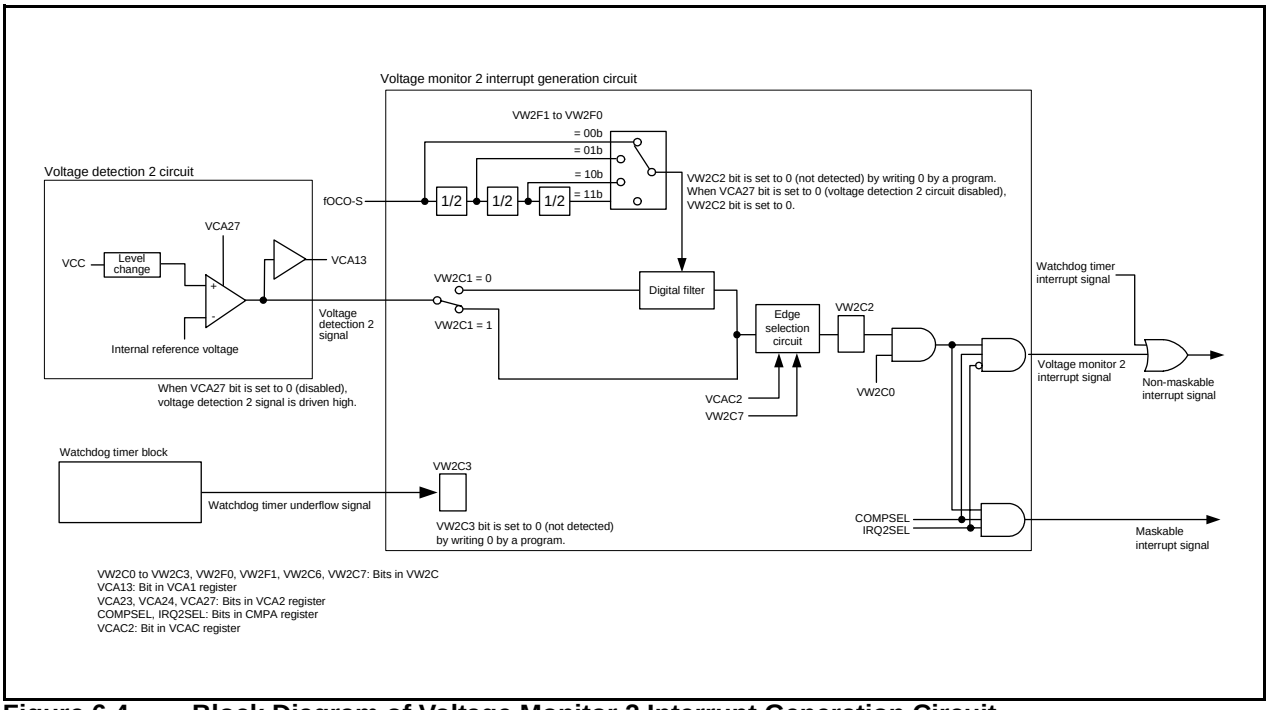


Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt Generation Circuit

6.2 Registers

6.2.1 Voltage Monitor Circuit Control Register (CMPA)

Address 0030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMPSEL	—	IRQ2SEL	IRQ1SEL	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	IRQ1SEL	Voltage monitor 1 interrupt type select bit (1)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	IRQ2SEL	Voltage monitor 2 interrupt type select bit (2)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	COMPSEL	Voltage monitor interrupt type selection enable bit (1, 2)	0: Bits IRQ1SEL and IRQ2SEL disabled 1: Bits IRQ1SEL and IRQ2SEL enabled	R/W

Notes:
1. When the VW1C0 bit in the VW1C register is set to 1 (enabled), do not set bits IRQ1SEL and COMPSEL simultaneously (with one instruction).
2. When the VW2C0 bit in the VW2C register is set to 1 (enabled), do not set bits IRQ2SEL and COMPSEL simultaneously (with one instruction).

6.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	VCAC2	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One edge 1: Both edges	R/W
b2	VCAC2	Voltage monitor 2 circuit edge select bit (2)	0: One edge 1: Both edges	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. When the VCAC1 bit is set to 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. When the VCAC2 bit is set to 0 (one edge), the VW2C7 bit in the VW2C register is enabled. Set the VW2C7 bit after setting the VCAC2 bit to 0.

6.2.3 Voltage Detect Register 1 (VCA1)

Address 0033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VCA13	—	—	—
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	VCA13	Voltage detection 2 signal monitor flag (1)	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. When the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled), the VCA13 bit is enabled.
   When the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled), the VCA13 bit is set to 1 (VCC ≥ Vdet2).

6.2.4 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.7 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1.
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

6.2.5 Voltage Detection 1 Level Select Register (VD1LS)

Address 0036h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	VD1S0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VD1S0	Voltage detection 1 level select bit (Reference voltage when the voltage falls)	b3 b2 b1 b0 0 0 0 0: 2.20 V (Vdet1_0) 0 0 0 1: 2.35 V (Vdet1_1) 0 0 1 0: 2.50 V (Vdet1_2) 0 0 1 1: 2.65 V (Vdet1_3) 0 1 0 0: 2.80 V (Vdet1_4) 0 1 0 1: 2.95 V (Vdet1_5) 0 1 1 0: 3.10 V (Vdet1_6) 0 1 1 1: 3.25 V (Vdet1_7) 1 0 0 0: 3.40 V (Vdet1_8) 1 0 0 1: 3.55 V (Vdet1_9) 1 0 1 0: 3.70 V (Vdet1_A) 1 0 1 1: 3.85 V (Vdet1_B) 1 1 0 0: 4.00 V (Vdet1_C) 1 1 0 1: 4.15 V (Vdet1_D) 1 1 1 0: 4.30 V (Vdet1_E) 1 1 1 1: 4.45 V (Vdet1_F)	R/W
b1	VD1S1			R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

6.2.6 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	VW0C0
After Reset	1	1	0	0	X	0	1	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	1	1	0	0	X	0	1	1

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	When read, the content is undefined.	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—	Reserved bits	Set to 1.	R/W
b7	—			

Note:
1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled). When writing to the VW0C0 bit, set a value after reset.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW0C register.

6.2.7 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter disable mode select bit (2, 6)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet1 passing detected	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit (5)	0: When VCC reaches Vdet1 or above. 1: When VCC reaches Vdet1 or below.	R/W

Notes:

1. The VW1C0 bit is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled). To set the VW0C0 bit to 1 (enabled), follow the procedure shown in **Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When using the digital filter (while the VW1C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled).
4. Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.
6. When the VW1C0 bit is set to 1 (enabled), do not set the VW1C1 bit and bits VW1F1 and VW1F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW1C register.
Rewriting the VW1C register may set the VW1C2 bit to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.

6.2.8 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	—	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Voltage monitor 2 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW2C1	Voltage monitor 2 digital filter disable mode select bit (2, 6)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW2C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet2 passing detected	R/W
b3	VW2C3	WDT detection monitor flag (4)	0: Not detected 1: Detected	R/W
b4	VW2F0	Sampling clock select bit (6)	b5 b4	R/W
b5	VW2F1		0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW2C7	Voltage monitor 2 interrupt generation condition select bit (5)	0: When VCC reaches Vdet2 or above. 1: When VCC reaches Vdet2 or below.	R/W

Notes:

1. The VW2C0 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled). To set the VW2C0 bit to 1 (enabled), follow the procedure shown in **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**.
2. When using the digital filter (while the VW2C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). After setting the VCAC2 bit to 0, set the VW2C7 bit.
6. When the VW2C0 bit is set to 1 (enabled), do not set the VW2C1 bit and bits VW2F1 and VW2F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
Rewriting the VW2C register may set the VW2C2 bit to 1. After rewriting this register, set the VW2C2 bit to 0.

6.2.9 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

6.3 VCC Input Voltage

6.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.3.2 Monitoring Vdet1

Once the following settings are made, the comparison result of voltage monitor 1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **30. Electrical Characteristics**).

(1) Set bits VD1S3 to VD1S0 in the VD1LS register (voltage detection 1 detection voltage).
(2) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

6.3.3 Monitoring Vdet2

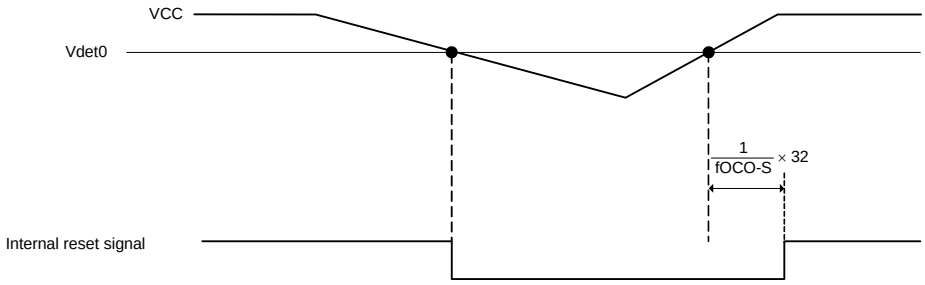
Once the following settings are made, the comparison result of voltage monitor 2 can be monitored by the VCA13 bit in the VCA1 register after td(E-A) has elapsed (refer to **30. Electrical Characteristics**).

- Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).

6.4 Voltage Monitor 0 Reset

To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset).

Figure 6.5 shows an Operating Example of Voltage Monitor 0 Reset.



When the internal reset signal is driven low, the pins, CPU, and SFRs are initialized.
When the internal reset signal level changes from low to high, a program is executed beginning with the address indicated by the reset vector.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after reset.

Figure 6.5 Operating Example of Voltage Monitor 0 Reset

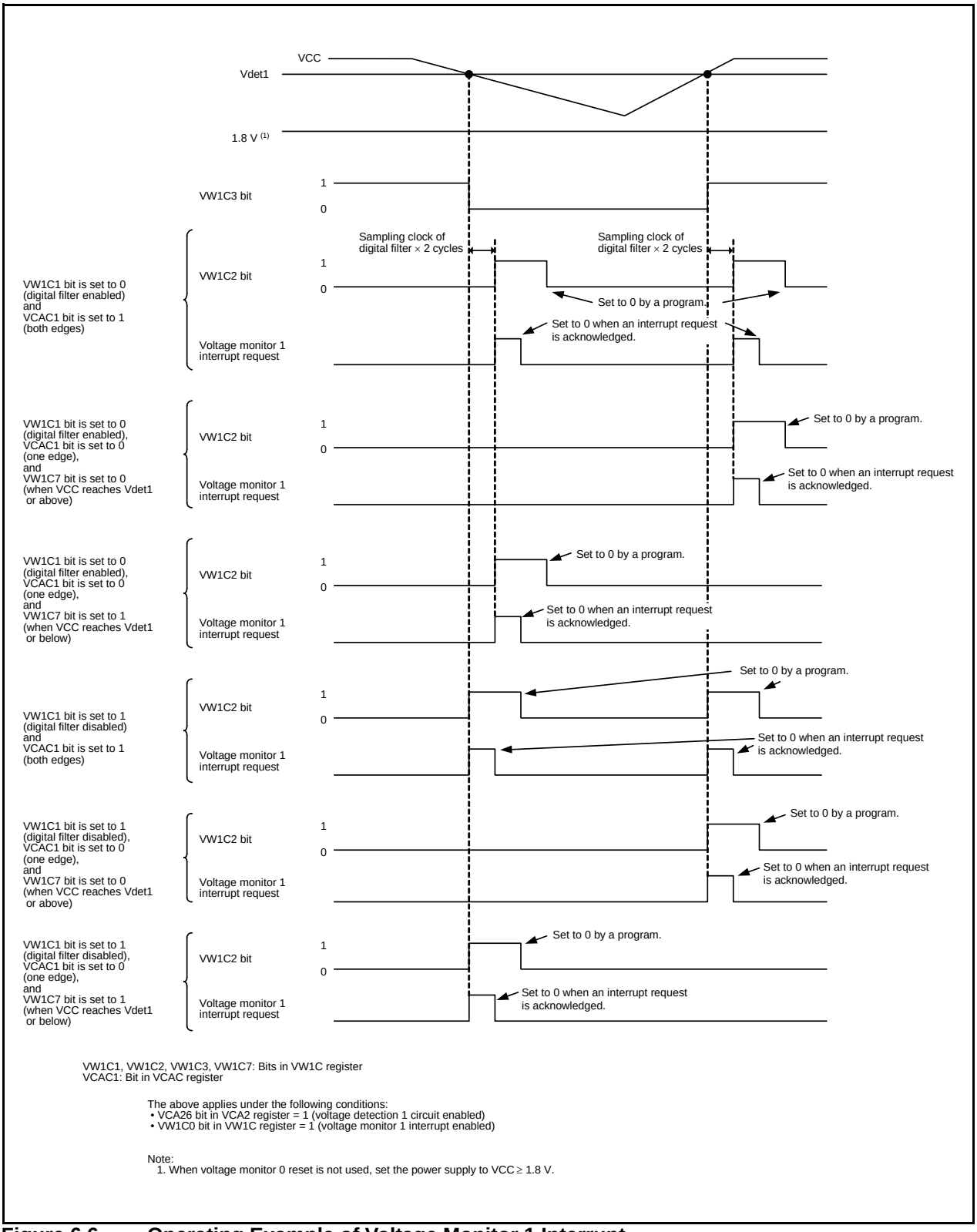
6.5 Voltage Monitor 1 Interrupt

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 6.6 shows an Operating Example of Voltage Monitor 1 Interrupt.
To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Select the voltage detection 1 detection voltage by bits VD1S3 to VD1S0 in the VD1LS register.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td (E-A).	
4	Set the COMPSEL bit in the CMPA register to 1.	
5 (1)	Select the interrupt type by the IRQ1SEL bit in the CMPA register.	
6	Select the sampling clock of the digital filter by bits VW1F1 to VW1F0 in the VW1C register.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
7 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	—
8	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register.	
9	Set the VW1C2 bit in the VW1C register to 0.	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	—
11	Wait for 2 cycles of the sampling clock of the digital filter	— (No wait time required)
12 (3)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled)	

Notes:
1. When the VW1C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with one instruction).
2. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed simultaneously (with one instruction).
3. When the voltage detection 1 circuit is enabled while the voltage monitor 1 interrupt is disabled, low voltage is detected and the VW1C2 bit becomes 1.
   When low voltage is detected after the voltage detection 1 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 1 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW1C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.


VCC
Vdet1
1.8 V (1)
VW1C3 bit
1
0
Sampling clock of digital filter × 2 cycles
Sampling clock of digital filter × 2 cycles
VW1C1 bit is set to 0 (digital filter enabled) and VCAC1 bit is set to 1 (both edges)
VW1C2 bit
Voltage monitor 1 interrupt request
Set to 0 by a program.
Set to 0 when an interrupt request is acknowledged.
VW1C1 bit is set to 0 (digital filter enabled), VCAC1 bit is set to 0 (one edge), and VW1C7 bit is set to 0 (when VCC reaches Vdet1 or above)
VW1C1 bit is set to 0 (digital filter enabled), VCAC1 bit is set to 0 (one edge), and VW1C7 bit is set to 1 (when VCC reaches Vdet1 or below)
VW1C1 bit is set to 1 (digital filter disabled) and VCAC1 bit is set to 1 (both edges)
VW1C1 bit is set to 1 (digital filter disabled), VCAC1 bit is set to 0 (one edge), and VW1C7 bit is set to 0 (when VCC reaches Vdet1 or above)
VW1C1 bit is set to 1 (digital filter disabled), VCAC1 bit is set to 0 (one edge), and VW1C7 bit is set to 1 (when VCC reaches Vdet1 or below)

VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above applies under the following conditions:
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt enabled)

Note:
1. When voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.6 Operating Example of Voltage Monitor 1 Interrupt

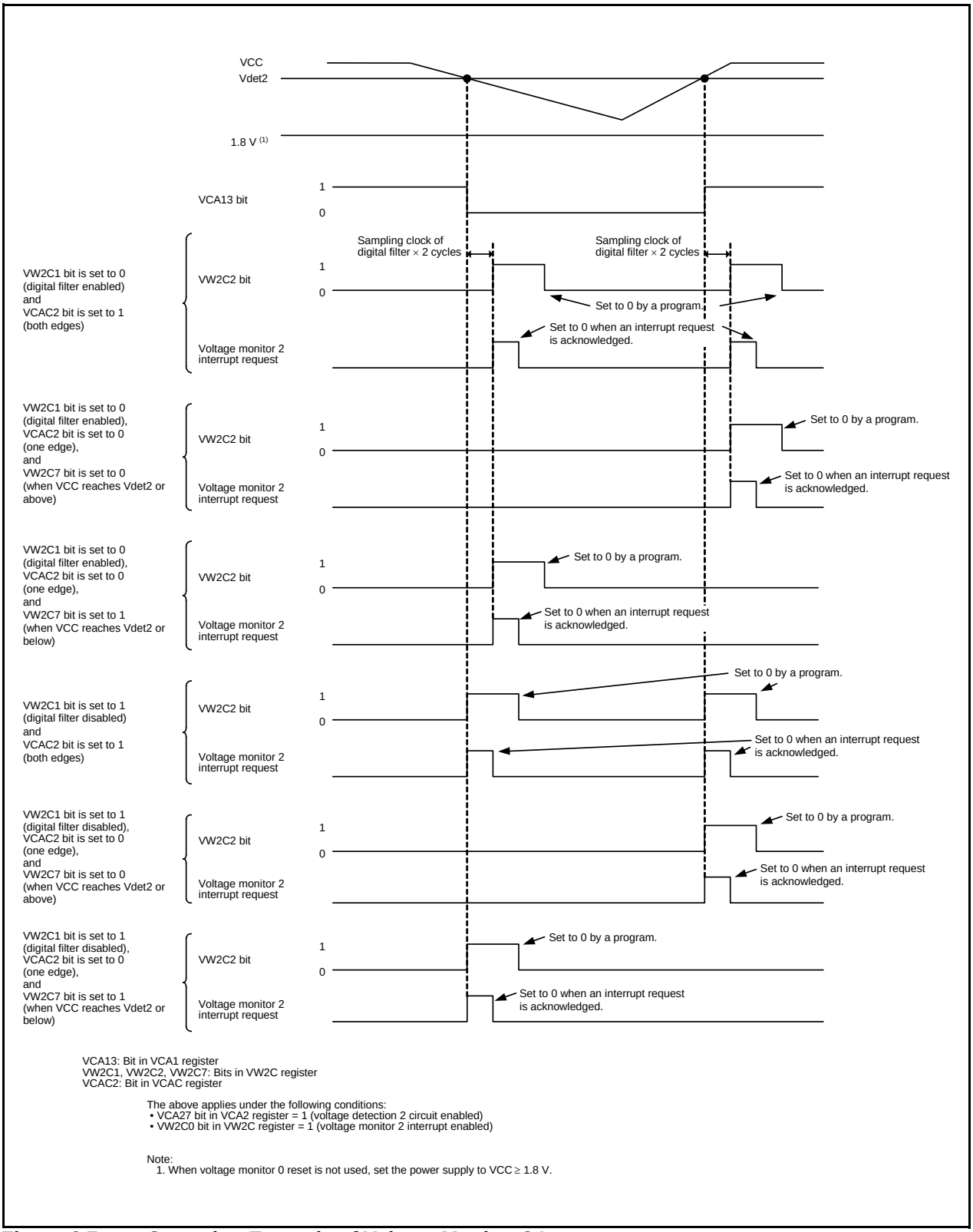
6.6 Voltage Monitor 2 Interrupt

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt. Figure 6.7 shows an Operating Example of Voltage Monitor 2 Interrupt.
To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
2	Wait for td(E-A).	
3	Set the COMPSEL bit in the CMPA register to 1.	
4 (1)	Select the interrupt type by the IRQ2SEL bit in the CMPA register.	
5	Select the sampling clock of the digital filter by bits VW2F0 to VW2F1 in the VW2C register.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
6 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	—
7	Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register.	
8	Set the VW2C2 bit in the VW2C register to 0.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	—
10	Wait for 2 cycles of the sampling clock of the digital filter.	— (No wait time required)
11 (3)	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is set to 0, steps 3 and 4 can be executed simultaneously (with one instruction).
2. When the VW2C0 bit is set to 0, steps 5 and 6 can be executed simultaneously (with one instruction).
3. When the voltage detection 2 circuit is enabled while the voltage monitor 2 interrupt is disabled, low voltage is detected and the VW2C2 bit becomes 1.
   When low voltage is detected after the voltage detection 2 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 2 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW2C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.


VCC
Vdet2
1.8 V (1)
VCA13 bit
1
0
Sampling clock of digital filter × 2 cycles
Sampling clock of digital filter × 2 cycles
VW2C1 bit is set to 0 (digital filter enabled) and VCAC2 bit is set to 1 (both edges)
VW2C2 bit
Voltage monitor 2 interrupt request
Set to 0 by a program.
Set to 0 when an interrupt request is acknowledged.
VW2C1 bit is set to 0 (digital filter enabled), VCAC2 bit is set to 0 (one edge), and VW2C7 bit is set to 0 (when VCC reaches Vdet2 or above)
VW2C1 bit is set to 0 (digital filter enabled), VCAC2 bit is set to 0 (one edge), and VW2C7 bit is set to 1 (when VCC reaches Vdet2 or below)
VW2C1 bit is set to 1 (digital filter disabled) and VCAC2 bit is set to 1 (both edges)
VW2C1 bit is set to 1 (digital filter disabled), VCAC2 bit is set to 0 (one edge), and VW2C7 bit is set to 0 (when VCC reaches Vdet2 or above)
VW2C1 bit is set to 1 (digital filter disabled), VCAC2 bit is set to 0 (one edge), and VW2C7 bit is set to 1 (when VCC reaches Vdet2 or below)

VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register

The above applies under the following conditions:
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage monitor 2 interrupt enabled)

Note:
1. When voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.7 Operating Example of Voltage Monitor 2 Interrupt

7. I/O Ports

Note

The description offered in this chapter is based on the R8C/LA8A Group.
For other groups, refer to 1.1.2 Differences between Groups.

7.1 Introduction

I/O ports are shared with the LCD ports for the LCD dive control waveform output and the I/O functions for the oscillation circuits, timers, and A/D converter. When these functions are not used, pins can be used as I/O ports. Table 7.1 lists the Overview of I/O Ports.

Table 7.1 Overview of I/O Ports

Port	I/O Format	I/O Setting	Internal Pull-Up Resister (1)	Drive Capacity Switch (2)	Input Level Switch (3)
P0 to P4	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 8-bit units.
P5_0 to P5_3	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 7-bit units.
P5_4 to P5_6	I/O CMOS3 state	Set in 1-bit units.	None	None	
P6	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 8-bit units.
P7_0 to P7_1	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	Set in 1-bit units.	Set in 8-bit units.
P7_2 to P7_6	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	
P8	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	Set in 1-bit units.	Set in 8-bit units.
P9_0 to P9_1	I/O CMOS3 state	Set in 1-bit units.	Set in 1-bit units.	None	Set in 2-bit units.

Notes:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers P0PUR to and P9PUR.
2. Whether the drive capacity of the output transistor is set to low or high can be selected by registers P7DRR and P8DRR.
3. The input threshold value can be selected among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) using registers VLT0 and VLT1.

Table 7.2 Programmable I/O Ports Provided for Each Group

Programmable I/O Port	R8C/LA6A Group Total: 56 I/O pins								R8C/LA8A Group Total: 72 I/O pins							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P1	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P4	✓	✓	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P6	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:
1. The symbol "✓" indicates a programmable I/O port.
2. The symbol "—" indicates the settings should be made as follows:
   - Set 1 to the corresponding PDi (i = 0 to 9) register. When read, the content is 1.
   - Set 0 to the corresponding Pi (i = 0 to 9) register. When read, the content is 0.
   - Set 0 to the corresponding P7DRR or P8DRR register. When read, the content is 0.

7.2 I/O Port Functions

The PDi_j (j = 0 to 7) bit in the PDi (i = 0 to 9) register controls the input/output of ports P0 to P9. The Pi register consists of a port latch to retain output data and a circuit to read the pin status.
Figures 7.1 to 7.4 show the I/O Port Configurations, and Table 7.3 lists the I/O Port Functions.

Table 7.3 I/O Port Functions

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register (1)	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Read	Read the pin input level.	Read the port latch.
Write	Write to the port latch.	Write to the port latch. The value written to the port latch is output from the pin.

Note:
1. i = 0 to 9; j = 0 to 7

7.3 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (refer to **Tables 1.9 to 1.11 Pin Name Information by Pin Number**).
Table 7.4 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 9; j = 0 to 7). Refer to the description of each function for information on how to set peripheral functions.

Table 7.4 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 9; j = 0 to 7)

I/O of Peripheral Function	PDi_j Bit Settings for Shared Pin Function
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting).

7.4 Pins Other than I/O Ports

Figure 7.6 shows the Pin Configuration.

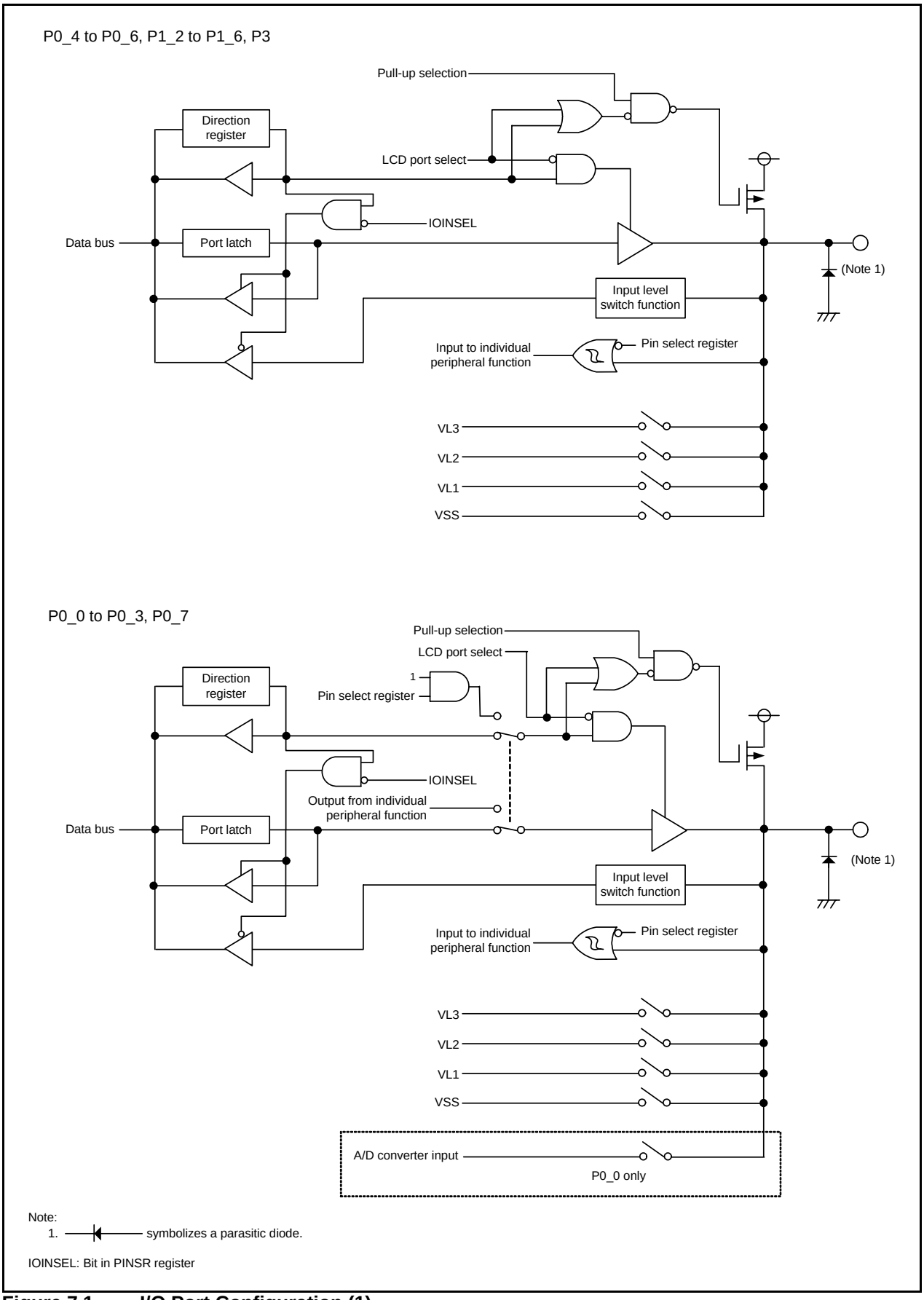


Figure 7.1 I/O Port Configuration (1)

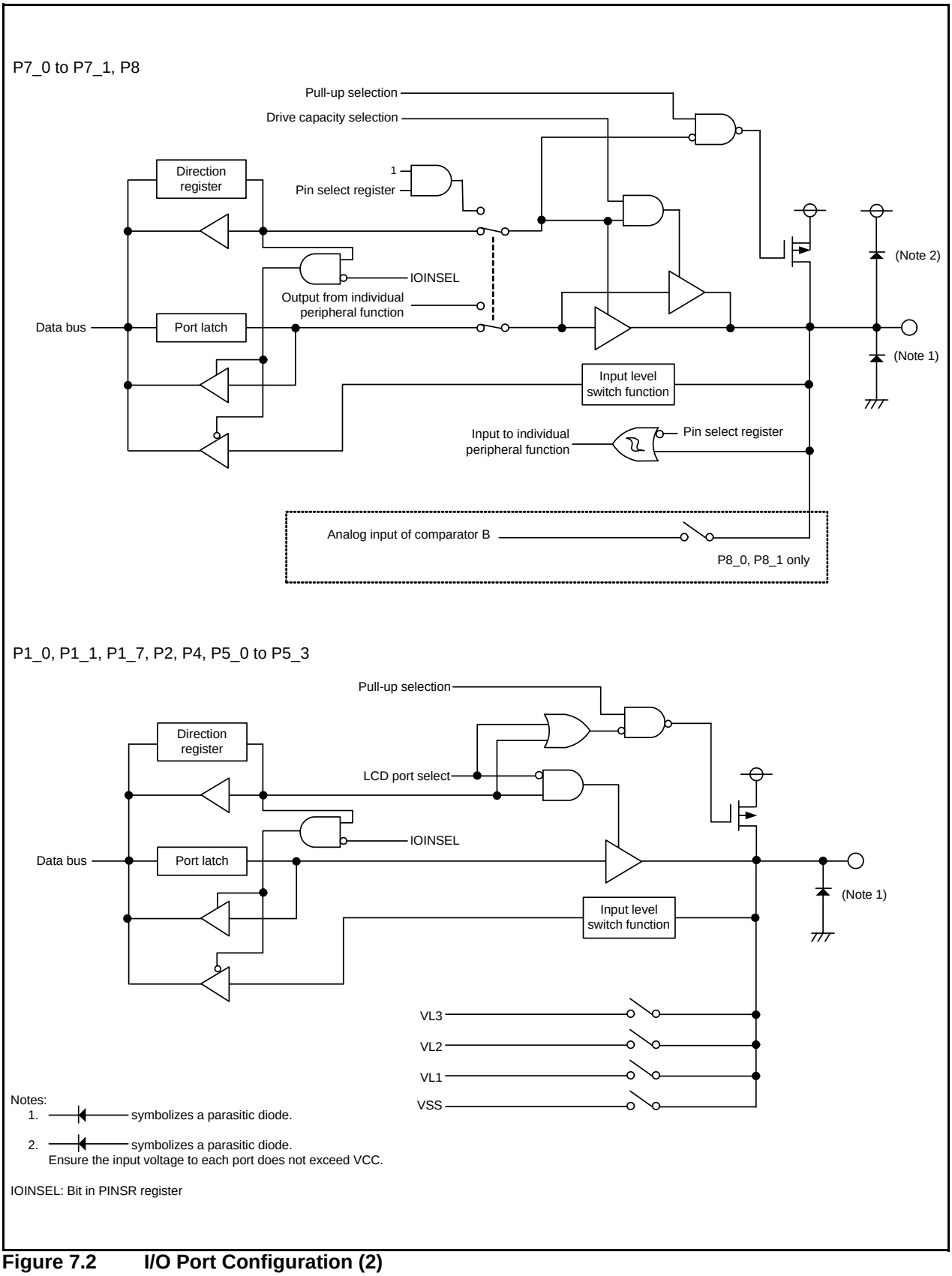


Figure 7.2 I/O Port Configuration (2)

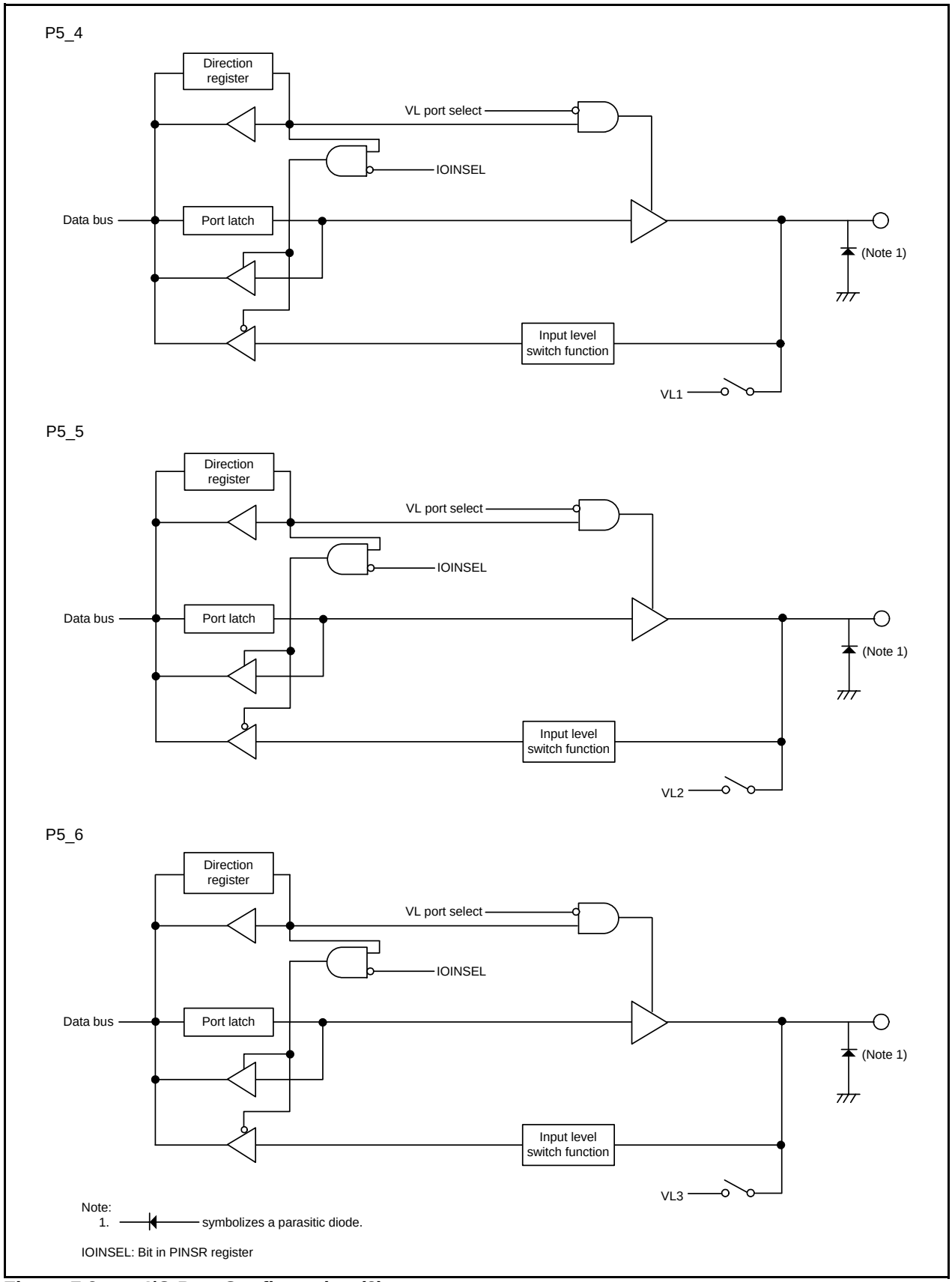


Figure 7.3 I/O Port Configuration (3)

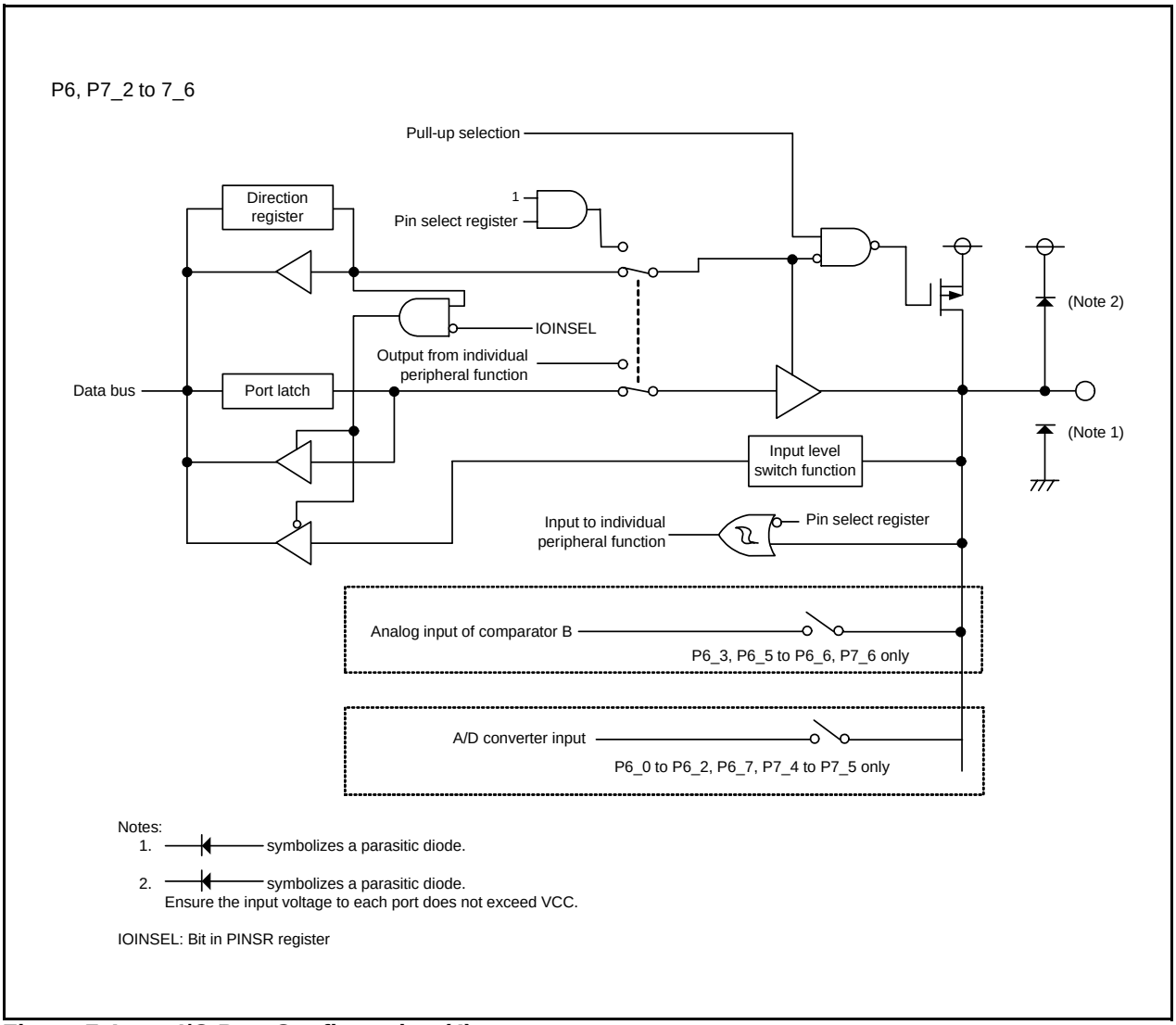


Figure 7.4 I/O Port Configuration (4)

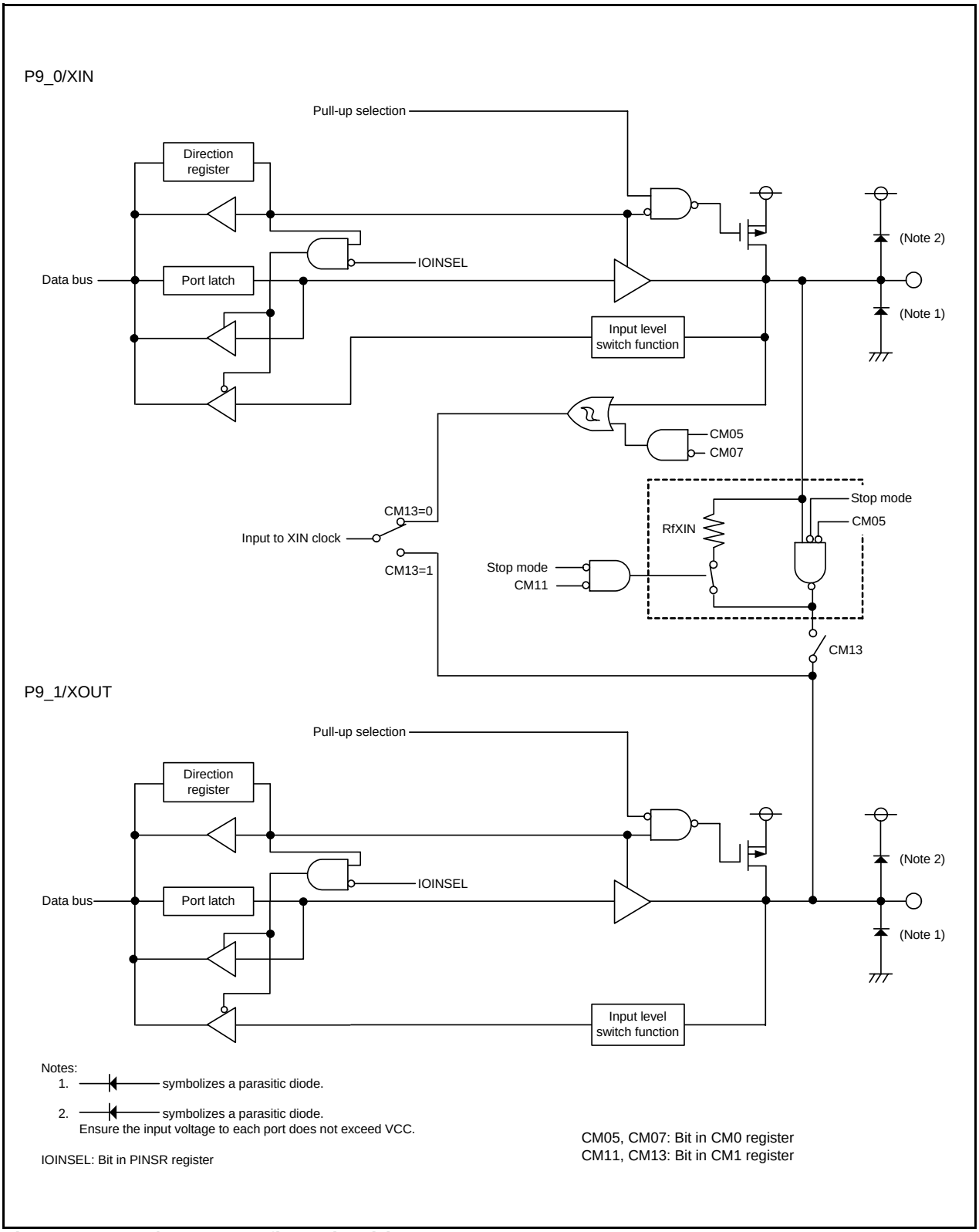


Figure 7.5 I/O Port Configuration (5)

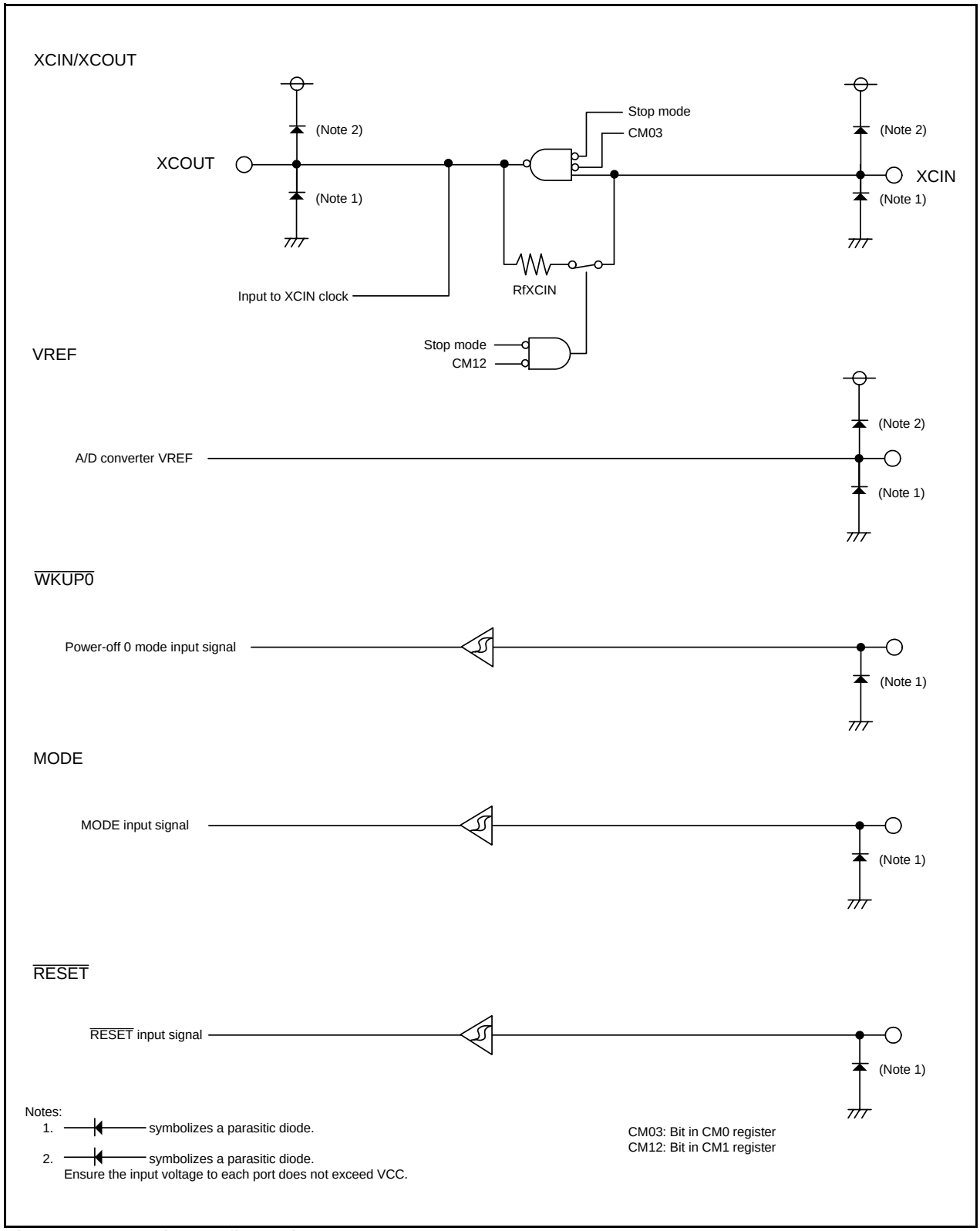


Figure 7.6 Pin Configuration

7.5 Registers

7.5.1 Port Pi Direction Register (PDi) (i = 0 to 9)

Address 00E2h (PD0), 00E3h (PD1), 00E6h (PD2), 00E7h (PD3),
00EAh (PD4), 00EBh (PD5 (1)), 00EEh (PD6), 00EFh (PD7(2)),
00F2h (PD8), 00F3h (PD9(3))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PDi_7	PDi_6	PDi_5	PDi_4	PDi_3	PDi_2	PDi_1	PDi_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDi_0	Port Pi_0 direction bit	0: Input mode (function as an input port) 1: Output mode (function as an output port)	R/W
b1	PDi_1	Port Pi_1 direction bit		R/W
b2	PDi_2	Port Pi_2 direction bit		R/W
b3	PDi_3	Port Pi_3 direction bit		R/W
b4	PDi_4	Port Pi_4 direction bit		R/W
b5	PDi_5	Port Pi_5 direction bit		R/W
b6	PDi_6	Port Pi_6 direction bit		R/W
b7	PDi_7	Port Pi_7 direction bit		R/W

Notes:
1. PD5_7 bit in the PD5 register are unavailable on this MCU.
   Set PD5_7 bit to 1. When read, the content is 1.
2. PD7_7 bit in the PD7 register are unavailable on this MCU.
   Set PD7_7 bit to 1. When read, the content is 1.
3. Bits PD9_2 to PD9_7 in the PD9 register are unavailable on this MCU.
   Set bits PD9_2 to PD9_7 to 1. When read, the content is 1.

The PDi register selects whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.
To use the peripheral function as output, set the direction register to 1 (output mode).

7.5.2 Port Pi Register (Pi) (i = 0 to 9)

Address 00E0h (P0), 00E1h (P1), 00E4h (P2), 00E5h (P3),
00E8h (P4), 00E9h (P5 (1)), 00ECh(P6), 00EDh (P7(2)),
00F0h (P8), 00F1h (P9(3))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	Pi_0	Port Pi_0 bit	0: Low level 1: High level	R/W
b1	Pi_1	Port Pi_1 bit		R/W
b2	Pi_2	Port Pi_2 bit		R/W
b3	Pi_3	Port Pi_3 bit		R/W
b4	Pi_4	Port Pi_4 bit		R/W
b5	Pi_5	Port Pi_5 bit		R/W
b6	Pi_6	Port Pi_6 bit		R/W
b7	Pi_7	Port Pi_7 bit		R/W

Notes:
1. P5_7 bit in the P5 register are unavailable on this MCU.
   Set P5_7 bit to 0. When read, the content is 0.
2. P7_7 bit in the P7 register are unavailable on this MCU.
   Set P7_7 bit to 0. When read, the content is 0.
3. Bits P9_2 to P9_7 in the P9 register are unavailable on this MCU.
   Set bits P9_2 to P9_7 to 0. When read, the content is 0.

Data input and output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to retain output data and a circuit to read the pin status. The value written in the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

Pi_j Bit (i = 0 to 9, j = 0 to 7) (Port Pi_0 Bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.

7.5.3 Timer RJ Pin Select Register (TRJSR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRJ1IOSEL1	TRJ1IOSEL0	—	—	TRJ0IOSEL1	TRJ0IOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJ0IOSEL0	TRJ0IO pin select bit	b1 b0 0 0: TRJ0IO pin not used 0 1: P6_2 assigned 1 0: P8_3 assigned 1 1: Do not set.	R/W
b1	TRJ0IOSEL1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	TRJ1IOSEL0	TRJ1IO pin select bit	b5 b4 0 0: TRJ1IO pin not used 0 1: P6_1 assigned 1 0: P8_2 assigned 1 1: Do not set.	R/W
b5	TRJ1IOSEL1			R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

To use the I/O pins for timer RJi, set the TRJSR register.
Set this register before setting the timer RJi associated registers. Also, do not change the setting value of this register during timer RJi operation.

7.5.4 Timer RB Pin Select Register (TRBSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRB1OSEL1	TRB1OSEL0	TRB0OSEL1	TRB0OSEL0	—	—	TRJ2IOSEL1	TRJ2IOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJ2IOSEL0	TRJ2IO pin select bit	b1 b0 0 0: TRJ2IO pin not used 0 1: P6_0 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b1	TRJ2IOSEL1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	TRB0OSEL0	TRB0O pin select bit	b5 b4 0 0: P8_7 assigned 0 1: P7_6 assigned 1 0: P6_6 assigned 1 1: Do not set.	R/W
b5	TRB0OSEL1			R/W
b6	TRB1OSEL0	TRB1O pin select bit	b7 b6 0 0: P7_5 assigned 0 1: P6_5 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b7	TRB1OSEL1			R/W

To use the output pins for timer RJi, set the TRBSR register.
Set this register before setting the timer RJi associated registers. Also, do not change the setting value of this register during timer RJi operation.

7.5.5 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	TRCIOASEL1	TRCIOASEL0	—	TRCCLKSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCCLKSEL0	TRCCLK pin select bit (1)	0: TRCCLK pin not used 1: P0_1 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b3 b2 0 0: TRCIOA/TRCTRG pin not used 0 1: TRCIOA/TRCTRG pin assigned to P0_0 1 0: TRCTRG pin assigned to P0_1 (1) 1 1: TRCTRG pin assigned to P0_2	R/W
b3	TRCIOASEL1			R/W
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P6_7 assigned 1 0: P6_6 assigned (2) 1 1: P6_5 assigned (3)	R/W
b5	TRCIOBSEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Pins TRCCLK and TRCTRG cannot be assigned to P0_1 at the same time.
2. When the TRCIOCSEL0 bit in the TRCPSR1 register is set to 1 (TRCIOC pin assigned to P6_6), P6_6 functions as the TRCIOC pin regardless of the content of bits TRCIOBSEL1 to TRCIOBSEL0.
3. When the TRCIODSEL0 bit in the TRCPSR1 register is set to 1 (TRCIOD pin assigned to P6_5), P6_5 functions as the TRCIOD pin regardless of the content of bits TRCIOBSEL1 to TRCIOBSEL0.

The TRCPSR0 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation. If the assignment of the timer RC pins is changed, an edge may occur depending on the changed pin level, causing the TRC register to be set to 0000h.

7.5.6 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TRCIODSEL0	—	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	0: TRCIOC pin not used 1: P6_6 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRCIODSEL0	TRCIOD pin select bit	0: TRCIOD pin not used 1: P6_5 assigned	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

The TRCPSR1 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

7.5.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK0SEL1	CLK0SEL0	RXD0SEL1	RXD0SEL0	TXD0SEL1	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	b1 b0 0 0: TXD0 pin not used 0 1: P8_5 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b1	TXD0SEL1			R/W
b2	RXD0SEL0	RXD0 pin select bit	b3 b2 0 0: RXD0 pin not used 0 1: P8_6 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b3	RXD0SEL1			R/W
b4	CLK0SEL0	CLK0 pin select bit	b5 b4 0 0: CLK0 pin not used 0 1: P8_4 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b5	CLK0SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		R/W
b7	—			R/W

The U0SR register selects which pin is assigned as the UART0 input/output. To use the I/O pins for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value of this register during UART0 operation.

7.5.8 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RXD2SEL1	RXD2SEL0	—	—	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2/SDA2 pin select bit	b1 b0 0 0: TXD2/SDA2 pin not used 0 1: P7_1 assigned 1 0: P7_2 assigned 1 1: P8_5 assigned	R/W
b1	TXD2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	RXD2SEL0	RXD2/SCL2 pin select bit	b5 b4 0 0: RXD2/SCL2 pin not used 0 1: P7_2 assigned 1 0: P7_1 assigned 1 1: P8_6 assigned	R/W
b5	RXD2SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR0 register selects which pin is assigned as the UART2 input/output. To use the I/O pins for UART2, set this register.
Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value of this register during UART2 operation.

7.5.9 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CTS2SEL1	CTS2SEL0	—	—	CLK2SEL1	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bit	b1 b0 0 0: CLK2 pin not used 0 1: P7_0 assigned 1 0: P8_4 assigned 1 1: Do not set.	R/W
b1	CLK2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	CTS2SEL0	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin select bit	b5 b4 0 0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin not used 0 1: P7_3 assigned 1 0: P8_7 assigned 1 1: Do not set.	R/W
b5	CTS2SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR1 register selects which pin is assigned as the UART2 input/output. To use the I/O pins for UART2, set this register.
Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value of this register during UART2 operation.

7.5.10 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SSOSEL0	SCSSEL0	SSCKSEL0	SSISEL0	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit	0: SSU function selected 1: I2C bus function selected	R/W
b1	—	Reserved bits	Set to 0.	—
b2	—			
b3	—			
b4	SSISEL0	SSI pin select bit	0: P8_1 assigned 1: P6_2 assigned	R/W
b5	SSCKSEL0	SSCK/SCL pin select bit	0: P8_2 assigned 1: P6_3 assigned	R/W
b6	SCSSEL0	SCS pin select bit	0: P8_0 assigned 1: P6_1 assigned	R/W
b7	SSOSEL0	SSO/SDA pin select bit	0: P8_3 assigned 1: P6_4 assigned	R/W

7.5.11 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7SEL0	INT6SEL0	INT5SEL0	INT4SEL0	INT3SEL0	INT2SEL0	INT1SEL0	INT0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0SEL0	$\overline{\text{INT0}}$ pin select bit	0: P0_3 assigned 1: P3_0 assigned	R/W
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	0: P8_0 assigned 1: P3_1 assigned	R/W
b2	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	0: P8_7 assigned 1: P3_2 assigned	R/W
b3	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	0: P8_1 assigned 1: P3_3 assigned	R/W
b4	INT4SEL0	$\overline{\text{INT4}}$ pin select bit	0: P1_4 assigned 1: P3_4 assigned	R/W
b5	INT5SEL0	$\overline{\text{INT5}}$ pin select bit	0: P1_5 assigned 1: P3_5 assigned	R/W
b6	INT6SEL0	$\overline{\text{INT6}}$ pin select bit	0: P1_6 assigned 1: P3_6 assigned	R/W
b7	INT7SEL0	$\overline{\text{INT7}}$ pin select bit	0: P0_1 assigned 1: P3_7 assigned	R/W

The INTSR register selects which pin is assigned as the $\overline{\text{INTi}}$ (i = 0 to 7) input. To use the $\overline{\text{INTi}}$, set this register. Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

7.5.12 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0 to 9) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register.	R/W
b4	IICTCTWI	I^2C double transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I^2C half transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

7.5.13 Port Pi Pull-Up Control Register (PiPUR) (i = 0 to 9)

Address 01E0h (P0PUR), 01E1h (P1PUR), 01E2h (P2PUR), 01E3h (P3PUR), 01E4h (P4PUR), 01E5h (P5PUR(2)), 01E6h (P6PUR), 01E7h (P7PUR(3)) 01E8h (P8PUR), 01E9h (P9PUR(4))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PUi7	PUi6	PUi5	PUi4	PUi3	PUi2	PUi1	PUi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PUi0	Port Pi_0 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b1	PUi1	Port Pi_1 pull-up		R/W
b2	PUi2	Port Pi_2 pull-up		R/W
b3	PUi3	Port Pi_3 pull-up		R/W
b4	PUi4	Port Pi_4 pull-up		R/W
b5	PUi5	Port Pi_5 pull-up		R/W
b6	PUi6	Port Pi_6 pull-up		R/W
b7	PUi7	Port Pi_7 pull-up		R/W

Notes:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.
2. Bits PU54 to PU57 in the P5PUR register is reserved. When read, the content is 0.
3. The PU77 bit in the P7PUR register is reserved. When read, the content is 0.
4. Bits PU92 to PU97 in the P9PUR register are unavailable on this MCU.
   Set bits PU92 to PU97 to 0. When read, the content is 0.

For pins used as input, the setting values in the PiPUR register are valid.

7.5.14 Port P7 Drive Capacity Control Register (P7DRR)

Address 01F0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	P7DRR1	P7DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P7DRR0	P7_0 drive capacity	0: Low 1: High (1)	R/W
b1	P7DRR1	P7_1 drive capacity		R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. Both high-level output and low-level output are set to high drive capacity.

The P7DRR register selects whether the drive capacity of the P7 output transistor is set to low or high.
The P7DRRi bit (i = 0 and 1) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.
For pins used as output, the setting values in the P7DRR register are valid.

7.5.15 Port P8 Drive Capacity Control Register (P8DRR)

Address 01F1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P8DRR7	P8DRR6	P8DRR5	P8DRR4	P8DRR3	P8DRR2	P8DRR1	P8DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P8DRR0	P8_0 drive capacity	0: Low 1: High (1)	R/W
b1	P8DRR1	P8_1 drive capacity		R/W
b2	P8DRR2	P8_2 drive capacity		R/W
b3	P8DRR3	P8_3 drive capacity		R/W
b4	P8DRR4	P8_4 drive capacity		R/W
b5	P8DRR5	P8_5 drive capacity		R/W
b6	P8DRR6	P8_6 drive capacity		R/W
b7	P8DRR7	P8_7 drive capacity		R/W

Note:
1. Both high-level output and low-level output are set to high drive capacity.

The P8DRR register selects whether the drive capacity of the P8 output transistor is set to low or high. The P8DRRi bit (i = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.
For pins used as output, the setting values in the P8DRR register are valid.

7.5.16 Input Threshold Control Register 0 (VLT0)

Address 01F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT07	VLT06	VLT05	VLT04	VLT03	VLT02	VLT01	VLT00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT00	P0 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT01			R/W
b2	VLT02	P1 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT03			R/W
b4	VLT04	P2 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT05			R/W
b6	VLT06	P3 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT07			R/W

The VLT0 register selects the voltage level of the input threshold values for ports P0 to P3. Bits VLT00 to VLT07 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.5.17 Input Threshold Control Register 1 (VLT1)

Address 01F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT17	VLT16	VLT15	VLT14	VLT13	VLT12	VLT11	VLT10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT10	P4 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT11			R/W
b2	VLT12	P5 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT13			R/W
b4	VLT14	P6 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT15			R/W
b6	VLT16	P7 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT17			R/W

The VLT1 register selects the voltage level of the input threshold values for ports P4 to P7. Bits VLT10 to VLT17 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.5.18 Input Threshold Control Register 2 (VLT2)

Address 01F7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VLT23	VLT22	VLT21	VLT20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT20	P8 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT21			R/W
b2	VLT22	P9 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT23			R/W
b4	—	Reserved bits	Set to 0.	—
b5	—			
b6	—			
b7	—			

The VLT2 register selects the voltage level of the input threshold values for ports P8 and P9. Bits VLT20 to VLT23 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.6 Port Settings

Tables 7.5 to 7.76 list the port settings.

Table 7.5 Port P0_0

Register		PD0	LSE0	ADINSEL					TRCPSR0		TRC OER	TRC MR	TRCIOR0			TRCCR2		Function
Bit		PD0_0	LSE00	CH			ADG SEL		TRCIOA SEL		EA	PWM 2	IOA			TCEG		
				2	1	0	1	0	1	0			2	1	0	1	0	
Pin	P0_0	0	0	X	X	X	X	X	Other than 01b		X	X	X	X	X	X	X	Input port (1)
		1	0	X	X	X	X	X	Other than 01b		X	X	X	X	X	X	X	Output port
	(SEG0)	X	1	X	X	X	X	X	Other than 01b		X	X	X	X	X	X	X	LCD drive control output
	(TRCIOA)	X	0	X	X	X	X	X	0	1	0	1	0	0	1	X	X	Timer waveform output (output compare function)
													0	1	X			
		0	0	X	X	X	X	X	0	1	X	1	1	0	X	X	X	Timer mode (input capture function)(1)
														1	0			
	(TRCTRG)	0	0	X	X	X	X	X	0	1	X	0	X	X	X	0	1	PWM2 mode (TRCTRG input)
																1	X	
	AN11	0	0	0	1	1	0	1	Other than 01b		X	X	X	X	X	X	X	A/D converter input (AN11)(1)

X: 0 or 1

Note:

1. Pulled up by setting the PU00 bit in the P0PUR register to 1.

Table 7.6 Port P0_1

Register		PD0	LSE0	ADMOD		TRCPSR0			TRC MR	TRC CR2		TRCCR1			INTEN	Function
Bit		PD0_1	LSE01	ADCAP		TRCIOA SEL		TRCCLK SEL0	PWM2	TCEG		TCK			INT7EN	
				1	0	1	0			1	0	2	1	0		
Pin	P0_1	0	0	X	X	Other than 10b		0	X	X	X	X	X	X	X	Input port (1)
		1	0	X	X	Other than 10b		0	X	X	X	X	X	X	X	Output port
	SEG1	X	1	X	X	Other than 10b		0	X	X	X	X	X	X	X	LCD drive control output
	$\overline{\text{INT7}}$	0	0	X	X	Other than 10b		0	X	X	X	X	X	X	1	$\overline{\text{INT7}}$ input (1)
	(TRCCLK)	0	X	X	X	Other than 10b		1	X	X	X	1	0	1	X	TRCCLK input (1)
	(TRCTRG)	0	0	X	X	1	0	0	0	0	1	X	X	X	X	PWM2 mode (TRCTRG input) (1)
										1	X					
	$\overline{\text{ADTRG}}$	0	0	1	1	Other than 10b		0	X	X	X	X	X	X	X	$\overline{\text{ADTRG}}$ input (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU01 bit in the P0PUR register to 1.

Table 7.7 Port P0_2

Register		PD0	LSE0	TRCPSR0		TRCMR	TRCCR2		KI0EN	Function
Bit		PD0_2	LSE02	TRCIOASEL		PWM2	TCEG			
				1	0		1	0		
Pin	P0_2	0	0	Other than 11b		X	X	X	X	Input port (1)
		1	0	Other than 11b		X	X	X	X	Output port
	SEG2	X	1	Other than 11b		X	X	X	X	LCD drive control output
	(TRCTRG)	0	0	1	1	0	0	1	X	PWM2 mode TRCTRG input (1)
							1	X		
	$\overline{KI0}$	0	0	Other than 11b		X	X	X	1	$\overline{KI0}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU02 bit in the P0PUR register to 1.

Table 7.8 Port P0_3

Register		PD0	LSE0	INTSR	INTEN	KIEN	Function
Bit		PD0_3	LSE03	INT0SEL0	INT0EN	KI1EN	
Pin	P0_3	0	0	X	X	X	Input port (1)
		1	0	X	X	X	Output port
	SEG3	X	1	X	X	X	LCD drive control output
	$\overline{INT0}$	0	0	0	1	X	$\overline{INT0}$ input (1)
	$\overline{KI1}$	0	0	X	X	1	$\overline{KI1}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU03 bit in the P0PUR register to 1.

Table 7.9 Port P0_4

Register		PD0	LSE0	KIEN	Function
Bit		PD0_4	LSE04	KI2EN	
Pin	P0_4	0	0	X	Input port (1)
		1	0	X	Output port
	SEG4	X	1	X	LCD drive control output
	$\overline{KI2}$	0	0	1	$\overline{KI2}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU04 bit in the P0PUR register to 1.

Table 7.10 Port P0_5

Register		PD0	LSE0	KIEN	Function
Bit		PD0_5	LSE05	KI3EN	
Pin	P0_5	0	0	X	Input port (1)
		1	0	X	Output port
	SEG5	X	1	X	LCD drive control output
	$\overline{KI3}$	0	0	1	$\overline{KI3}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU05 bit in the P0PUR register to 1.

Table 7.11 Port P0_6

Register		PD0	LSE0	KIEN1	Function
Bit		PD0_6	LSE06	KI4EN1	
Pin	P0_6	0	0	X	Input port (1)
		1	0	X	Output port
	SEG6	X	1	X	LCD drive control output
	$\overline{KI4}$	0	0	1	$\overline{KI4}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU06 bit in the P0PUR register to 1.

Table 7.12 Port P0_7

Register		PD0	LSE0	KIEN1	TRHCR	Function
Bit		PD0_7	LSE07	KI5EN1	TRHOE	
Pin	P0_7	0	0	X	0	Input port (1)
		1	0	X	0	Output port
	SEG7	X	1	X	0	LCD drive control output
	TRHO	X	0	X	1	Timer waveform output
	$\overline{KI5}$	0	0	1	0	$\overline{KI5}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU07 bit in the P0PUR register to 1.

Table 7.13 Port P1_0

Register		PD1	LSE1	Function
Bit		PD1_0	LSE08	
Pin	P1_0	0	0	Input port (1)
		1	0	Output port
	SEG8	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU10 bit in the P1PUR register to 1.

Table 7.14 Port P1_1

Register		PD1	LSE1	Function
Bit		PD1_1	LSE09	
Pin	P1_1	0	0	Input port (1)
		1	0	Output port
	SEG9	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU11 bit in the P1PUR register to 1.

Table 7.15 Port P1_2

Register		PD1	LSE1	KIEN1	Function
Bit		PD1_2	LSE10	KI6EN1	
Pin	P1_2	0	0	X	Input port (1)
		1	0	X	Output port
	SEG10	X	1	X	LCD drive control output
	$\overline{KI6}$	0	0	1	$\overline{KI6}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU12 bit in the P1PUR register to 1.

Table 7.16 Port P1_3

Register		PD1	LSE1	KIEN1	Function
Bit		PD1_3	LSE11	KI7EN1	
Pin	P1_3	0	0	X	Input port (1)
		1	0	X	Output port
	SEG11	X	1	X	LCD drive control output
	$\overline{KI7}$	0	0	1	$\overline{KI7}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU13 bit in the P1PUR register to 1.

Table 7.17 Port P1_4

Register		PD1	LSE1	INTSR	INTEN1	Function
Bit		PD1_4	LSE14	INT4SEL0	INT4EN	
Pin	P1_4	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG12	X	1	X	X	LCD drive control output
	$\overline{INT4}$	0	0	0	1	$\overline{INT4}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU14 bit in the P1PUR register to 1.

Table 7.18 Port P1_5

Register		PD1	LSE1	INTSR	INTEN1	Function
Bit		PD1_5	LSE15	INT5SEL0	INT5EN	
Pin	P1_5	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG13	X	1	X	X	LCD drive control output
	$\overline{INT5}$	0	0	0	1	$\overline{INT5}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU15 bit in the P1PUR register to 1.

Table 7.19 Port P1_6

Register		PD1	LSE2	INTSR	INTEN1	Function
Bit		PD1_6	LSE16	INT6SEL0	INT6EN	
Pin	P1_6	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG14	X	1	X	X	LCD drive control output
	$\overline{INT6}$	0	0	0	1	$\overline{INT6}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU16 bit in the P1PUR register to 1.

Table 7.20 Port P1_7

Register		PD1	LSE2	INTSR	INTEN1	Function
Bit		PD1_7	LSE17	INT7SEL0	INT7EN	
Pin	P1_7	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG15	X	1	X	X	LCD drive control output
	$\overline{INT7}$	0	0	0	1	$\overline{INT7}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU17 bit in the P1PUR register to 1.

Table 7.21 Port P2_0

Register		PD2	LSE2	Function
Bit		PD2_0	LSE20	
Pin	P2_0	0	0	Input port (1)
		1	0	Output port
	SEG16	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU20 bit in the P2PUR register to 1.

Table 7.22 Port P2_1

Register		PD2	LSE2	Function
Bit		PD2_1	LSE21	
Pin	P2_1	0	0	Input port (1)
		1	0	Output port
	SEG17	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU21 bit in the P2PUR register to 1.

Table 7.23 Port P2_2

Register		PD2	LSE2	Function
Bit		PD2_2	LSE22	
Pin	P2_2	0	0	Input port (1)
		1	0	Output port
	SEG18	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU22 bit in the P2PUR register to 1.

Table 7.24 Port P2_3

Register		PD2	LSE2	Function
Bit		PD2_3	LSE23	
Pin	P2_3	0	0	Input port (1)
		1	0	Output port
	SEG19	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU23 bit in the P2PUR register to 1.

Table 7.25 Port P2_4

Register		PD2	LSE2	Function
Bit		PD2_4	LSE24	
Pin	P2_4	0	0	Input port (1)
		1	0	Output port
	SEG20	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU24 bit in the P2PUR register to 1.

Table 7.26 Port P2_5

Register		PD2	LSE2	Function
Bit		PD2_5	LSE25	
Pin	P2_5	0	0	Input port (1)
		1	0	Output port
	SEG21	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU25 bit in the P2PUR register to 1.

Table 7.27 Port P2_6

Register		PD2	LSE2	Function
Bit		PD2_6	LSE26	
Pin	P2_6	0	0	Input port (1)
		1	0	Output port
	SEG22	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU26 bit in the P2PUR register to 1.

Table 7.28 Port P2_7

Register		PD2	LSE2	Function
Bit		PD2_7	LSE27	
Pin	P2_7	0	0	Input port (1)
		1	0	Output port
	SEG23	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU27 bit in the P2PUR register to 1.

Table 7.29 Port P3_0

Register		PD3	LSE3	INTSR	INTEN	Function
Bit		PD3_0	LSE24	INT0SEL0	INT0EN	
Pin	P3_0	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG24	X	1	X	X	LCD drive control output
	($\overline{\text{INT0}}$)	0	0	1	1	$\overline{\text{INT0}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU30 bit in the P3PUR register to 1.

Table 7.30 Port P3_1

Register		PD3	LSE3	INTSR	INTEN	Function
Bit		PD3_1	LSE25	INT1SEL0	INT1EN	
Pin	P3_1	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG25	X	1	X	X	LCD drive control output
	($\overline{\text{INT1}}$)	0	0	1	1	$\overline{\text{INT1}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU31 bit in the P3PUR register to 1.

Table 7.31 Port P3_2

Register		PD3	LSE3	INTSR	INTEN	Function
Bit		PD3_2	LSE26	INT2SEL0	INT2EN	
Pin	P3_2	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG26	X	1	X	X	LCD drive control output
	($\overline{\text{INT2}}$)	0	0	1	1	$\overline{\text{INT2}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU32 bit in the P3PUR register to 1.

Table 7.32 Port P3_3

Register		PD3	LSE3	INTSR	INTEN	Function
Bit		PD3_3	LSE27	INT3SEL0	INT3EN	
Pin	P3_3	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG27	X	1	X	X	LCD drive control output
	($\overline{\text{INT3}}$)	0	0	1	1	$\overline{\text{INT3}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU33 bit in the P3PUR register to 1.

Table 7.33 Port P3_4

Register		PD3	LSE3	INTSR	INTEN	Function
Bit		PD3_4	LSE28	INT4SEL0	INT4EN	
Pin	P3_4	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG28	X	1	X	X	LCD drive control output
	($\overline{\text{INT4}}$)	0	0	1	1	$\overline{\text{INT4}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU34 bit in the P3PUR register to 1.

Table 7.34 Port P3_5

Register		PD3	LSE3	INTSR	INTEN	Function
Bit		PD3_5	LSE29	INT5SEL0	INT5EN	
Pin	P3_5	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG29	X	1	X	X	LCD drive control output
	($\overline{\text{INT5}}$)	0	0	1	1	$\overline{\text{INT5}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU35 bit in the P3PUR register to 1.

Table 7.35 Port P3_6

Register		PD3	LSE3	INTSR	INTEN	Function
Bit		PD3_6	LSE30	INT6SEL0	INT6EN	
Pin	P3_6	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG30	X	1	X	X	LCD drive control output
	($\overline{\text{INT6}}$)	0	0	1	1	$\overline{\text{INT6}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU36 bit in the P3PUR register to 1.

Table 7.36 Port P3_7

Register		PD3	LSE3	INTSR	INTEN	Function
Bit		PD3_7	LSE31	INT7SEL0	INT7EN	
Pin	P3_7	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG31	X	1	X	X	LCD drive control output
	($\overline{\text{INT7}}$)	0	0	1	1	$\overline{\text{INT7}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU37 bit in the P3PUR register to 1.

Table 7.37 Port P4_0

Register		PD4	LSE4	Function
Bit		PD4_0	LSE32	
Pin	P4_0	0	0	Input port (1)
		1	0	Output port
	SEG32	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU40 bit in the P4PUR register to 1.

Table 7.38 Port P4_1

Register		PD4	LSE4	Function
Bit		PD4_1	LSE33	
Pin	P4_1	0	0	Input port (1)
		1	0	Output port
	SEG33	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU41 bit in the P4PUR register to 1.

Table 7.39 Port P4_2

Register		PD4	LSE4	Function
Bit		PD4_2	LSE34	
Pin	P4_2	0	0	Input port (1)
		1	0	Output port
	SEG34	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU42 bit in the P4PUR register to 1.

Table 7.40 Port P4_3

Register		PD4	LSE4	Function
Bit		PD4_3	LSE35	
Pin	P4_3	0	0	Input port (1)
		1	0	Output port
	SEG35	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU43 bit in the P4PUR register to 1.

Table 7.41 Port P4_4

Register		PD4	LSE4	Function
Bit		PD4_4	LSE36	
Pin	P4_4	0	0	Input port (1)
		1	0	Output port
	SEG36	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU44 bit in the P4PUR register to 1.

Table 7.42 Port P4_5

Register		PD4	LSE4	Function
Bit		PD4_5	LSE37	
Pin	P4_5	0	0	Input port (1)
		1	0	Output port
	SEG37	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU45 bit in the P4PUR register to 1.

Table 7.43 Port P4_6

Register		PD4	LSE4	Function
Bit		PD4_6	LSE38	
Pin	P4_6	0	0	Input port (1)
		1	0	Output port
	SEG38	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU46 bit in the P4PUR register to 1.

Table 7.44 Port P4_7

Register		PD4	LSE	LCR4		Function
Bit		PD4_7	LSE39	LCTZS	COMEXP	
Pin	P4_7	0	0	X	X	Input port (1)
		1	0	X	X	Output port
	SEG39	X	1	0	0	LCD drive control output
	COMEXP	X	1	1	1	LCD drive control output (memory-type liquid crystal panel)

X: 0 or 1
Note:
1. Pulled up by setting the PU47 bit in the P4PUR register to 1.

Table 7.45 Port P5_0

Register		PD5	LSE5	Function
Bit		PD5_0	LCOM0	
Pin	P5_0	0	0	Input port (1)
		1	0	Output port
	COM0	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU50 bit in the P5PUR register to 1.

Table 7.46 Port P5_1

Register		PD5	LSE5	Function
Bit		PD5_1	LCOM1	
Pin	P5_1	0	0	Input port (1)
		1	0	Output port
	COM1	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU51 bit in the P5PUR register to 1.

Table 7.47 Port P5_2

Register		PD5	LSE5	Function
Bit		PD5_2	LCOM2	
Pin	P5_2	0	0	Input port (1)
		1	0	Output port
	COM2	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU52 bit in the P5PUR register to 1.

Table 7.48 Port P5_3

Register		PD5	LSE5	Function
Bit		PD5_3	LCOM3	
Pin	P5_3	0	0	Input port (1)
		1	0	Output port
	COM3	X	1	LCD drive control output

X: 0 or 1
Note:
1. Pulled up by setting the PU53 bit in the P5PUR register to 1.

Table 7.49 Port P5_4

Register		PD5	LSE5	Function
Bit		PD5_4	LVLP1	
Pin	P5_4	0	0	Input port (1)
		1	0	Output port
	VL1	X	1	VL voltage input

X: 0 or 1
Note:
1. Pulled up by setting the PU54 bit in the P5PUR register to 1.

Table 7.50 Port P5_5

Register		PD5	LSE5	Function
Bit		PD5_5	LVLP2	
Pin	P5_5	0	0	Input port (1)
		1	0	Output port
	VL2	X	1	VL voltage input

X: 0 or 1
Note:
1. Pulled up by setting the PU55 bit in the P5PUR register to 1.

Table 7.51 Port P5_6

Register		PD5	LSE5	Function
Bit		PD5_6	LVLP3	
Pin	P5_6	0	0	Input port (1)
		1	0	Output port
	VL3	X	1	VL voltage input

X: 0 or 1

Note:

1. Pulled up by setting the PU56 bit in the P5PUR register to 1.

Table 7.52 Port P6_0

Register		PD6	ADINSEL					TRBSR		TRJ2IOC	TRJ2MR			Function
Bit		PD6_0	CH			ADGSEL		TRJ2IOSEL		TOPCR	TMOD			
			2	1	0	1	0	1	0		2	1	0	
Pin	P6_0	0	X	X	X	X	X	Other than 01b		1	X	X	X	Input port (1)
		1	X	X	X	X	X	Other than 01b		1	X	X	X	Output port
	AN3	0	0	1	1	0	0	Other than 01b		1	X	X	X	A/D converter input (AN3)(1)
	(TRJ2IO)	X	X	X	X	X	X	0	1	0	0	0	1	Pulse output mode
										0	0	1	0	Event counter mode
										0	0	1	1	Pulse width measurement mode
										0	1	0	0	Pulse period measurement mode

X: 0 or 1

Note:

1. Pulled up by setting the PU60 bit in the P6PUR register to 1.

Table 7.53 Port P6_1

Register		PD6	ADINSEL					TRJSR		TRJ1IOC	TRJ1MR			SSUIICSR	SSMR2		Function
Bit		PD6_1	CH			ADGSEL		TRJ1IOSEL		TOPCR	TMOD			SCSSEL0	CSS		
			2	1	0	1	0	1	0		2	1	0		1	0	
Pin	P6_1	0	X	X	X	X	X	Other than 01b		1	X	X	X	0	0	0	Input port (1)
		1	X	X	X	X	X	Other than 01b		1	X	X	X	0	0	0	Output port
	AN4	0	1	0	0	0	0	Other than 01b		1	X	X	X	0	0	0	A/D converter input (AN4) (1)
	(TRJ1IO)	X	X	X	X	X	X	0	1	0	0	0	1	0	0	0	Pulse output mode
										0	0	1	0				Event counter mode
										0	0	1	1				Pulse width measurement mode
										0	1	0	0				Pulse period measurement mode
	($\overline{SCS}$)	0	X	X	X	X	X	X	X	1	X	X	X	1	0	1	$\overline{SCS}$ input (1)
		0	X	X	X	X	X	X	X	1	X	X	X	1	1	X	$\overline{SCS}$ output (2)

X: 0 or 1

Notes:

1. Pulled up by setting the PU61 bit in the P6PUR register to 1.
2. N-channel open-drain output by setting the CSOS bit in the SSMR2 register to 1.

Table 7.54 Port P6_2

Register		PD6	ADINSEL					TRJSR		TRJ0IOC	TRJ0MR			SSUIICSR		SSU Associated Register (3)		Function
Bit		PD6_2	CH			ADG SEL		TRJ0IO SEL		TOPCR	TMOD			SSI SEL0	IIC SEL	SSI		
			2	1	0	1	0	1	0		2	1	0			Output control	Input control	
Pin	P6_2	0	X	X	X	X	X	Other than 01b		1	X	X	X	0	X	0	0	Input port (1)
		1	X	X	X	X	X	Other than 01b		1	X	X	X	0	X	0	0	Output port
	AN5	0	1	0	1	0	0	Other than 01b		1	X	X	X	0	X	0	0	A/D converter input (AN5) (1)
	(TRJ0IO)	X	X	X	X	X	X	0	1	0	0	0	1	0	X	0	0	Pulse output mode
										0	0	1	0					Event counter mode
										0	0	1	1					Pulse width measurement mode
										0	1	0	0					Pulse period measurement mode
	(SSI)	0	X	X	X	X	X	Other than 01b		1	X	X	X	1	0	0	1	SSI input (1)
		X	X	X	X	X	X	Other than 01b		1	X	X	X	1	0	1	0	SSI output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU62 bit in the P6PUR register to 1.
2. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit to 0 (standard mode).
3. Synchronous serial communication unit (refer to **Table 24.4 Association between Communication Modes and I/O Pins**).

Table 7.55 Port P6_3

Register		PD6	ADINSEL					SSUIICSR		SSMR2	SSU Associated Register (3)		Function
Bit		PD6_3	CH			ADGSEL		SSCKSEL0	IICSEL	SCKS	SSCK		
			2	1	0	1	0				Output control	Input control	
Pin	P6_3	0	X	X	X	X	X	0	0	0	0	0	Input port (1)
									1		X	X	
		1	X	X	X	X	X	0	0	0	0	0	Output port
									1		X	X	
	AN6	0	1	1	0	0	0	0	0	0	0	0	A/D converter input (AN6) (1)
									1		X	X	
	(SCL)	0	X	X	X	X	X	1	1	0	1	X	SCL input/output
	(SSCK)	0	X	X	X	X	X	1	0	1	0	1	SSCK input (1)
		0	X	X	X	X	X	1	0	1	1	0	SSCK output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU63 bit in the P6PUR register to 1.
2. N-channel open-drain output by setting the SCKDS bit in the SSMR2 register to 1. At this time, set the PD6_3 bit in the PD6 register to 0.
3. Synchronous serial communication unit (refer to **Table 24.4 Association between Communication Modes and I/O Pins**).

Table 7.56 Port P6_4

Register		PD6	ADINSEL					SSUIICSR		SSU Associated Register (3)		Function
Bit		PD6_4	CH			ADGSEL		SSOSEL0	IICSEL	SSI		
			2	1	0	1	0			Output control	Input control	
Pin	P6_4	0	X	X	X	X	X	0	1	X	X	Input port (1)
									0	0	0	
		1	X	X	X	X	X	0	1	X	X	Output port
									0	0	0	
	AN7	0	1	1	1	0	0	0	1	X	X	A/D converter input (AN7) (1)
									0	0	0	
	(SDA)	0	X	X	X	X	X	1	1	X	X	SDA input/output
	(SSO)	0	X	X	X	X	X	1	0	0	1	SSO input (1)
		0	X	X	X	X	X	1		1	0	SSO output (2)

X: 0 or 1

Notes:

1. Pulled up by setting the PU64 bit in the P6PUR register to 1.
2. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit to 0 (standard mode)
3. Synchronous serial communication unit (refer to **Table 24.4 Association between Communication Modes and I/O Pins**).

Table 7.57 Port P6_5

Register		PD6	ADINSEL					TRC PSR0		TRC PSR1	TRC OER		TRCMR			TRC IOR0			TRC IOR1			INT CMP	TRB 1IOC	TRB SR		TRB 1MR		Function
Bit		PD 6_5	CH			ADG SEL		TRC IOB SEL		TRC IOD SEL0	EB	ED	PWM			IOB			IOD			INT1 CP0	TOC NT	TRB1 OSEL		TM OD		
			2	1	0	1	0	1	0				2	B	D	2	1	0	2	1	0			1	0	1	0	
Pin	P6_5	0	X	X	X	X	X	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	X	X	Other than 01b		0	0	Input port (1)
		1	X	X	X	X	X	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	X	X	Other than 01b		0	0	Output port
		X																					1			X	X	
	AN8	0	0	0	0	0	1	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	X	X	Other than 01b		0	0	A/D converter input (AN8) (1)
	(TRCIOB)	X	X	X	X	X	X	1	1	0	0	X	0	X	X	X	X	X	X	X	X	X	X	Other than 01b		0	0	PWM2 mode waveform output
		X	X	X	X	X	X	1	1	0	0	X	1	1	X	X	X	X	X	X	X	X	X	Other than 01b		0	0	PWM mode waveform output
		X	X	X	X	X	X	1	1	0	0	X	1	0	X	0	0	1	X	X	X	X	X	Other than 01b		0	0	Timer waveform output (output compare function)
																0	1	X										
		0	X	X	X	X	X	1	1	0	X	X	1	0	X	1	0	X	X	X	X	X	X	Other than 01b		0	0	Timer mode (input capture function) (1)
																	1	0										
	(TRCIOD)	X	X	X	X	X	X	X		1	X	0	1	X	1	X	X	X	X	X	X	X	X	Other than 01b		0	0	PWM mode waveform output
		X	X	X	X	X	X	X		1	X	0	1	X	0	X	X	X	0	0	1	X	X	Other than 01b		0	0	Timer waveform output (output compare function)
																			0	1	X	X	X	Other than 01b				
		0	X	X	X	X	X	X		1	X	X	1	X	0	X	X	X	1	X	X	X	X	Other than 01b		0	0	Timer mode (input capture function) (1)
	IVREF1	0	X	X	X	X	X	Other than 11b		0	X	X	X	X	X	X	X	X	X	X	X	1	X	Other than 01b		0	0	Comparator B1 reference voltage input (IVREF1)
	(TRB1O)	X	X	X	X	X	X	Other than 11b		X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	Programmable waveform generation mode (pulse output)
		X	X	X	X	X	X	Other than 11b		X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	Programmable one-shot waveform generation mode
		X	X	X	X	X	X	Other than 11b		X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	Programmable wait one-shot waveform generation mode

X: 0 or 1

Note:

1. Pulled up by setting the PU65 bit in the P6PUR register to 1.

Table 7.58 Port P6_6

Register		PD6	ADINSEL					TRC PSR0		TRC PSR1	TRC OER		TRCMR			TRC IOR0			TRC IOR1			INT CMP	TRB 0IOC	TRB SR		TRB 0MR		Function
Bit		PD 6_6	CH			ADG SEL		TRC IOB SEL		TRC IOCS EL0	EB	ED	PWM			IOB			IOD			INT1 CP0	TOC NT	TRB0 OSEL		TM OD		
			2	1	0	1	0	1	0				2	B	D	2	1	0	2	1	0			1	0	1	0	
Pin	P6_6	0	X	X	X	X	X	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	X	X	Other than 10b		0	0	Input port (1)
		1	X	X	X	X	X	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	X	X	Other than 10b		0	0	Output port
		X																					1			X	X	
	AN9	0	0	0	1	0	1	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	X	X	Other than 10b		0	0	A/D converter input (AN9) (1)
	(TRCIOB)	X	X	X	X	X	X	1	0	0	0	X	0	X	X	X	X	X	X	X	X	X	X	Other than 10b		0	0	PWM2 mode waveform output
		X	X	X	X	X	X	1	0	0	0	X	1	1	X	X	X	X	X	X	X	X	X	Other than 10b		0	0	PWM mode waveform output
		X	X	X	X	X	X	1	0	0	0	X	1	0	X	0	0	1	X	X	X	X	X	Other than 10b		0	0	Timer waveform output (output compare function)
																0	1	X										
		0	X	X	X	X	X	1	0	0	X	X	1	0	X	1	0	X	X	X	X	X	X	Other than 10b		0	0	Timer mode (input capture function) (1)
																	1	0										
	(TRCIOC)	X	X	X	X	X	X	X		1	X	0	1	X	1	X	X	X	X	X	X	X	X	Other than 10b		0	0	PWM mode waveform output
		X	X	X	X	X	X	X		1	X	0	1	X	0	X	X	X	0	0	1	X	X	Other than 10b		0	0	Timer waveform output (output compare function)
																			0	1	X							
		0	X	X	X	X	X	X		1	X	X	1	X	0	X	X	X	1	X	X	X	X	Other than 10b		0	0	Timer mode (input capture function) (1)
	IVREF3	0	X	X	X	X	X	Other than 10b		0	X	X	X	X	X	X	X	X	X	X	X	1	X	Other than 10b		0	0	Comparator B1 reference voltage input (IVREF3)
	(TRB0O)	X	X	X	X	X	X	Other than 10b		X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	0	1	Programmable waveform generation mode (pulse output)
		X	X	X	X	X	X	Other than 10b		X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	1	0	Programmable one-shot waveform generation mode
		X	X	X	X	X	X	Other than 10b		X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	1	1	Programmable wait one-shot waveform generation mode

X: 0 or 1

Note:

1. Pulled up by setting the PU66 bit in the P6PUR register to 1.

Table 7.59 Port P6_7

Register		PD6	ADINSEL					TRCPSR0		TRCOER	TRCMR			TRCIOR0			Function
Bit		PD6_7	CH			ADGSEL		TRCIOBSEL		EB	PWM			IOB			
			2	1	0	1	0	1	0		2	B	D	2	1	0	
Pin	P6_7	0	X	X	X	X	X	Other than 10b		X	X	X	X	X	X	X	Input port (1)
		1	X	X	X	X	X	Other than 10b		X	X	X	X	X	X	X	Output port
	AN10	0	0	1	0	0	1	Other than 10b		X	X	X	X	X	X	X	A/D converter input (AN10) (1)
	(TRCIOB)	X	X	X	X	X	X	0	1	0	0	X	X	X	X	X	PWM2 mode waveform output
		X	X	X	X	X	X	0	1	0	1	1	X	X	X	X	PWM mode waveform output
		X	X	X	X	X	X	0	1	0	1	0	X	0	0	1	Timer waveform output (output compare function)
														0	1	X	
		0	X	X	X	X	X	0	1	X	1	0	X	1	0	X	Timer mode (input capture function) (1)
															1	0	

X: 0 or 1

Note:

1. Pulled up by setting the PU67 bit in the P6PUR register to 1.

Table 7.60 Port P7_0

Register		PD7	U2SR1		U2MR				Function
Bit		PD7_0	CLK2SEL		SMD			CKDIR	
			1	0	2	1	0		
Pin	P7_0	0	Other than 01b		X	X	X	X	Input port (1)
		1	Other than 01b		X	X	X	X	Output port (2)
	(CLK2)	0	0	1	X	X	X	1	CLK2 input (1)
		0	0	1	0	0	1	0	CLK2 output (2, 3)
	TRJ2O	X	Other than 01b		X	X	X	X	Pulse output mode (2)
	$\overline{\text{WKUP1}}$	0	Other than 01b		X	X	X	X	$\overline{\text{WKUP1}}$ input (1)

X: 0 or 1

Notes:

1. Pulled up by setting the PU70 bit in the P7PUR register to 1.
2. Output drive capacity high by setting the P7DRR0 bit in the P7DRR register to 1.
3. N-channel open-drain output by setting the NODC bit in the U2SMR3 register to 1.

Table 7.61 Port P7_1

Register		PD7	U2SR0				U2MR			U2SMR	Function
Bit		PD7_1	TXD2SEL		RXD2SEL		SMD			IICM	
			1	0	1	0	2	1	0		
Pin	P7_1	0	Other than 01b		Other than 10b		X	X	X	X	Input port (1)
		1	Other than 01b		Other than 10b		X	X	X	X	Output port (2)
	(TXD2)	X	0	1	Other than 10b		0	0	1	0	TXD2 output (2, 3)
							1	0	X		
							1	1	0		
	(RXD2)	0	Other than 01b		1	0	X	X	X	0	RXD2 input (2)
	(SDA2)	0	0	1	Other than 10b		0	1	0	1	SDA2 input/output (2, 3)
	(SCL2)	0	Other than 01b		1	0	0	1	0	1	SCL2 input/output (2, 3)
	TRJ1O	X	Other than 01b		Other than 10b		X	X	X	X	Pulse output mode (2)

X: 0 or 1

Notes:

1. Pulled up by setting the PU71 bit in the P7PUR register to 1.
2. Output drive capacity high by setting the P7DRR1 bit in the P7DRR register to 1.
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1. At this time, set the PD7_1 bit in the PD7 register to 0.

Table 7.62 Port P7_2

Register		PD7	U2SR0				U2MR			U2SMR	Function
Bit		PD7_2	TXD2SEL		RXD2SEL		SMD			IICM	
			1	0	1	0	2	1	0		
Pin	P7_2	0	Other than 10b		Other than 01b		X	X	X	X	Input port (1)
		1	Other than 10b		Other than 01b		X	X	X	X	Output port
	(TXD2)	X	1	0	Other than 01b		0	0	1	0	TXD2 output (2)
							1	0	X		
							1	1	0		
	(RXD2)	0	Other than 10b		1	0	X	X	X	0	RXD2 input (1)
	(SDA2)	0	1	0	Other than 01b		0	1	0	1	SDA2 input/output (2)
	(SCL2)	0	Other than 10b		0	1	0	1	0	1	SCL2 input/output (2)
	TRJ0O	X	Other than 10b		Other than 01b		X	X	X	X	Pulse output mode

X: 0 or 1

Notes:
1. Pulled up by setting the PU72 bit in the P7PUR register to 1.
2. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1. At this time, set the PD7_2 bit in the PD7 register to 0.

Table 7.63 Port P7_3

Register		PD7	U2C0		U2SR1		U2MR			Function
Bit		PD7_3	CRS	CRD	CTS2SEL		SMD			
					1	0	2	1	0	
Pin	P7_3	0	X	X	Other than 01b		X	X	X	Input port (1)
		1	X	X	Other than 01b		X	X	X	Output port
	($\overline{\text{CTS2}}$)	0	0	0	0	1	Other than 000b			$\overline{\text{CTS2}}$ input (1)
	($\overline{\text{RTS2}}$)	0	1	0	0	1	Other than 000b			$\overline{\text{RTS2}}$ output

X: 0 or 1

Note:
1. Pulled up by setting the PU73 bit in the P7PUR register to 1.

Table 7.64 Port P7_4

Register		PD7	ADINSEL			ADGSEL		Function
Bit		PD7_4	CH			1	0	
			2	1	0			
Pin	P7_4	0	X	X	X	X	X	Input port (1)
		1	X	X	X	X	X	Output port
	AN0	0	0	0	0	0	0	A/D converter input (AN0) (1)

X: 0 or 1

Note:
1. Pulled up by setting the PU74 bit in the P7PUR register to 1.

Table 7.65 Port P7_5

Register		PD7	ADINSEL					TRB1IOC	TRBSR		TRB1MR		Function
Bit		PD7_5	CH			ADGSEL		TOCNT	TRB1OSEL		TMOD		
			2	1	0	1	0		1	0	1	0	
Pin	P7_5	0	X	X	X	X	X	X	Other than 00b		0	0	Input port (1)
		1	X	X	X	X	X	X	Other than 00b		0	0	Output port
		X						1					
	AN1	0	0	0	1	0	0	X	Other than 00b		0	0	A/D converter input (AN1) (1)
	TRB1O	X	X	X	X	X	X	0	0	0	0	1	Programmable waveform generation mode (pulse output)
		X	X	X	X	X	X	0	0	0	1	0	Programmable one-shot waveform generation mode
		X	X	X	X	X	X	0	0	0	1	1	Programmable wait one-shot waveform generation mode

X: 0 or 1

Note:

1. Pulled up by setting the PU75 bit in the P7PUR register to 1.

Table 7.66 Port P7_6

Register		PD7	ADINSEL					VCA2	TRB1IOC	TRBSR		TRB1MR		Function
Bit		PD7_6	CH			ADGSEL		VCA24	TOCNT	TRB0OSEL		TMOD		
			2	1	0	1	0			1	0	1	0	
Pin	P7_6	0	X	X	X	X	X	X	X	Other than 01b		0	0	Input port (1)
		1	X	X	X	X	X	X	X	Other than 01b		0	0	Output port
		X							1					
	AN2	0	0	1	0	0	0	X	X	Other than 01b		0	0	A/D converter input (AN2) (1)
	(TRB0O)	X	X	X	X	X	X	X	0	0	1	0	1	Programmable waveform generation mode (pulse output)
		X	X	X	X	X	X	X	0	0	1	1	0	Programmable one-shot waveform generation mode
		X	X	X	X	X	X	X	0	0	1	1	1	Programmable wait one-shot waveform generation mode

X: 0 or 1

Note:

1. Pulled up by setting the PU76 bit in the P7PUR register to 1.

Table 7.67 Port P8_0

Register		PD8	INTSR	INTEN	INTCMP	SSUIICSR	SSMR2		Function
Bit		PD8_0	INT1SEL0	INT1EN	INT1CP0	SCSSEL0	CSS		
							1	0	
Pin	P8_0	0	X	X	X	1	0	0	Input port (1)
		1	X	X	X	1	0	0	Output port (2)
	$\overline{SCS}$	0	X	X	X	0	0	1	$\overline{SCS}$ input (1)
		0	X	X	X	0	1	X	$\overline{SCS}$ output (1, 2, 3)
	$\overline{INT1}$	0	0	1	0	1	0	0	$\overline{INT1}$ input (1)
	IVCMP1	0	X	X	1	1	0	0	Comparator B1 input (IVCMP1)

X: 0 or 1

Notes:

1. Pulled up by setting the PU80 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR0 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the CSOS bit in the SSMR2 register to 1.

Table 7.68 Port P8_1

Register		PD8	INTSR	INTEN	INTCMP	SSUIICSR		SSU Associated Register (4)		Function
Bit		PD8_1	INT3SEL0	INT3EN	INT3CP0	SSISEL0	IICSEL	SSI		
								Output control	Input control	
Pin	P8_1	0	X	X	X	1	X	0	0	Input port (1)
		1	X	X	X	1	X	0	0	Output port (2)
	SSI	0	X	X	X	0	0	0	1	SSI input (1)
		X	X	X	X	0	0	1	0	SSI output (1, 2, 3)
	$\overline{\text{INT3}}$	0	0	1	0	1	X	0	0	$\overline{\text{INT3}}$ input (1)
	IVCMP3	0	X	X	1	1	X	0	0	Comparator B1 input (IVCMP3)

X: 0 or 1

Notes:
1. Pulled up by setting the PU81 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR1 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit to 0 (standard mode).
4. Synchronous serial communication unit (refer to **Table 24.4 Association between Communication Modes and I/O Pins**).

Table 7.69 Port P8_2

Register		PD8	TRJSR		TRJ1IOC	TRJ1MR			SSUIICSR		SSMR2	SSU Associated Register (4)		Function
Bit		PD8_2	TRJ1OSEL		TOPCR	TMOD			SSCK SEL0	IICSEL	SCKS	SSCK		
			1	0		2	1	0				Output control	Input control	
Pin	P8_2	0	Other than 10b		1	X	X	X	1	0	0	0	0	Input port (1)
										1		X	X	
		1	Other than 10b		1	X	X	X	1	0	0	0	0	Output port (2)
										1		X	X	
	SCL	0	Other than 10b		1	X	X	X	0	1	0	X	X	SCL input/output (1, 2)
	SSCK	0	Other than 10b		1	X	X	X	0	0	1	0	1	SSCK input (1)
		0	Other than 10b						0	0	1	1	0	SSCK output (1, 2, 3)
	(TRJ1IO)	X	1	0	0	0	0	1	1	0	0	0	0	Pulse output mode (1, 2)
										1		X	X	
		X	1	0	0	0	1	0	1	0	0	0	0	Event counter mode
										1		X	X	
		X	1	0	0	0	1	1	1	0	0	0	0	Pulse width measurement mode
										1		X	X	
		X	1	0	0	1	0	0	1	0	0	0	0	Pulse period measurement mode
										1		X	X	

X: 0 or 1

Notes:
1. Pulled up by setting the PU82 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR2 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1. At this time, set the PD8_2 bit in the PD8 register to 0.
4. Synchronous serial communication unit (refer to **Table 24.4 Association between Communication Modes and I/O Pins**).

Table 7.70 Port P8_3

Register		PD8	TRJSR		TRJ0IOC	TRJ0MR			SSUIICSR		SSMR2	SSU Associated Register (4)		Function
Bit		PD8_3	TRJ0OSEL		TOPCR	TMOD			SSO SEL0	IICSEL	SCKS	SSI		
			1	0		2	1	0				Output control	Input control	
Pin	P8_3	0	Other than 10b		1	X	X	X	1	1	0	X	X	Input port (1)
										0		0	0	
		1	Other than 10b		1	X	X	X	1	1	0	X	X	Output port (2)
										0		0	0	
	SDA	0	Other than 10b		1	X	X	X	0	1	0	X	X	SDA input/output (1, 2)
	SSO	0	Other than 10b		1	X	X	X	0	0	1	0	1	SSO input (1)
		0	Other than 10b						0	0	1	1	0	SSO output (1, 2, 3)
	TRJ0IO	X	1	0	0	0	0	1	1	0	0	0	0	Pulse output mode (1, 2)
										1		X	X	
		X	1	0	0	0	1	0	1	0	0	0	0	Event counter mode
										1		X	X	
		X	1	0	0	0	1	1	1	0	0	0	0	Pulse width measurement mode
										1		X	X	
		X	1	0	0	1	0	0	1	0	0	0	0	Pulse period measurement mode
										1		X	X	

X: 0 or 1

Notes:
1. Pulled up by setting the PU83 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR3 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit to 0 (standard mode).
4. Synchronous serial communication unit (refer to **Table 24.4 Association between Communication Modes and I/O Pins**).

Table 7.71 Port P8_4

Register		PD8	U0SR		U0MR				U2SR1		U2MR				Function
Bit		PD8_4	CLK0SEL		SMD			CKDIR	CLK2SEL		SMD			CKDIR	
			1	0	2	1	0		1	0	2	1	0		
Pin	P8_4	0	Other than 01b		X	X	X	X	Other than 10b		X	X	X	X	Input port (1)
		1	Other than 01b		X	X	X	X	Other than 10b		X	X	X	X	Output port (2)
	CLK0	0	0	1	X	X	X	1	Other than 10b		X	X	X	X	CLK0 (external clock input) (1)
		X	0	1	0	0	1	0	Other than 10b		X	X	X	X	CLK0 (internal clock output) (2)
	CLK2	0	Other than 01b		X	X	X	X	1	0	X	X	X	1	CLK2 (external clock input) (1)
		X	Other than 01b		X	X	X	X	1	0	0	0	1	0	CLK2 (internal clock output) (2, 3)

X: 0 or 1

Notes:
1. Pulled up by setting the PU84 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR4 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the NODC bit in the U2SMR3 register to 1. At this time, set the PD8_4 bit in the PD8 register to 0.

Table 7.72 Port P8_5

Register		PD8	U0SR		U0MR			U2SR0		U2MR			U2SMR	Function
Bit		PD8_5	TXD0SEL		SMD			TXD2SEL		SMD			IICM	
			1	0	2	1	0	1	0	2	1	0		
Pin	P8_5	0	Other than 01b		X	X	X	Other than 11b		X	X	X	X	Input port (1)
		1	Other than 01b		X	X	X	Other than 11b		X	X	X	X	Output port (2)
	(TXD0)	X	0	1	0	0	1	Other than 11b		X	X	X	X	TXD0 output (2)
					1	0	X							
					1	1	0							
	(TXD2)	X	Other than 01b		X	X	X	1	1	0	0	1	0	TXD2 output (2, 3)
										1	0	X		
										1	1	0		
	(SDA2)	0	Other than 01b		X	X	X	1	1	0	1	0	1	SDA2 input/output (2, 3)

X: 0 or 1

Notes:

1. Pulled up by setting the PU85 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR5 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1. At this time, set the PD8_5 bit in the PD8 register to 0.

Table 7.73 Port P8_6

Register		PD8	U0SR		U2SR0		U2MR			U2SMR	Function
Bit		PD8_6	RXD0SEL		RXD2SEL		SMD			IICM	
			1	0	1	0	2	1	0		
Pin	P8_6	0	Other than 01b		Other than 11b		X	X	X	X	Input port (1)
		1	Other than 01b		Other than 11b		X	X	X	X	Output port (2)
	(RXD0)	0	0	1	Other than 11b		X	X	X	X	RXD0 input (2)
	(RXD2)	0	Other than 01b		1	1	X	X	X	1	RXD2 input (2)
	(SCL2)	0	Other than 01b		1	1	0	1	0	1	SCL2 input/output (3)

X: 0 or 1

Notes:

1. Pulled up by setting the PU86 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR6 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1. At this time, set the PD8_6 bit in the PD8 register to 0.

Table 7.74 Port P8_7

Register		PD8	TRB0 IOC	TRBSR		TRB0MR		INTSR	INTEN	U2C0		U2SR1		U2MR			Function
Bit		PD8_7	TOC NT	TRB0OSEL		TMOD		INT2 SEL0	INT2 EN	CRS	CRD	CTSSEL		SMD			
				1	0	1	0					1	0	2	1	0	
Pin	P8_7	0	X	Other than 00b		0	0	X	X	X	X	Other than 10b		X	X	X	Input port (1)
		1	X	Other than 00b		0	0	X	X	X	X	Other than 10b		X	X	X	Output port (2)
		X	1														
	TRB0O	X	0	0	0	0	1	X	X	X	X	Other than 10b		X	X	X	Programmable waveform generation mode (pulse output) (2)
		X	0	0	0	1	0	X	X	X	X	Other than 10b		X	X	X	Programmable one-shot waveform generation mode (2)
		X	0	0	0	1	1	X	X	X	X	Other than 10b		X	X	X	Programmable wait one-shot waveform generation mode (2)
	$\overline{INT2}$	0	X	Other than 00b		0	0	0	1	X	X	Other than 10b		X	X	X	$\overline{INT2}$ input (1)
	($\overline{CTS2}$)	0	X	Other than 00b		0	0	X	X	0	0	1	0	Other than 000b			$\overline{CTS2}$ input (1)
	($\overline{RTS2}$)	0	X	Other than 00b		0	0	X	X	1	0	1	0	Other than 000b			$\overline{RTS2}$ output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU87 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR7 bit in the P8DRR register to 1.

Table 7.75 Port P9_0

Register		PD9	CM0		CM1			Circuit Specifications		Function
Bit		PD9_0	CM05	CM07	CM10	CM11	CM13	Oscillation buffer	Feedback resistor	
Pin	P9_0	0	1	X	0	1	0	OFF	OFF	Input port (1)
		1	1	X	0	1	0	OFF	OFF	Output port
	XIN	0	0	0	0	1	0	ON	ON	XIN clock input (1)
		0	0	0	1	1	0	ON	ON	XIN clock input stop (STOP mode)(1)
		0	0	0	0	0	1	ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
		0	0	0	0	1	1	ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
		0	1	0	0	0	1	OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
		0	1	0	0	1	1	OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
		0	0	0	1	X	1	OFF	OFF	Oscillation stop (STOP mode)

X: 0 or 1

Note:
1. Pulled up by setting the PU90 bit in the P9PUR register to 1.

Table 7.76 Port P9_1

Register		PD9	CM0		CM1			Circuit Specifications		Function
Bit		PD9_1	CM05	CM07	CM10	CM11	CM13	Oscillation buffer	Feedback resistor	
Pin	P9_1	0	X	X	0	1	0	OFF	OFF	Input port (1)
		1	X	X	0	1	0	OFF	OFF	Output port
	XOUT	0	0	0	0	0	1	ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
		0	0	0	0	1	1	ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
		0	1	0	0	0	1	OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
		0	1	0	0	1	1	OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
		0	0	0	1	X	1	OFF	OFF	Oscillation stop (STOP mode)

X: 0 or 1

Note:

1. Pulled up by setting the PU91 bit in the P9PUR register to 1.

7.7 Unassigned Pin Handling

Table 7.77 lists Unassigned Pin Handling.

Table 7.77 Unassigned Pin Handling

Pin Name	Connection
Ports P0 to P4, P5_0 to P5_6, Ports P6, P7_0 to P7_6, P8, P9_0, P9_1	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up). (2) • After setting to output mode, leave these pins open. (1, 2)
XCOUT	Open
XCIN, VL1	Connect to VCC via a pull-up resistor. (2)
VREF, VL2, VL3	Connect to VCC.
$\overline{\text{WKUP0}}$ (3)	Connect to VSS. (3)
$\overline{\text{RESET}}$ (4)	Connect to VCC via a pull-up resistor. (4)

Notes:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When power-off 0 mode is not used.
4. When the power-on reset function is used.

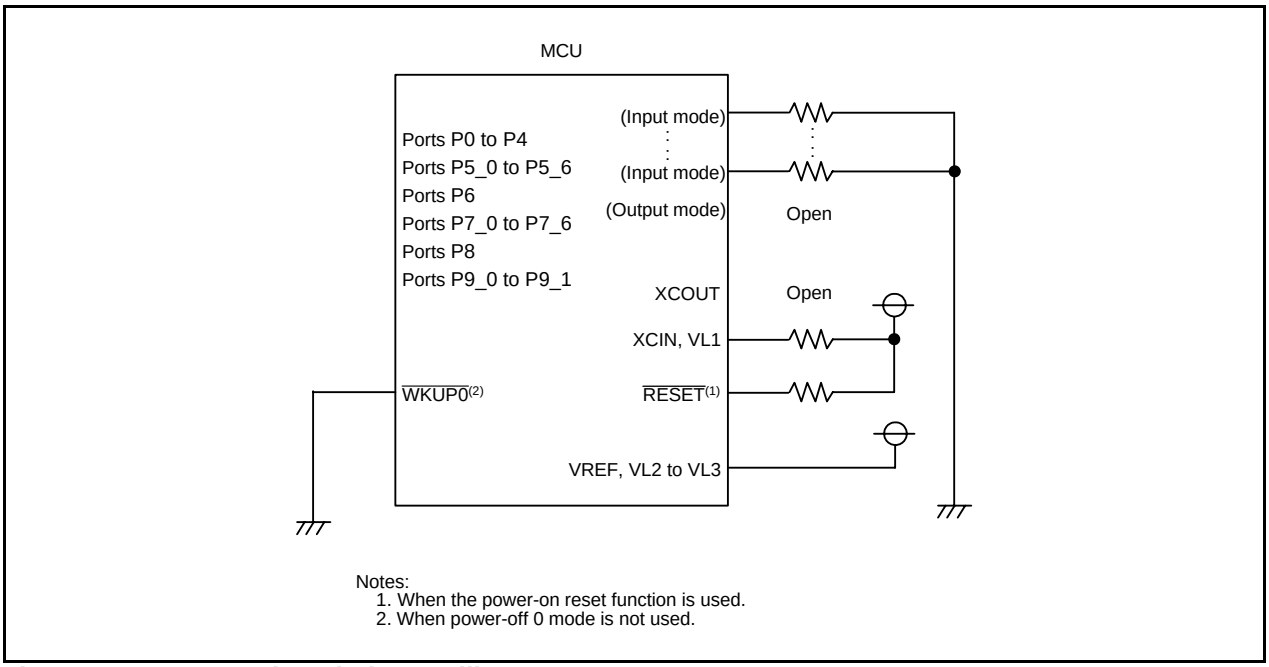


Figure 7.7 Unassigned Pin Handling

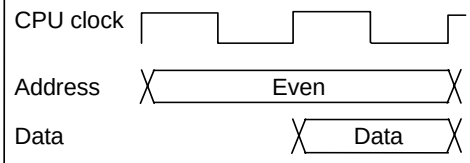
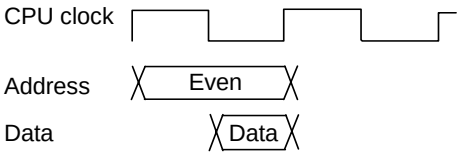
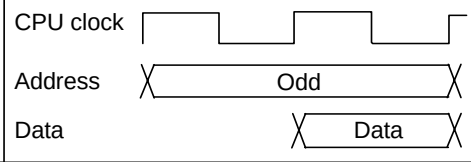
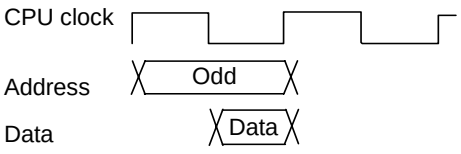
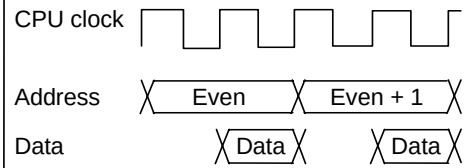
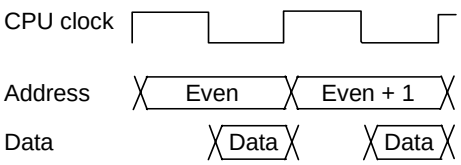
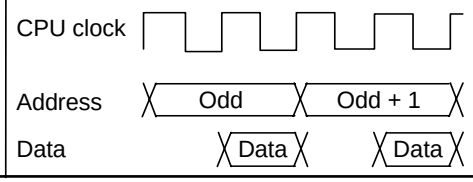
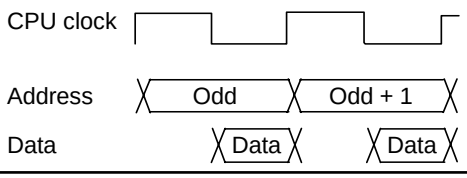
8. Bus

The bus cycles differ when accessing ROM/RAM and when accessing SFR.
Table 8.1 lists the Bus Cycles by Access Area.
ROM/RAM and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 8.2 shows Access Units and Bus Operations.

Table 8.1 Bus Cycles by Access Area

Access Area	Bus Cycle
SFR/Data flash	2 cycles of CPU clock
Program ROM/RAM	1 cycle of CPU clock

Table 8.2 Access Units and Bus Operations

Area	SFR, Data flash	ROM (program ROM), RAM
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Each interrupt control register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
Timer RJ: TRJi Registers (i = 0 to 2)
SSU: Registers SSTDR, SSTDRH, SSRDR, and SSRDRH
UART2: Registers U2MR, U2BRG, U2TB, U2C0, U2C1, U2RB, U2SMR5, U2SMR4, U2SMR3, U2SMR2, and U2SMR
A/D converter: Registers AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, ADMOD, ADINSEL, ADCON0, and ADCON1
Address match interrupt: Registers RMAD0, AIER0, RMAD1, and AIER1
Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Data flash, Even address Byte Access” in Table 8.2 Access Units and Bus Operations, and 16-bit data is accessed at a time.

9. Clock Generation Circuit

The following five circuits are incorporated in the clock generation circuit:
- XIN clock oscillation circuit
- XCIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator
- Low-speed on-chip oscillator for the watchdog timer

9.1 Introduction

Table 9.1 lists the Specification Overview of Clock Generation Circuit. Figure 9.1 shows the Clock Generation Circuit and Figure 9.2 shows the Peripheral Function Clock.

Table 9.1 Specification Overview of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	XCIN Clock Oscillation Circuit	On-Chip Oscillator		Low-Speed On-Chip Oscillator for Watchdog Timer
			High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator	
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• Watchdog timer clock source
Clock frequency	0 to 20 MHz	32.768 kHz	Approx. 20 MHz (2)	Approx. 125 kHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	• Crystal oscillator	–	–	–
Oscillator connect pins	XIN, XOUT (1)	XCIN, XCOUT	– (1)	– (1)	–
Oscillation stop, restart function	Usable	Usable	Usable	Usable	Usable
Oscillator status after reset	Stop	Oscillate	Stop	Oscillate	Stop (2) Oscillate (3)
Others	Externally generated clock can be input	• Externally generated clock can be input • On-chip feedback resistor Rf (connected/ not connected selectable)	–	–	–

Notes:
1. These pins can be used as P9_0 and P9_1 when using the on-chip oscillator clock as the CPU clock while the XIN clock oscillation circuit is not used.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
2. This applies when the CSPROINI bit in the OFS register is set to 1 (count source protection mode disabled after reset).
3. This applies when the CSPROINI bit in the OFS register is set to 0 (count source protection mode enabled after reset).

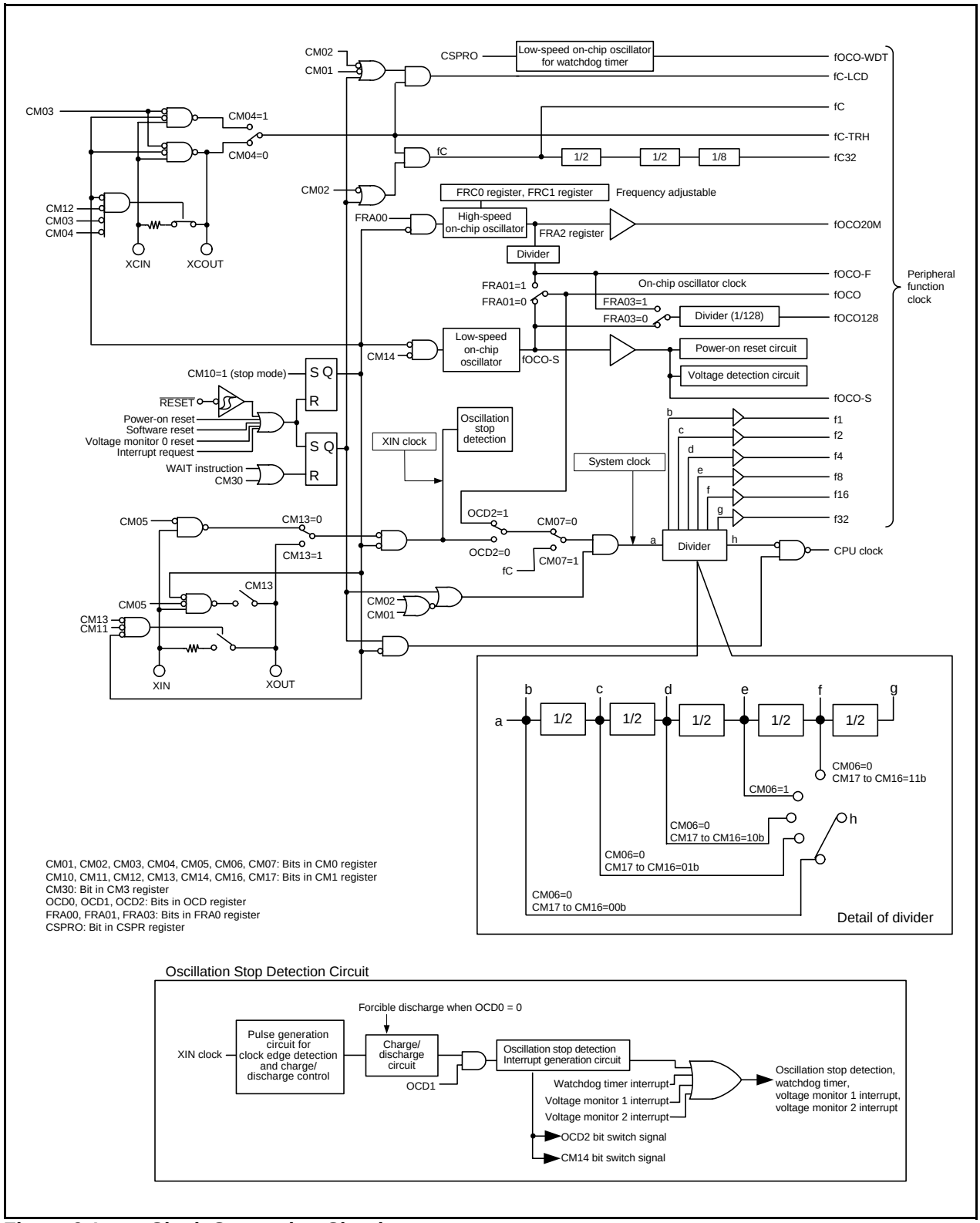


Figure 9.1 Clock Generation Circuit

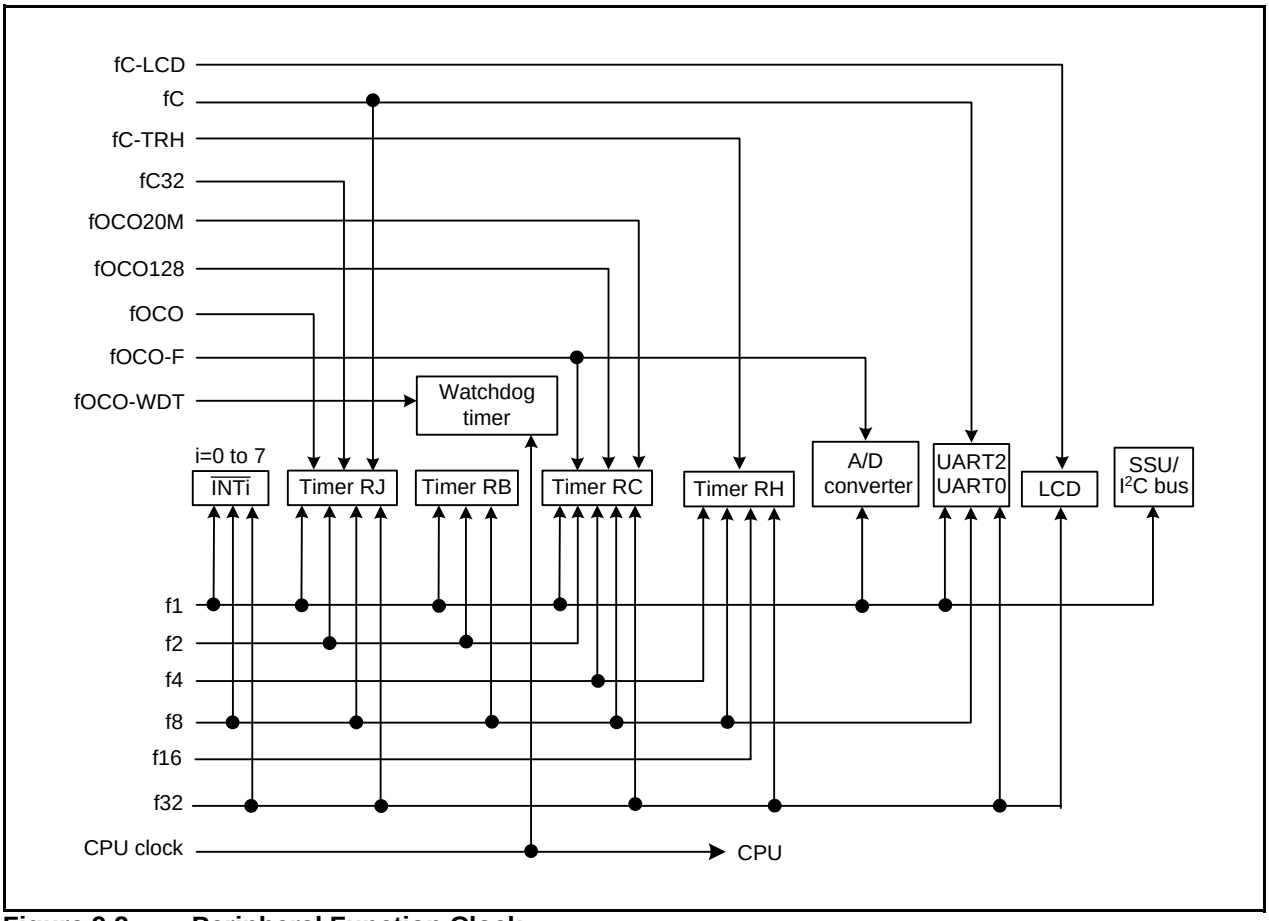


Figure 9.2 Peripheral Function Clock

9.2 Registers

9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	CM01	CM00
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM00	Power-off 2 mode transition enable bit	0: Disabled 1: Enabled	R/W
b1	CM01	Peripheral function clock stop bit in wait mode (6)	b1 b0 0 0: Peripheral function clock does not stop in wait mode 0 1: Clocks f1 to f32 stop in wait mode 1 0: Clocks f1 to f32 and fC stop in wait mode 1 1: Clocks f1 to f32, fC, and fC-LCD stop in wait mode	R/W
b2	CM02			R/W
b3	CM03	XCIN clock stop bit (5, 7)	0: XCIN clock oscillates 1: XCIN clock stops	R/W
b4	CM04	XCIN external clock input enable bit	0: External clock input disabled 1: External clock input enabled	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 2)	0: XIN clock oscillates 1: XIN clock stops	R/W
b6	CM06	CPU clock division select bit 0 (3)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	System clock select bit (4)	0: XIN clock or on-chip oscillator clock 1: XCIN clock	R/W

Notes:

1. The CM05 bit can be used to stop the XIN clock when the system clock is other than the XIN clock. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (a) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. Only when the CM05 bit to 1 (XIN clock stops) and the CM13 bit is set to 0 (I/O ports), P9_0 and P9_1 can be used as I/O ports.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
3. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
4. Set the CM07 bit to 1 (XCIN clock) from 0 after allowing the XCIN clock oscillation to stabilize.
5. To use the XCIN clock, set the CM03 bit to 1 once and then set it to 0 (XCIN clock oscillates) after turning on the power and exiting power-off 0.
6. When setting the CM00 bit to 1, set bits CM02 to CM01 to 11b.
7. When inputting an external clock, set the CM03 bit to 0 (XCIN clock oscillates).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 7, 8)	0: Clock oscillates 1: All clocks stop (stop mode/power-off 2 mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	XCIN-XCOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b3	CM13	Port/XIN-XOUT switch bit (5, 6)	0: I/O ports P9_0 and P9_1 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0, bits CM16 and CM17 are enabled.
2. When the CM10 bit is set to 1, the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. To use P9_0 and P9_1 as input ports, set the CM13 bit to 0 (I/O ports) and the CM05 bit in the CM0 register to 1 (XIN clock stops).
   To use as external clock input, set the CM13 bit to 0 (I/O ports), the CM05 bit to 0 (XIN clock oscillates), and the CM11 bit to 1 (on-chip feedback resistor disabled). When the PD9_0 bit in the PD9 register is further set to 0 (input mode), an external clock can be input. Set XOUT as the I/O port P9_1 at this time. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
6. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.
7. Do not set the CM10 bit to 1 when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).
8. When the CM00 bit in the CM0 register is 1 (enabled), the MCU enters power-off 2 mode.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

9.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division (2)	R/W
b6	CM36	System clock select bit when exiting wait, stop, or power-off 2 mode	b7 b6 0 0: MCU exits with the CPU clock used immediately before entering wait, stop, or power-off 2 mode 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (3) 1 1: XIN clock selected (4)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode or power-off 2 mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 to CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode, stop mode, or power-off 2 mode:
   • OCD2 bit in OCD register = 1 (on-chip oscillator selected)
   • FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
   • FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
4. When bits CM37 to CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode, stop mode, or power-off 2 mode.
   • OM05 bit in OM0 register = 1 (XIN clock oscillates)
   • OM13 bit in OM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0. However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock, XCIN clock, and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

9.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	On-chip oscillator clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
2. When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) when the XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. When the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even if 0 (XIN clock selected) is written to it.
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled).
5. The OCD3 bit remains 0 (XIN clock oscillates) when bits OCD1 to OCD0 are set to 00b.
6. Refer to **9.7.1 How to Use Oscillation Stop Detection Function** for the switching procedure when the XIN clock re-oscillates after detecting an oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

9.2.5 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected (3)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: fOCO-F divided by 128 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Notes:
1. Change the FRA01 bit under the following conditions.
   - FRA00 = 1 (high-speed on-chip oscillator on)
   - CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division mode can be set when VCC = 2.7 V to 5.5 V 000b to 111b
     Divide ratio of 4 or more when VCC = 1.8 V to 5.5 V 011b to 111b (divide-by-4 or more)
2. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA01 bit to 0 before setting the FRA00 bit to 0.
3. When setting the FRA01 bit to be 1 (high-speed on-chip oscillator selected) and stopping the low-speed on-chip oscillator, wait for one or more cycles of the low-speed on-chip oscillator and then set the CM14 bit in the CM1 register to 1 (low-speed on-chip oscillator off).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

9.2.6 High-Speed On-Chip Oscillator Frequency Control Register 0 (FRC0)

Address 0024h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be changed by the following settings. 20 MHz: FRC0 = value after a reset, FRC1 = value after a reset 18.432 MHz: Transfer the data of the FR18S0 register to the FRC0 register, and transfer the data of the FR18S1 register to the FRC1 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRC0 register.
Also, rewrite the FRC0 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).

9.2.7 High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 0025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	FRA22	FRA21	FRA20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switch bit	Division ratio selection	R/W
b1	FRA21		These bits select the division ratio for the high-speed on-chip oscillator clock.	R/W
b2	FRA22		b2 b1 b0 0 0 0: Divide-by-1 mode 0 0 1: Divide-by-2 mode 0 1 0: Divide-by-3 mode 0 1 1: Divide-by-4 mode 1 0 0: Divide-by-5 mode 1 0 1: Divide-by-6 mode 1 1 0: Divide-by-7 mode 1 1 1: Divide-by-8 mode	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA2 register.

9.2.8 High-Speed On-Chip Oscillator 18 MHz Set Value Register 0 (FR18S0)

Address 0029h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7-b0	18.432 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRC0 register and by transferring the correction value of the FR18S1 register to the FRC1 register.	R

9.2.9 High-Speed On-Chip Oscillator 18 MHz Set Value Register 1 (FR18S1)

Address 002Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7-b0	18.432 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRC1 register and by transferring the correction value of the FR18S0 register to the FRC0 register.	R

9.2.10 High-Speed On-Chip Oscillator Control Register 1 (FRC1)

Address 002Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

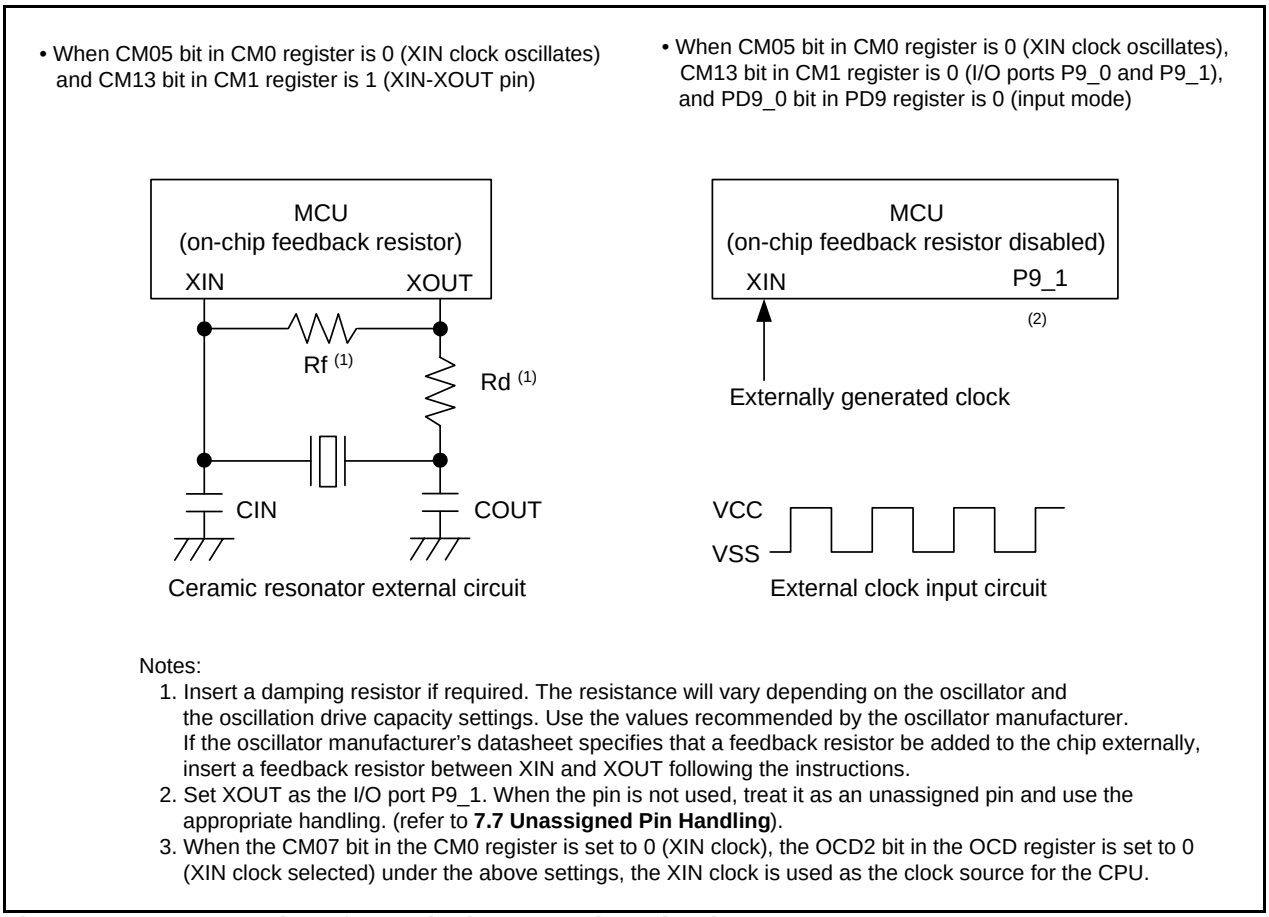
Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 20 MHz: FRC0 = value after a reset, FRC1 = value after a reset 18.432 MHz: Transfer the value in the FRC0 register to the FRC1 register and the value in the FR18S1 register to the FRC1 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRC1 register.
Also, rewrite the FRC1 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).

The clocks generated by the clock generation circuits are described below.

9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a oscillator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XIN pin.
Figure 9.3 shows Examples of XIN Clock Connection Circuit.
During and after reset, the XIN clock stops.
After setting the CM13 bit in the CM1 register to 1 (XIN-XOUT pin), the XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates).
After the XIN clock oscillation stabilizes, the XIN clock is used as the CPU clock source by setting the OCD2 bit in the OCD register to 0 (XIN clock selected).
The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) by setting the OCD2 bit is to 1 (on-chip oscillator clock selected).
When switching the XIN clock to an externally generated clock, or an externally generated clock to the XIN clock, set the CM05 bit to 1 (XIN clock stops).
In stop mode, all clocks including the XIN clock stop. Refer to **10. Power Control** for details.


• When CM05 bit in CM0 register is 0 (XIN clock oscillates) and CM13 bit in CM1 register is 1 (XIN-XOUT pin)
MCU
(on-chip feedback resistor)
XIN
XOUT
Rf (1)
Rd (1)
CIN
COUT
Ceramic resonator external circuit
• When CM05 bit in CM0 register is 0 (XIN clock oscillates), CM13 bit in CM1 register is 0 (I/O ports P9_0 and P9_1), and PD9_0 bit in PD9 register is 0 (input mode)
MCU
(on-chip feedback resistor disabled)
XIN
P9_1
(2)
Externally generated clock
VCC
VSS
External clock input circuit

Notes:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity settings. Use the values recommended by the oscillator manufacturer. If the oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.
2. Set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling. (refer to **7.7 Unassigned Pin Handling**).
3. When the CM07 bit in the CM0 register is set to 0 (XIN clock), the OCD2 bit in the OCD register is set to 0 (XIN clock selected) under the above settings, the XIN clock is used as the clock source for the CPU.

Figure 9.3 Examples of XIN Clock Connection Circuit

9.4 On-Chip Oscillator Clock

The on-chip oscillator clock is supplied by the on-chip oscillator (high-speed on-chip oscillator or low-speed on-chip oscillator). This clock is selected by the FRA01 bit in the FRA0 register.

9.4.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, and peripheral function clock (fOCO, fOCO-S, and fOCO128).
After a reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 1 (no division) is selected as the CPU clock.
If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating and supplies the necessary clock for the MCU.
The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

9.4.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, and peripheral function clock (fOCO, fOCO-F, fOCO20M, and fOCO128).
To use the high-speed on-chip oscillator clock as the clock source for the CPU clock, peripheral clock, fOCO, and fOCO-F, set bits FRA20 to FRA22 in the FRA2 register as follows:

- All division mode can be set when VCC = 2.7 V to 5.5 V — 000b to 111b
- Divide ratio of 4 or more when VCC = 1.8 V to 5.5 V — 011b to 111b (divide by 4 or more)

After a reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. Oscillation is started by setting the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on).

Frequency correction data is stored in registers FR18S0 and FR18S1.
To adjust the frequency of the high-speed on-chip oscillator clock to 18.432 MHz, first transfer the correction value of the FR18S0 register to the FRC0 register and the correction value of the FR18S1 register to the FRC1 register before using the values. This enables the bit rates such as 9,600 bps and 38,400 bps to be used when the serial interface is used in UART mode (refer to **Table 21.8** and **Table 22.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)**).

9.5 XCIN Clock

The XCIN clock is supplied by the XCIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XCIN clock oscillation circuit is configured by connecting a crystal oscillator between pins XCIN and XCOUT. The XCIN clock oscillation circuit includes an on-chip a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XCIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XCIN pin.

Figure 9.4 shows Examples of XCIN Clock Connection Circuits.

Bits CM04 to CM03 in the CM0 register are set to 00b (external clock input disabled, XCIN clock oscillates) by reset and the XCIN clock starts oscillating (with the on-chip feedback resistor enabled). After the XCIN clock oscillation stabilizes following reset, the XCIN clock is used as the CPU clock source by setting the CM07 bit in the CM07 register to 1 (XCIN clock).

When the CM03 bit is set to 1 (XCIN clock stops), the XCIN clock stops.

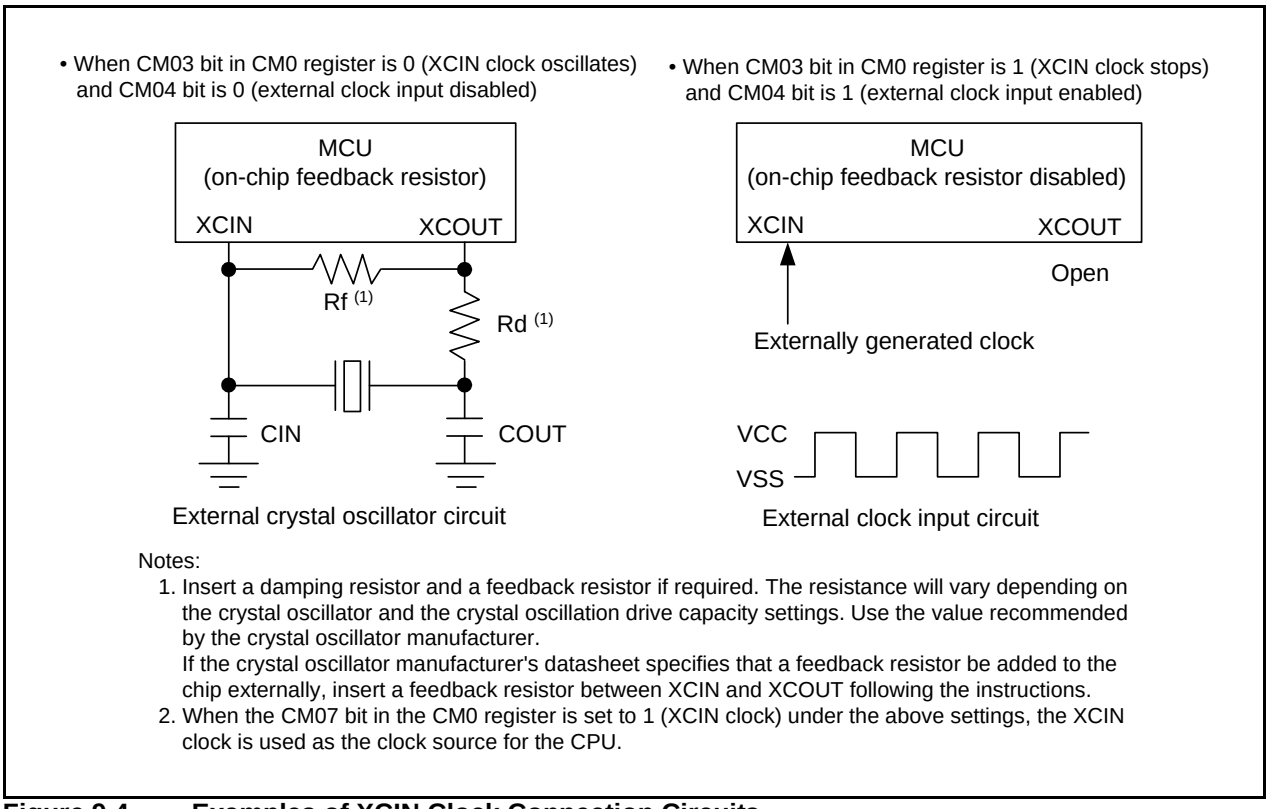
When bits CM04 to CM03 are set to 10b (external clock input enabled, XCIN clock oscillates), an externally generated clock can also be input to the XCIN pin. Leave the XCOUT pin open at this time.

This MCU has an on-chip feedback resistor, which can be disabled/enabled by the CM12 bit in the CM1 register.

To use the XCIN clock, set the CM03 bit to 1 once and then set it to 0 (XCIN clock oscillates).

When the XCIN clock is not used, set bits CM04 to CM03 to 01b (external clock input disabled, XCIN clock stops) and the CM12 bit to 1 (on-chip feedback resistor disabled).

In stop mode, all clocks including the XCIN clock stop. Refer to **10. Power Control** for details.



Notes:
1. Insert a damping resistor and a feedback resistor if required. The resistance will vary depending on the crystal oscillator and the crystal oscillation drive capacity settings. Use the value recommended by the crystal oscillator manufacturer.
   If the crystal oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XCIN and XCOUT following the instructions.
2. When the CM07 bit in the CM0 register is set to 1 (XCIN clock) under the above settings, the XCIN clock is used as the clock source for the CPU.

Figure 9.4 Examples of XCIN Clock Connection Circuits

9.6 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. (Refer to **Figure 9.1 Clock Generation Circuit**.)

9.6.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. The XIN clock, XCIN clock, or on-chip oscillator clock can be selected.

9.6.2 CPU Clock

The CPU clock is an operating clock for the CPU and the watchdog timer.
The system clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. The division ratio can be selected by the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register.
Use the XCIN clock while the XCIN clock oscillation stabilizes.
After a reset, the low-speed on-chip oscillator clock divided by 1 (no division) is used as the CPU clock.
When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 in CM0 register and bits CM16 and CM17 in CM1 register enabled).

9.6.3 Peripheral Function Clock (f1, f2, f4, f8, f16, and f32)

The peripheral function clock is an operating clock for the peripheral functions.
The fi (i = 1, 2, 4, 8, 16, and 32) clock is generated by the system clock divided by i. It is used for timers RJ, RB, RC, RH, the serial interface, the A/D converter, and the LCD waveform control circuit.
When the MCU enters wait mode after bits CM02 to CM01 in the CM0 register are set to 01, 10, or 11, the fi clock stops.

9.6.4 fOCO

fOCO is an operating clock for the peripheral functions.
This clock runs at the same frequency as the on-chip oscillator clock and can be used as the source for timer RJ.
In wait mode, the fOCO clock does not stop.

9.6.5 fOCO20M

fOCO20M is used as the count source for timer RC.
This clock is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO20M clock does not stop.
This clock can be used with supply voltage VCC = 3.0 to 5.5 V.

9.6.6 fOCO-F

fOCO-F is used as the count source for timers RC and RD, and the A/D converter.
This clock is generated by the high-speed on-chip oscillator, divided by i (i = 1, 2, 3, 4, 5, 6, 7, or 8; division ratio selected by the FRA2 register). It is supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO-F clock does not stop.

9.6.7 fOCO-S

fOCO-S is an operating clock for the voltage detection circuit.
This clock is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on).
In wait mode, the fOCO-S clock does not stop.

9.6.8 fOCO128

fOCO128 clock is generated by fOCO-S or fOCO-F divided by 128. fOCO-S divided by 128 is selected by setting the FRA03 bit to 0 and fOCO-F divided by 128 is selected by setting the FRA03 bit to 1.
fOCO128 is configured as the capture signal used in the TRCGRA register for timer RC.

9.6.9 fC-LCD

fC-LCD is used in the LCD waveform control circuit.
Use this clock only while the XCIN clock oscillation stabilizes.

9.6.10 fC and fC32

fC and fC32 are used for timers RJ, RH and the serial interface.
Use theses clocks while the XCIN clock oscillation stabilizes.

9.6.11 fOCO-WDT

fOCO-WDT is an operating clock for the watchdog timer.
This clock is generated by the low-speed on-chip oscillator for the watchdog timer and supplied by setting the CSPRO bit in the CSPR register to 1 (count source protection mode enabled).
In count source protection mode for the watchdog timer, the fOCO-WDT clock does not stop.

9.6.12 fC-TRH

fC-TRH is used as the count source for timer RH.
Use this clock while the XCIN clock oscillation stabilizes.

9.7 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit.
The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 9.2 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the MCU is placed in the following states if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on)
- Oscillation stop detection interrupt request is generated

Table 9.2 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation stop detection clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Condition for enabling the oscillation stop detection function	Bits OCD1 to OCD0 are set to 11b.
Operation at oscillation stop detection	Oscillation stop detection interrupt generation

9.7.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the voltage monitor 1 interrupt, the voltage monitor 2 interrupt, and the watchdog timer interrupt. To use the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.
  Table 9.3 lists the Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt. Figure 9.6 shows an Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.5 shows the Procedure for Switching Low-Speed On-Chip Oscillator to XIN Clock.
- To enter wait mode while the oscillation stop detection function is used, set bits CM02 to CM1 to 00 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b to stop or start the XIN clock by a program (select stop mode or change the CM05 bit).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, set the FRA01 bit in the FRA0 register to 0 (low-speed on-chip oscillator selected) and then bits OCD1 to OCD0 to 11b.
  To use the high-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, first set the FRA00 bit to 1 (high-speed on-chip oscillator on) and the FRA01 bit to 1 (high-speed on-chip oscillator selected). Then set bits OCD1 to OCD0 to 11b.

Table 9.3 Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection (when (a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) Bits OCD1 to OCD0 in OCD register = 11b and OCD2 bit = 1
Watchdog timer	VW2C3 bit in VW2C register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1
Voltage monitor 2	VW2C2 bit in VW2C register = 1

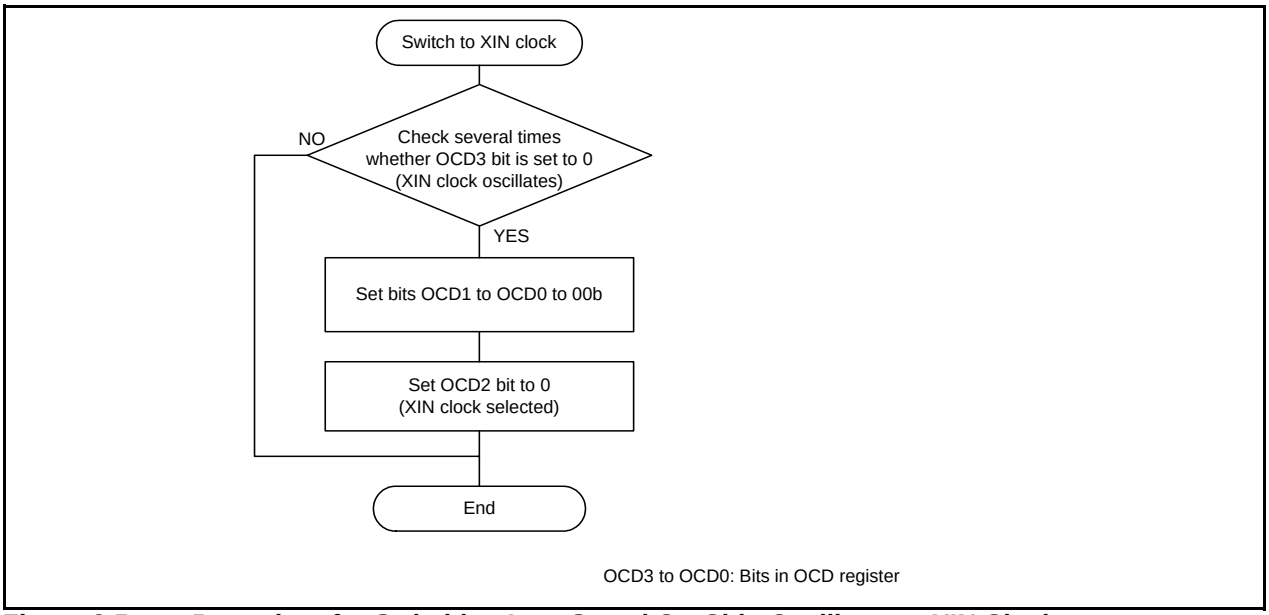

Switch to XIN clock
Check several times whether OCD3 bit is set to 0 (XIN clock oscillates)
NO
YES
Set bits OCD1 to OCD0 to 00b
Set OCD2 bit to 0 (XIN clock selected)
End
OCD3 to OCD0: Bits in OCD register

Figure 9.5 Procedure for Switching Low-Speed On-Chip Oscillator to XIN Clock

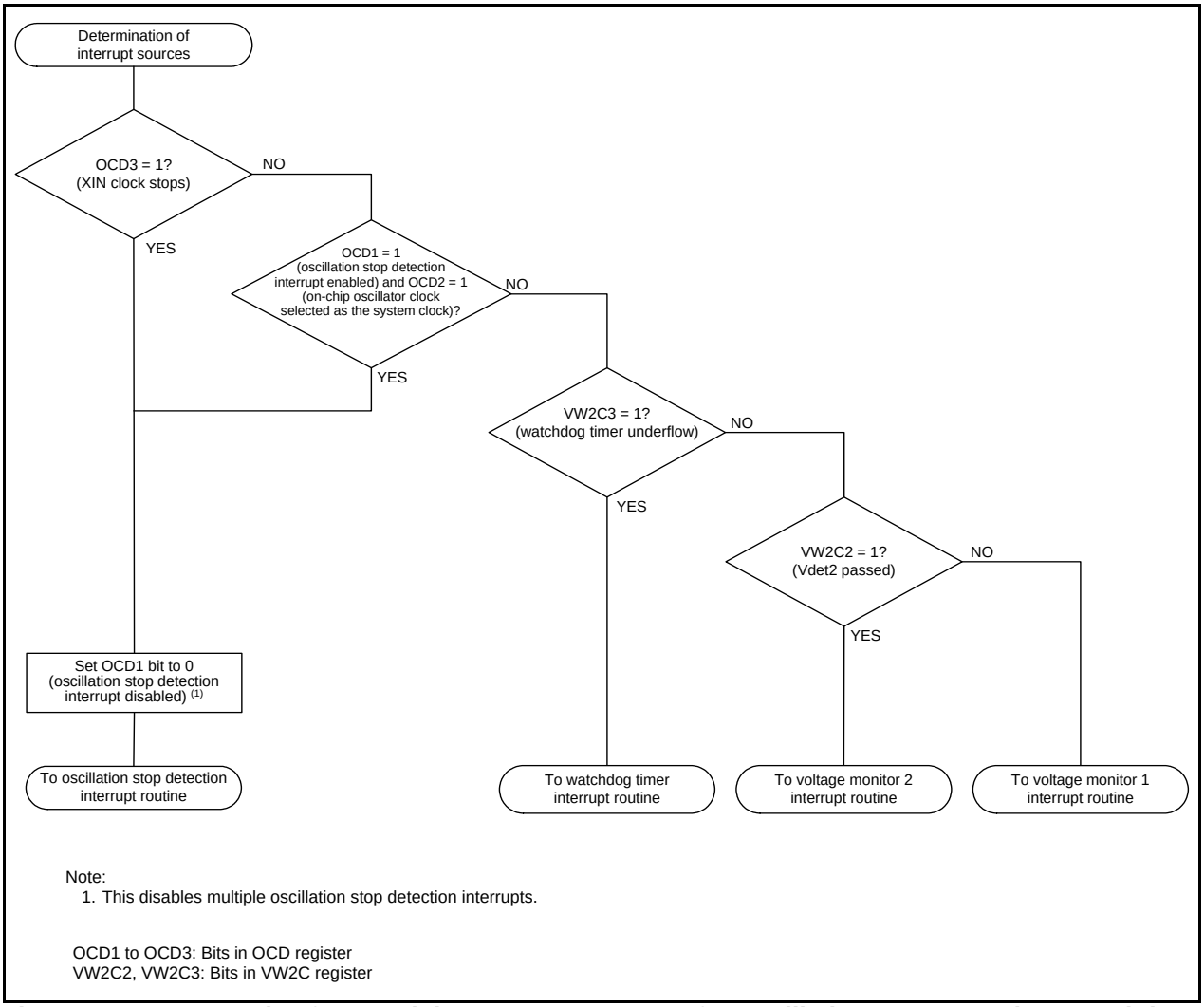

Determination of interrupt sources
OCD3 = 1? (XIN clock stops)
NO
YES
OCD1 = 1 (oscillation stop detection interrupt enabled) and OCD2 = 1 (on-chip oscillator clock selected as the system clock)?
NO
YES
VW2C3 = 1? (watchdog timer underflow)
NO
YES
VW2C2 = 1? (Vdet2 passed)
NO
YES
Set OCD1 bit to 0 (oscillation stop detection interrupt disabled) (1)
To oscillation stop detection interrupt routine
To watchdog timer interrupt routine
To voltage monitor 2 interrupt routine
To voltage monitor 1 interrupt routine
Note:
1. This disables multiple oscillation stop detection interrupts.
OCD1 to OCD3: Bits in OCD register
VW2C2, VW2C3: Bits in VW2C register

Figure 9.6 Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

9.8 Notes on Clock Generation Circuit

9.8.1 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b.

9.8.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

9.8.3 XCIN Clock

To use the XCIN clock, set the CM03 bit to 1 once and then set it to 0 (XCIN clock oscillates).

10. Power Control

10.1 Introduction

There are four power control modes. The states other than wait mode, stop mode, power-off 0 mode, and power-off 2 mode are referred to as standard operating mode here.
Table 10.1 lists each mode. Figure 10.1 shows the State Transitions in Power Control Mode.

Table 10.1 Power Control

Mode		Operation
Standard operating mode	High-speed clock	The CPU and peripheral functions operate.
	High-speed on-chip oscillator	
	Low-speed clock	The CPU and peripheral functions operate.
	Low-speed on-chip oscillator	
Wait mode		The CPU stops and peripheral functions operate.
Stop mode		The CPU stops and peripheral functions other than the watchdog timer stop (oscillation off).
Power-off 0 mode		The CPU stops and all peripheral functions stop (oscillation off), the contents of RAM and SFRs are not retained.
Power-off 2 mode		The CPU stops and peripheral functions other than the watchdog timer and timer RH stop, the contents of RAM and SFRs are retained.

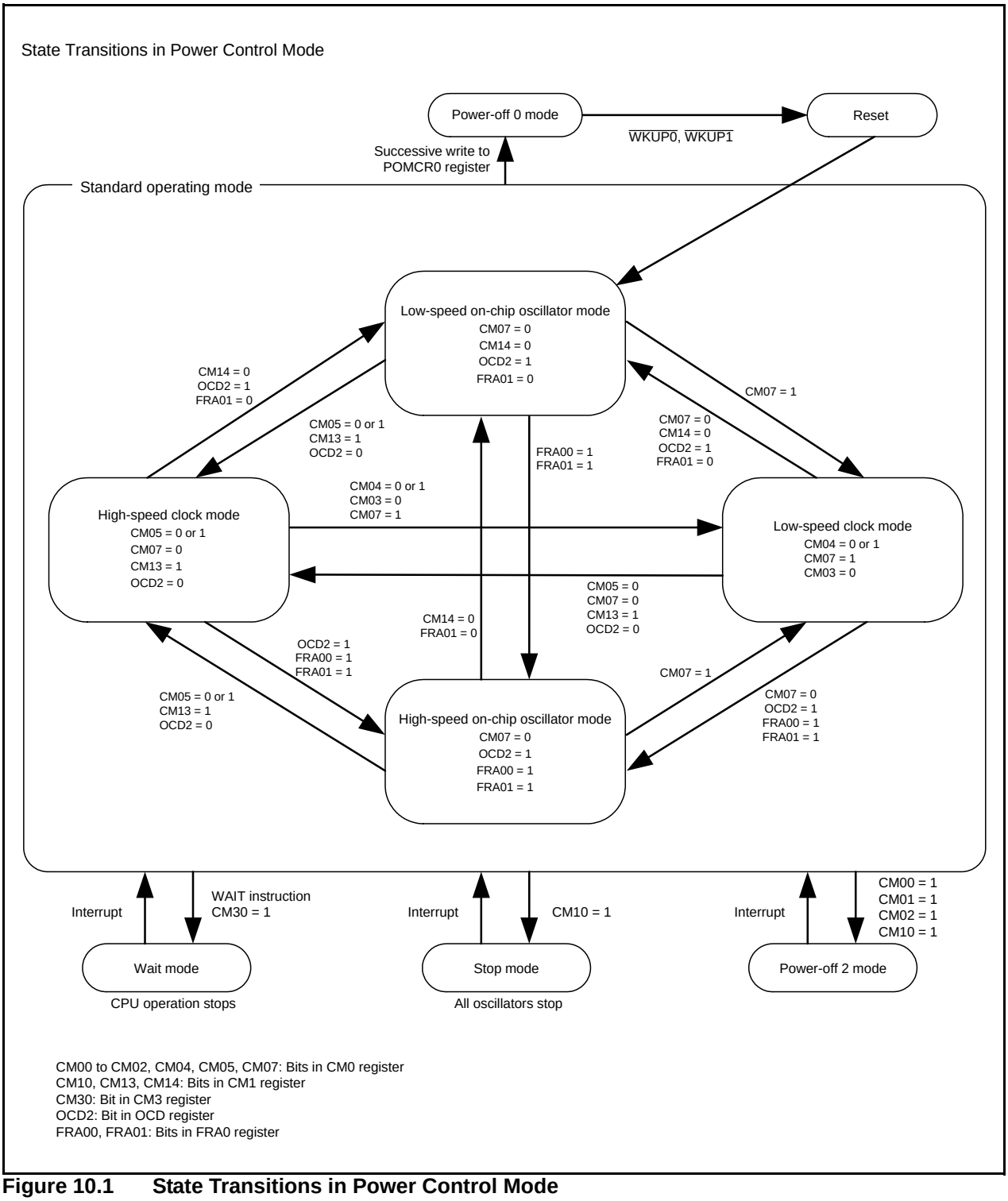


Figure 10.1 State Transitions in Power Control Mode

10.2 Registers

10.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	CM01	CM00
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM00	Power-off 2 mode transition enable bit	0: Disabled 1: Enabled	R/W
b1	CM01	Peripheral function clock stop bit in wait mode (6)	b1 b0 0 0: Peripheral function clock does not stop in wait mode 0 1: Clocks f1 to f32 stop in wait mode 1 0: Clocks f1 to f32 and fC stop in wait mode 1 1: Clocks f1 to f32, fC, and fC-LCD stop in wait mode	R/W
b2	CM02			R/W
b3	CM03	XCIN clock stop bit (5, 7)	0: XCIN clock oscillates 1: XCIN clock stops	R/W
b4	CM04	XCIN external clock input enable bit	0: External clock input disabled 1: External clock input enabled	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 2)	0: XIN clock oscillates 1: XIN clock stops	R/W
b6	CM06	CPU clock division select bit 0 (3)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	System clock select bit (4)	0: XIN clock or on-chip oscillator clock 1: XCIN clock	R/W

Notes:

1. The CM05 bit can be used to stop the XIN clock when the system clock is other than the XIN clock. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (a) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. Only when the CM05 bit to 1 (XIN clock stops) and the CM13 bit is set to 0 (I/O ports), P9_0 and P9_1 can be used as I/O ports.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
3. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
4. Set the CM07 bit to 1 (XCIN clock) from 0 after allowing the XCIN clock oscillation to stabilize.
5. To use the XCIN clock, set the CM03 bit to 1 once and then set it to 0 (XCIN clock oscillates) after turning on the power and exiting power-off 0.
6. When setting the CM00 bit to 1, set bits CM02 to CM01 to 11b.
7. When inputting an external clock, set the CM03 bit to 0 (XCIN clock oscillates).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

10.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 7, 8)	0: Clock oscillates 1: All clocks stop (stop mode/power-off 2 mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	XCIN-XCOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b3	CM13	Port/XIN-XOUT switch bit (5, 6)	0: I/O ports P9_0 and P9_1 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0, bits CM16 and CM17 are enabled.
2. When the CM10 bit is set to 1, the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. To use P9_0 and P9_1 as input ports, set the CM13 bit to 0 (I/O ports) and the CM05 bit in the CM0 register to 1 (XIN clock stops).
   To use as external clock input, set the CM13 bit to 0 (I/O ports), the CM05 bit to 0 (XIN clock oscillates), and the CM11 bit to 1 (on-chip feedback resistor disabled). When the PD9_0 bit in the PD9 register is further set to 0 (input mode), an external clock can be input. Set XOUT as the I/O port P9_1 at this time. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
   The P9_0 pin is shared with the XIN pin, and the P9_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
6. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.
7. Do not set the CM10 bit to 1 when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).
8. When the CM00 bit in the CM0 register is 1 (enabled), the MCU enters power-off 2 mode.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

10.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division (2)	R/W
b6	CM36	System clock select bit when exiting wait, stop, or power-off 2 mode	b7 b6 0 0: MCU exits with the CPU clock used immediately before entering wait, stop, or power-off 2 mode 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (3) 1 1: XIN clock selected (4)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode or power-off 2 mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 to CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode, stop mode, or power-off 2 mode:
   • OCD2 bit in OCD register = 1 (on-chip oscillator selected)
   • FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
   • FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
4. When bits CM37 to CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode, stop mode, or power-off 2 mode.
   • OM05 bit in OM0 register = 1 (XIN clock oscillates)
   • OM13 bit in OM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0. However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock, XCIN clock, and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

10.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	On-chip oscillator clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
2. When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) when the XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. When the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even if 0 (XIN clock selected) is written to it.
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled).
5. The OCD3 bit remains 0 (XIN clock oscillates) when bits OCD1 to OCD0 are set to 00b.
6. Refer to **9.7.1 How to Use Oscillation Stop Detection Function** for the switching procedure when the XIN clock re-oscillates after detecting an oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

10.2.5 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected (3)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: fOCO-F divided by 128 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Notes:

1. Change the FRA01 bit under the following conditions.
   - FRA00 = 1 (high-speed on-chip oscillator on)
   - CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division mode can be set when VCC = 2.7 V to 5.5 V 000b to 111b
     Divide ratio of 4 or more when VCC = 1.8 V to 5.5 V 011b to 111b (divide-by-4 or more)
2. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA01 bit to 0 before setting the FRA00 bit to 0.
3. When setting the FRA01 bit to be 1 (high-speed on-chip oscillator selected) and stopping the low-speed on-chip oscillator, wait for one or more cycles of the low-speed on-chip oscillator and then set the CM14 bit in the CM1 register to 1 (low-speed on-chip oscillator off).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

10.2.6 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.7 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1.
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

10.2.7 Power-Off Mode Control Register 0 (POMCR0)

Address 0020h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POM07	POM06	POM05	POM04	POM03	POM02	POM01	POM00
After Reset	X	X	X	X	X	X	0	0

Initial write: Setting the input pin to exit the mode in power-off 0 mode

Bit	Symbol	Bit Name	Function	R/W
b0	POM00	Reserved bit	Set to 0.	W
b1	POM01	$\overline{\text{WKUP1}}$ input enable bit	0: Input disabled 1: Input enabled	W
b2	POM02	Reserved bits	Set to 0.	W
b3	POM03			
b4	POM04			
b5	POM05			
b6	POM06			
b7	POM07			

Second to fifth write: Entering power-off 0 mode

Bit	Function	R/W
b7 to b0	Write 88h, 15h, 92h, and 25h successively.	W

Read

Bit	Symbol	Bit Name	Function	R/W
b0	POM00	$\overline{\text{WKUP0}}$ source power-off 0 exit flag	0: Undetected 1: Detected	R
b1	POM01	$\overline{\text{WKUP1}}$ source power-off 0 exit flag	0: Undetected 1: Detected	R
b2	—	Nothing is assigned. When read, the content is undefined.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. Write to the POMCR0 register five times successively to enter power-off 0 mode.

Table 10.2 POMCR0 Register Values After Exiting Power-Off 0 Mode

Power-off 0 mode exit source	POM07	POM06	POM05	POM04	POM03	POM02	POM01	POM00
$\overline{\text{WKUP0}}$ source	X	X	X	X	X	X	0	1
$\overline{\text{WKUP1}}$ source	X	X	X	X	X	X	1	0

10.3 Standard Operating Mode

Table 10.3 lists the Clock Selection in Standard Operating Mode.

In standard operating mode, the CPU and peripheral function clocks are supplied to operate the CPU and the peripheral functions. Power control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. If unnecessary oscillator circuits stop, power consumption is further reduced.

Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. Allow sufficient wait time in a program until oscillation stabilizes before switching the clock.

Table 10.3 Clock Selection in Standard Operating Mode

Modes		OCD Register	CM1 Register				CM0 Register					FRA0 Register	
		OCD2	CM17	CM16	CM14	CM13	CM07	CM06	CM05	CM04	CM03	FRA01	FRA00
High-speed clock mode	No division	0	0	0	—	1	0	0	0 or 1	—	—	—	—
	Divide-by-2	0	0	1	—	1	0	0	0 or 1	—	—	—	—
	Divide-by-4	0	1	0	—	1	0	0	0 or 1	—	—	—	—
	Divide-by-8	0	—	—	—	1	0	1	0 or 1	—	—	—	—
	Divide-by-16	0	1	1	—	1	0	0	0 or 1	—	—	—	—
Low-speed clock mode	No division	—	0	0	—	—	1	0	—	0 or 1	0	—	—
	Divide-by-2	—	0	1	—	—	1	0	—	0 or 1	0	—	—
	Divide-by-4	—	1	0	—	—	1	0	—	0 or 1	0	—	—
	Divide-by-8	—	—	—	—	—	1	1	—	0 or 1	0	—	—
	Divide-by-16	—	1	1	—	—	1	0	—	0 or 1	0	—	—
High-speed on-chip oscillator mode	No division	1	0	0	—	—	0	0	—	—	—	1	1
	Divide-by-2	1	0	1	—	—	0	0	—	—	—	1	1
	Divide-by-4	1	1	0	—	—	0	0	—	—	—	1	1
	Divide-by-8	1	—	—	—	—	0	1	—	—	—	1	1
	Divide-by-16	1	1	1	—	—	0	0	—	—	—	1	1
Low-speed on-chip oscillator mode	No division	1	0	0	0	—	0	0	—	—	—	0	—
	Divide-by-2	1	0	1	0	—	0	0	—	—	—	0	—
	Divide-by-4	1	1	0	0	—	0	0	—	—	—	0	—
	Divide-by-8	1	—	—	0	—	0	1	—	—	—	0	—
	Divide-by-16	—	1	1	0	—	0	0	—	—	—	0	—

—: Indicates that either 0 or 1 can be set.

10.3.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. When the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on), fOCO can be used for timer RJ.
Also, when the FRA00 bit is set to 1, fOCO20M can be used for timer RC.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

10.3.2 Low-Speed Clock Mode

The XCIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock.
In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). When the CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8, low-current-consumption read mode can be used. However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
Also, if the FRA00 bit is set to 1, fOCO20M can be used for timer RC.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
To enter wait mode from low-speed clock mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **10.8 Reducing Power Consumption**.

10.3.3 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 1. The on-chip oscillator divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. When the FRA00 bit is set to 1, fOCO20M can be used for timer RC.
Also, when the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

10.3.4 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 0, the low-speed on-chip oscillator is used as the on-chip oscillator clock. At this time, the on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. When the FRA00 bit is set to 1, fOCO20M can be used for timer RC.
Also, When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-current-consumption read mode can be used. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
To enter wait mode from low-speed clock mode, lower consumption current in wait mode can be further reduced by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **10.8 Reducing Power Consumption**.

10.4 Wait Mode

Since the CPU clock stops in wait mode, CPU operation using the CPU clock and watchdog timer operation with count source protection mode disabled are halted. However, the XIN clock, XCIN clock, and on-chip oscillator clock do not stop, so peripheral functions using these clocks continue operating.

10.4.1 Peripheral Function Clock Stop Function

The peripheral function clock to stop in wait mode can be selected by setting bits CM01 and CM02 in the CM0 register (peripheral function clock stop bits in wait mode). This controls power consumption according to applications.

10.4.2 Entering Wait Mode

The MCU enters wait mode by executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).

When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).

If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.

Enter wait mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

10.4.3 Pin Status in Wait Mode

Each I/O port retains its states immediately before the MCU enters wait mode.

10.4.4 Exiting Wait Mode

The MCU exits wait mode by a reset or peripheral function interrupt. The peripheral function interrupts are affected by bits CM01 and CM02.

Table 10.4 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 to CM01 = 00b	CM02 to CM01 = 01b	CM02 to CM01 = 10b	CM02 to CM01 = 11b
Serial interface interrupt	Usable when operating with an internal or external clock.	Usable when operating with fC or an external clock.	Usable when operating with an external clock.	Usable when operating with an external clock.
Synchronous serial communication unit interrupt/I^2C bus interface interrupt	Usable in all modes.	(Do not use.)	(Do not use.)	(Do not use.)
Key input interrupt	Usable	Usable	Usable	Usable
A/D conversion interrupt	(Do not use.)	(Do not use.)	(Do not use.)	(Do not use.)
Timer RJ interrupt	Usable in all modes.	Usable if there is no filter in event counter mode. Usable by selecting fOCO, fC, or fC32 as the count source.	Usable if there is no filter in event counter mode. Usable by selecting fOCO as the count source.	Usable if there is no filter in event counter mode. Usable by selecting fOCO as the count source.
Timer RB interrupt	Usable in all modes.	(Do not use.)	Usable by selecting fOCO as timer RJ count source and timer RJ underflow as timer RB count source	Usable by selecting fOCO as timer RJ count source and timer RJ underflow as timer RB count source
Timer RC interrupt	Usable in all modes.	(Do not use.)	(Do not use.)	(Do not use.)
Timer RH interrupt	Usable in all modes.	Usable when operating in real time clock mode.	Usable when operating in real time clock mode.	Usable when operating in real time clock mode.
$\overline{INT}$ interrupt	Usable	Usable if there is no filter.	Usable if there is no filter.	Usable if there is no filter.
Voltage monitor 1 interrupt	Usable	Usable	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable	Usable	Usable
Oscillation stop detection interrupt	Usable	(Do not use.)	(Do not use.)	(Do not use.)

The following interrupts can be used to exit wait mode:

- When bits CM02 to CM01 are set to 00b (peripheral function clock does not stop in wait mode), peripheral function interrupts other than A/D conversion interrupts.
- When bits CM02 to CM01 are set to 01b (clocks f1 to f32 stop in wait mode), the interrupts of the peripheral functions operating with external signals, the on-chip oscillator clock, or clocks fC1 to f32.
- When bits CM02 to CM01 are set to 10b (clocks f1 to f32 and fC stop in wait mode), the interrupts of the peripheral functions operating with external signals or the on-chip oscillator clock.
- When bits CM02 to CM01 are set to 11b (clocks f1 to f32, fC, and fC-LCD stop in wait mode), the same applies when bits CM02 to CM01 are set to 10b.

Table 10.4 lists Interrupts to Exit Wait Mode and Usage Conditions.

Figure 10.2 shows the Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).
To use a peripheral function interrupt to exit wait mode, set up the following before setting the CM30 bit to 1.
(1) Set the I flag to 0 (maskable interrupt disabled)
(2) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 10.2.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register	VCA2 Register	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Remarks
FMSTP Bit	VCA20 Bit				
0 (flash memory operates)	0 (internal power low consumption disabled)	100 μs (max.)	Period of system clock × 1 cycle	Period of CPU clock × 2 cycles	The total of T0 to T2 is the time from wait mode to first instruction execution following exit.
	1 (internal power low consumption enabled)	100 μs (max.)			
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)			

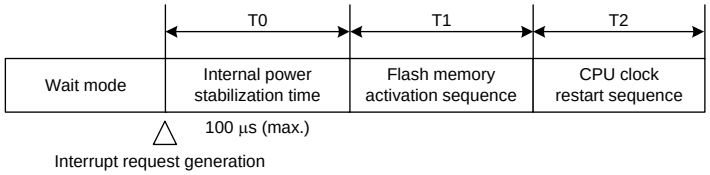


Figure 10.2 Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

Figure 10.3 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed.
To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 10.3.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register / FMSTP Bit	VCA2 Register / VCA20 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	100 μs (max.)	Period of system clock × 1 cycle	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode until an interrupt routine is executed.
	1 (internal power low consumption enabled)	100 μs (max.)				
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Same as above	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)				

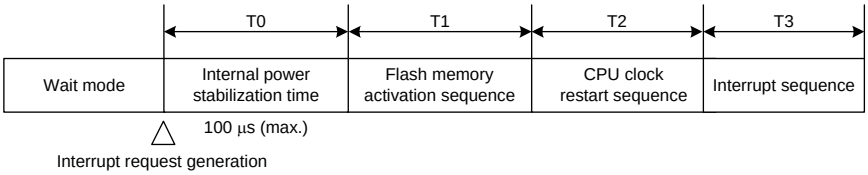


Figure 10.3 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

10.5 Stop Mode

All oscillator circuits except fOCO-WDT stop in stop mode. Since the CPU clock and the peripheral function clock stop, CPU operation and peripheral function operation using these clocks are halted. If the voltage applied to the VCC pin is VRAM or more, the content of internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 10.5 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 10.5 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	Usable
$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$ interrupt	Usable if there is no filter.
Timer RJ interrupt	Usable if there is no filter when an external pulse is counted in event counter mode.
Serial interface interrupt	When an external clock is selected.
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (the VW1C1 bit in the VW1C register is set to 1).
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (the VW2C1 bit in the VW2C register is set to 1).

10.5.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 after the CM00 bit in the CM0 register is set to 0. At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use stop mode, set the following before the MCU enters stop mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

Enter stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

10.5.2 Pin Status in Stop Mode

Each I/O port retains its state before the MCU enters stop mode.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pin), the XOUT (P9_1) pin is held high.

10.5.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 10.4 shows the Time from Stop Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.
When the MCU exits stop mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.

The clock used immediately before stop mode divided by 8 is used as the CPU clock when the MCU exits stop mode by a peripheral function interrupt. To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled).

FMR0 Register / FMSTP Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 µs (max.)	Period of system clock × 1 cycle	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 is the time from stop mode until an interrupt routine is executed.
1 (flash memory stops)	100 µs (max.)	Same as above	Same as above	Same as above	

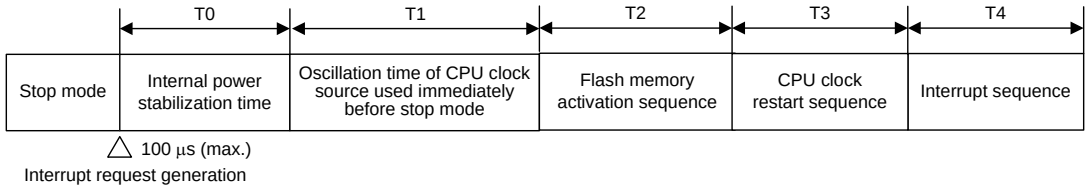


Figure 10.4 Time from Stop Mode to Interrupt Routine Execution

10.6 Power-Off 0 Mode

All oscillator circuits including fOCO-WDT and fOCO-S stop in power-off 0 mode. Since the CPU clock stops, the CPU and all the peripheral functions using this clock are halted.
The least power is consumed in this mode.

10.6.1 Pin Handling in Power-Off 0 Mode

Figure 10.5 shows Pin Handling in Power-Off 0 Mode. The hardware reset must be used in this mode.
The power-on reset cannot be used. For details of resets, refer to **5. Resets**.

10.6.2 Entering Power-Off 0 Mode

Table 10.6 lists the Entering Power-Off 0 Mode and Exit Methods.

(1) Set the FMR01 bit to 0 (CPU rewrite mode disabled).
(2) Set the input pin to exit the mode in power-off 0 mode by the initial write to the POMCR0 register.
(3) When 88h, 15h, 92h, and 25h are written successively to the POMCR0 register, the MCU enters power-off 0 mode.

10.6.3 Pin Status in Power-Off 0 Mode

Table 10.7 lists the Pin Status in Power-Off 0 Mode.
When the MCU enters power-off 0 mode, the contents of RAM and SFRs are not retained.
Save the data needs to be retained to the data flash before entering power-off 0 mode.

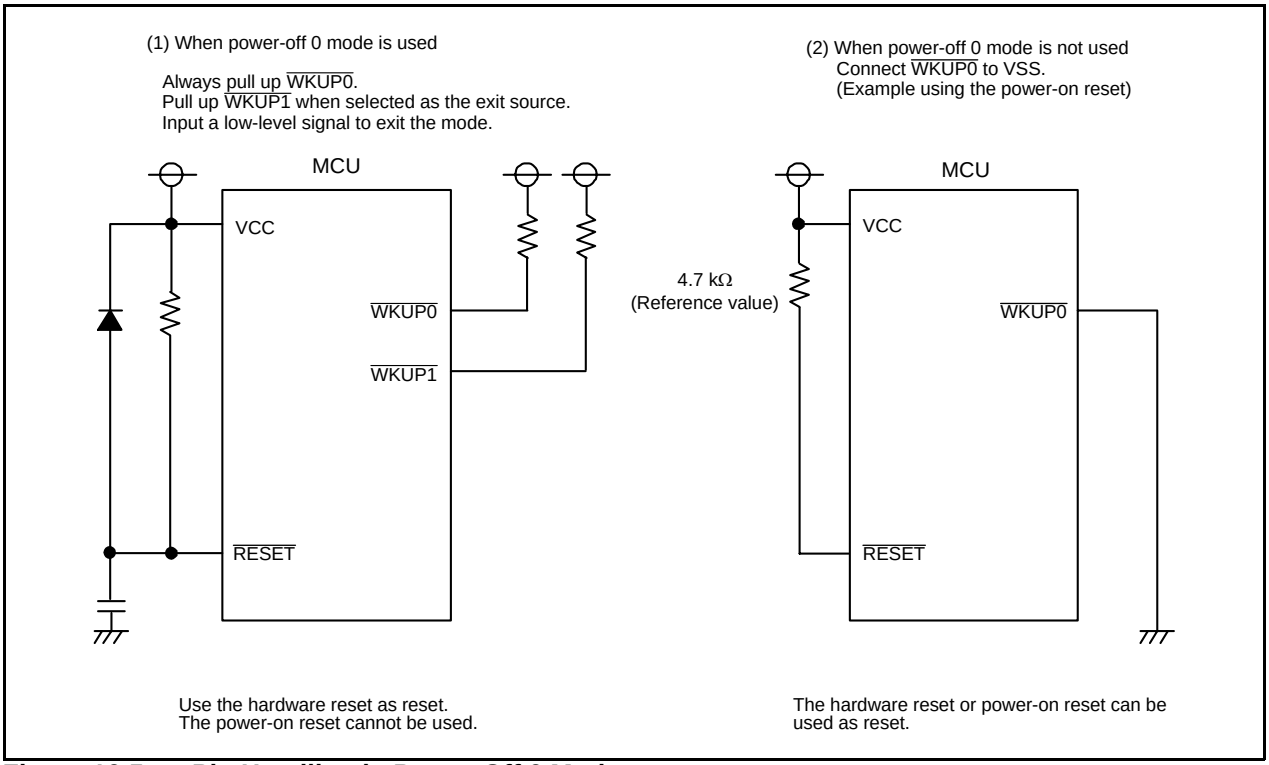


Figure 10.5 Pin Handling in Power-Off 0 Mode

10.6.4 Exiting Power-Off 0 Mode

To exit the mode, input a low-level pulse to the $\overline{\text{RESET}}$, $\overline{\text{WKUP0}}$, or $\overline{\text{WKUP1}}$ pin (when input is enabled).
- $\overline{\text{RESET}}$ pin: The low-level input width must be 2 ms or more.
- Pins $\overline{\text{WKUP0}}$ and $\overline{\text{WKUP1}}$: The low-level input width must be 10 μs or more.

After exiting power-off 0 mode, the operation is the same as a normal reset sequence.
When power-off 0 mode is exited, the exit source can be identified by reading the flags in the POMCR0 register. The values of these flags are undefined after power-on and set to 0 by writing to the POMCR0 register. If multiple exit sources coincide, multiple flags are set.
Figure 10.6 show the Time from Power-Off 0 Mode to Reset Vector Address Read Execution.

Table 10.6 Entering Power-Off 0 Mode and Exit Methods

Entering Power-Off 0 Mode	Status	Exit Method
Write the pin state and the exit method to the POMCR0 register (1) in power-off 0 mode. Then, write 88h,15h, 92h, and 25h successively.	All peripheral functions stop, the contents of RAM and SFRs are not retained.	$\overline{\text{RESET}}$ input, $\overline{\text{WKUP0}}$ input, or $\overline{\text{WKUP1}}$ input (1)

Note:
1. To use $\overline{\text{WKUP1}}$ to exit power-off mode, set the POM01 bit to 1 (input enabled) by the initial write to the POMCR0 register.

Table 10.7 Pin Status in Power-Off 0 Mode

Pin Name	Status
Ports P0 to P4, P5_0 to P5_6	The states of registers LSE0 to LSE5 before entering power-off 0 mode are retained. When LCD ports are selected by these registers, low-level output. When ports are selected, the pins are placed in the high-impedance state.
Ports P6, P7_0 to P7_6, P8, P9_0 to P9_1	High impedance
WKUP0	$\overline{\text{WKUP0}}$ input
XCIN, XCOUT	Oscillation is off (high impedance)
VL1 to VL3	High impedance

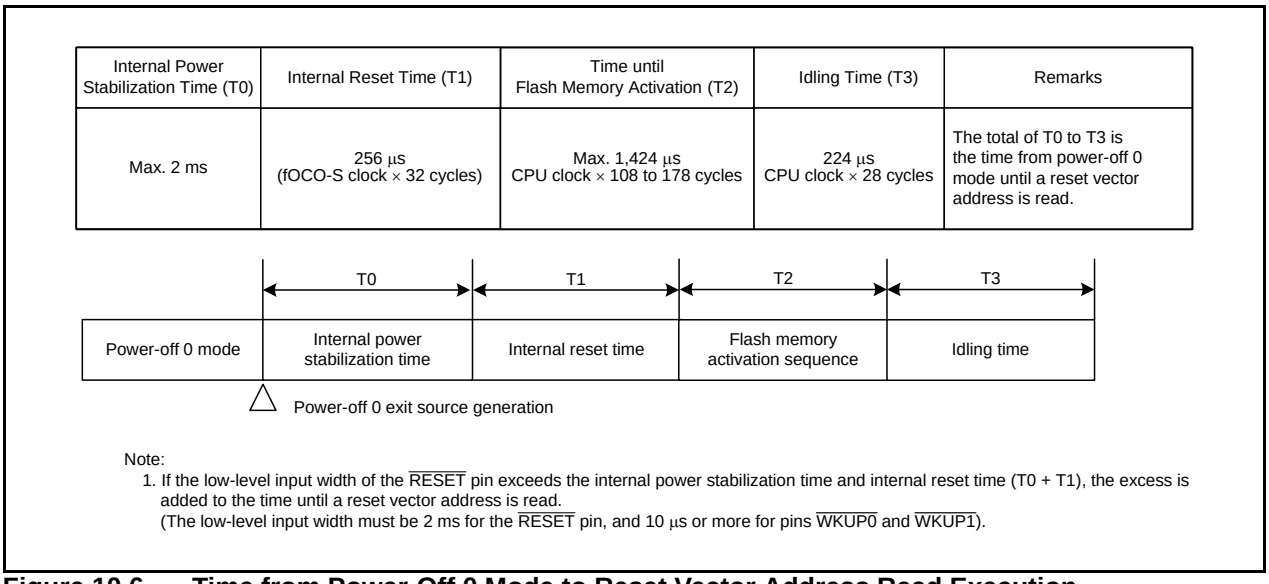

Internal Power Stabilization Time (T0)
Internal Reset Time (T1)
Time until Flash Memory Activation (T2)
Idling Time (T3)
Remarks
Max. 2 ms
256 μs (fOCO-S clock × 32 cycles)
Max. 1,424 μs CPU clock × 108 to 178 cycles
224 μs CPU clock × 28 cycles
The total of T0 to T3 is the time from power-off 0 mode until a reset vector address is read.
T0
T1
T2
T3
Power-off 0 mode
Internal power stabilization time
Internal reset time
Flash memory activation sequence
Idling time
Power-off 0 exit source generation
Note:
1. If the low-level input width of the RESET pin exceeds the internal power stabilization time and internal reset time (T0 + T1), the excess is added to the time until a reset vector address is read.
(The low-level input width must be 2 ms for the RESET pin, and 10 μs or more for pins WKUP0 and WKUP1).

Figure 10.6 Time from Power-Off 0 Mode to Reset Vector Address Read Execution

10.7 Power-off 2 Mode

All oscillator circuits except fOCO-WDT and fC-TRH stop in power-off 2 mode. Since the CPU clock stops, the CPU and the peripheral functions (other than the watchdog timer and timer RH) using this clock are halted. If the voltage applied to the VCC pin is VRAM or more, the content of internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 10.8 lists Interrupts to Exit Power-off 2 Mode and Usage Conditions.

Table 10.8 Interrupts to Exit Power-off 2 Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	Usable
$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$ interrupt	Usable if there is no filter.
Timer RH interrupt	Usable if in real-time clock mode.

10.7.1 Entering Power-off 2 Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 after the CM00 bit in the CM0 register is set to 0. At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use power-off 2 mode, set the following before the MCU enters power-off 2 mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

Enter power-off 2 mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter power-off 2 mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

10.7.2 Pin Status in Power-off 2 Mode

Each I/O port retains its state before the MCU enters power-off 2 mode.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pin), the XOUT (P9_1) pin is held high.

10.7.3 Exiting Power-off 2 Mode

The MCU exits power-off 2 mode by a reset or peripheral function interrupt.
Figure 10.7 shows the Time from Power-off 2 Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit power-off 2 mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting power-off 2 mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting power-off 2 mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting power-off 2 mode.

When the MCU exits power-off 2 mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.
The clock used immediately before power-off 2 mode divided by 8 is used as the CPU clock when the MCU exits power-off 2 mode by a peripheral function interrupt. To enter power-off 2 mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled).

FMR0 Register / FMSTP Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 µs (max.)	Period of system clock × 1 cycle	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 is the time from power-off 2 mode until an interrupt routine is executed.
1 (flash memory stops)	100 µs (max.)	Same as above	Same as above	Same as above	

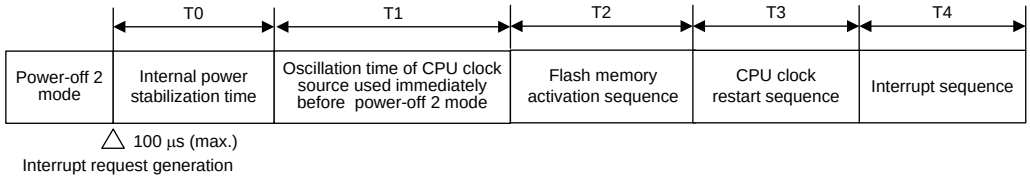


Figure 10.7 Time from Power-off 2 Mode to Interrupt Routine Execution

10.8 Reducing Power Consumption

This section describes key points and processing methods for reducing power consumption. They should be referred to when designing a system or creating a program.

10.8.1 Voltage Detection Circuit

When voltage monitor 1 is not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). When voltage monitor 2 is not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).
When power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

10.8.2 Ports

Even after the MCU enters wait mode, stop mode, or power-off 2 mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to output. When setting them to input, fix to a stable electric potential before the MCU enters wait mode, stop mode, or power-off 2 mode.

10.8.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases. Unnecessary clocks should be stopped accordingly.

Stopping the low-speed on-chip oscillator oscillation: CM14 bit in CM1 register
Stopping the high-speed on-chip oscillator oscillation: FRA00 bit in FRA0 register

10.8.4 Wait Mode, Stop Mode, and Power-Off Mode

Power consumption can be reduced in wait mode, stop mode, and power-off mode.

10.8.5 Stopping Peripheral Function Clocks

When peripheral function clocks are not necessary in wait mode, set bits CM01 and CM02 bit in the CM0 register to stop the clock.

10.8.6 Timers

When timer RJ is not used, set the TCKCUT bit in the TRJiMR register to 1 (count source cutoff).
When timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).
When timer RC is not used, set the MSTTRC bit in the MSTCR0 register to 1 (standby).

10.8.7 A/D Converter

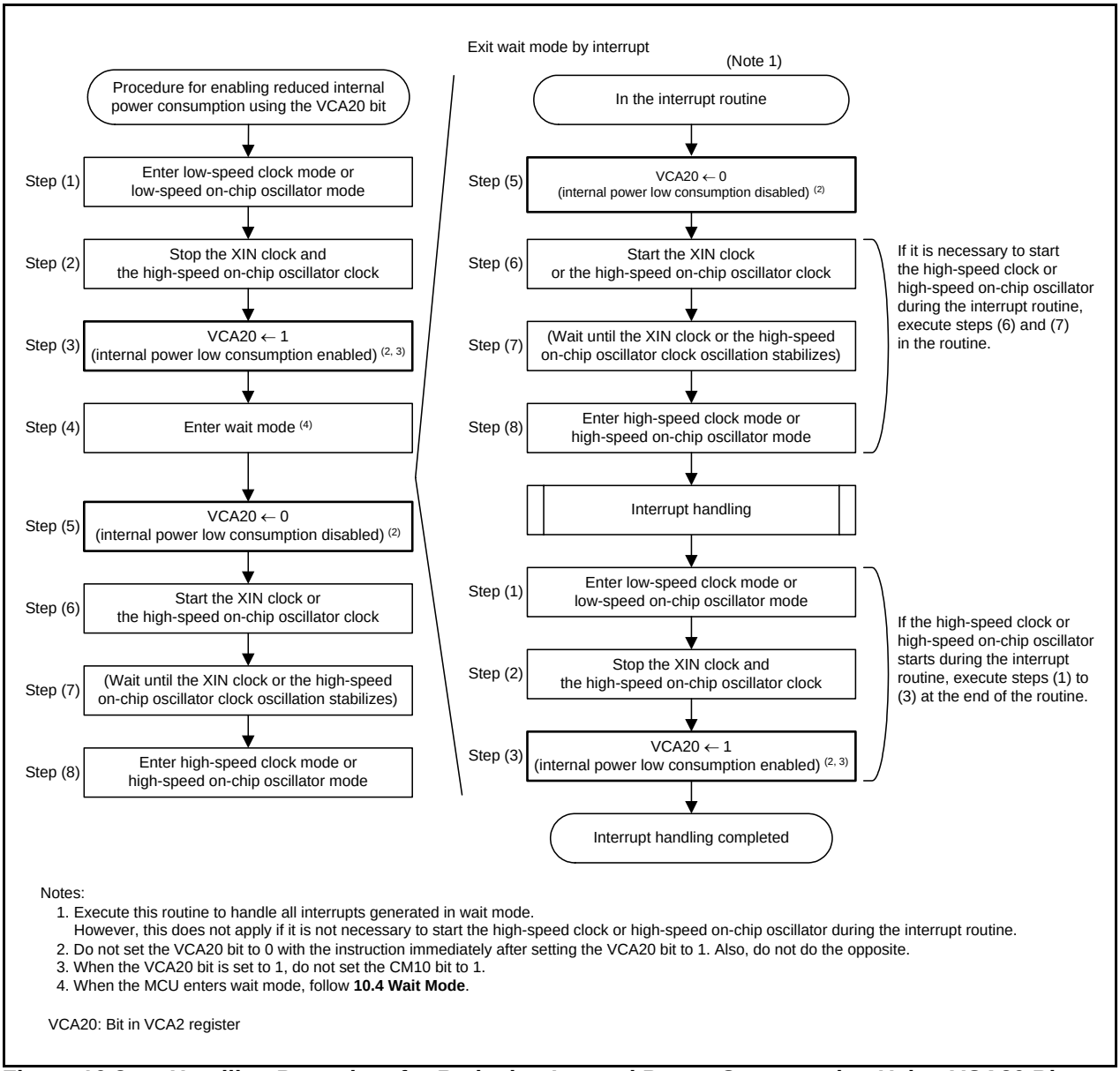
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.

10.8.8 Clock Synchronous Serial Interface

When the SSU or I^2C bus is not used, set the MSTIIC bit in the MSTCR0 register to 1 (standby).

10.8.9 Reducing Internal Power Consumption

When the MCU enters wait mode using low-speed clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced by using the VCA20 bit in the VCA2 register. Figure 10.8 shows the Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit. To enable reduced internal power consumption by the VCA20 bit, follow this procedure.


Procedure for enabling reduced internal power consumption using the VCA20 bit
Step (1)
Enter low-speed clock mode or low-speed on-chip oscillator mode
Step (2)
Stop the XIN clock and the high-speed on-chip oscillator clock
Step (3)
VCA20 ← 1 (internal power low consumption enabled) (2, 3)
Step (4)
Enter wait mode (4)
Step (5)
VCA20 ← 0 (internal power low consumption disabled) (2)
Step (6)
Start the XIN clock or the high-speed on-chip oscillator clock
Step (7)
(Wait until the XIN clock or the high-speed on-chip oscillator clock oscillation stabilizes)
Step (8)
Enter high-speed clock mode or high-speed on-chip oscillator mode
Exit wait mode by interrupt
(Note 1)
In the interrupt routine
Step (5)
VCA20 ← 0 (internal power low consumption disabled) (2)
Step (6)
Start the XIN clock or the high-speed on-chip oscillator clock
Step (7)
(Wait until the XIN clock or the high-speed on-chip oscillator clock oscillation stabilizes)
Step (8)
Enter high-speed clock mode or high-speed on-chip oscillator mode
If it is necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine, execute steps (6) and (7) in the routine.
Interrupt handling
Step (1)
Enter low-speed clock mode or low-speed on-chip oscillator mode
Step (2)
Stop the XIN clock and the high-speed on-chip oscillator clock
Step (3)
VCA20 ← 1 (internal power low consumption enabled) (2, 3)
If the high-speed clock or high-speed on-chip oscillator starts during the interrupt routine, execute steps (1) to (3) at the end of the routine.
Interrupt handling completed

Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1.
4. When the MCU enters wait mode, follow **10.4 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 10.8 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit

10.8.10 Stopping Flash Memory

In low-speed on-chip oscillator mode and low-speed clock mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.

Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.

When the MUC enters stop mode, wait mode, or power-off 2 mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.

Do not use the settings of FMR27 = 1 (low-current-consumption read mode enabled) and FMSTP = 1 (flash memory stops) at the same time.

Figure 10.9 shows the Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit.

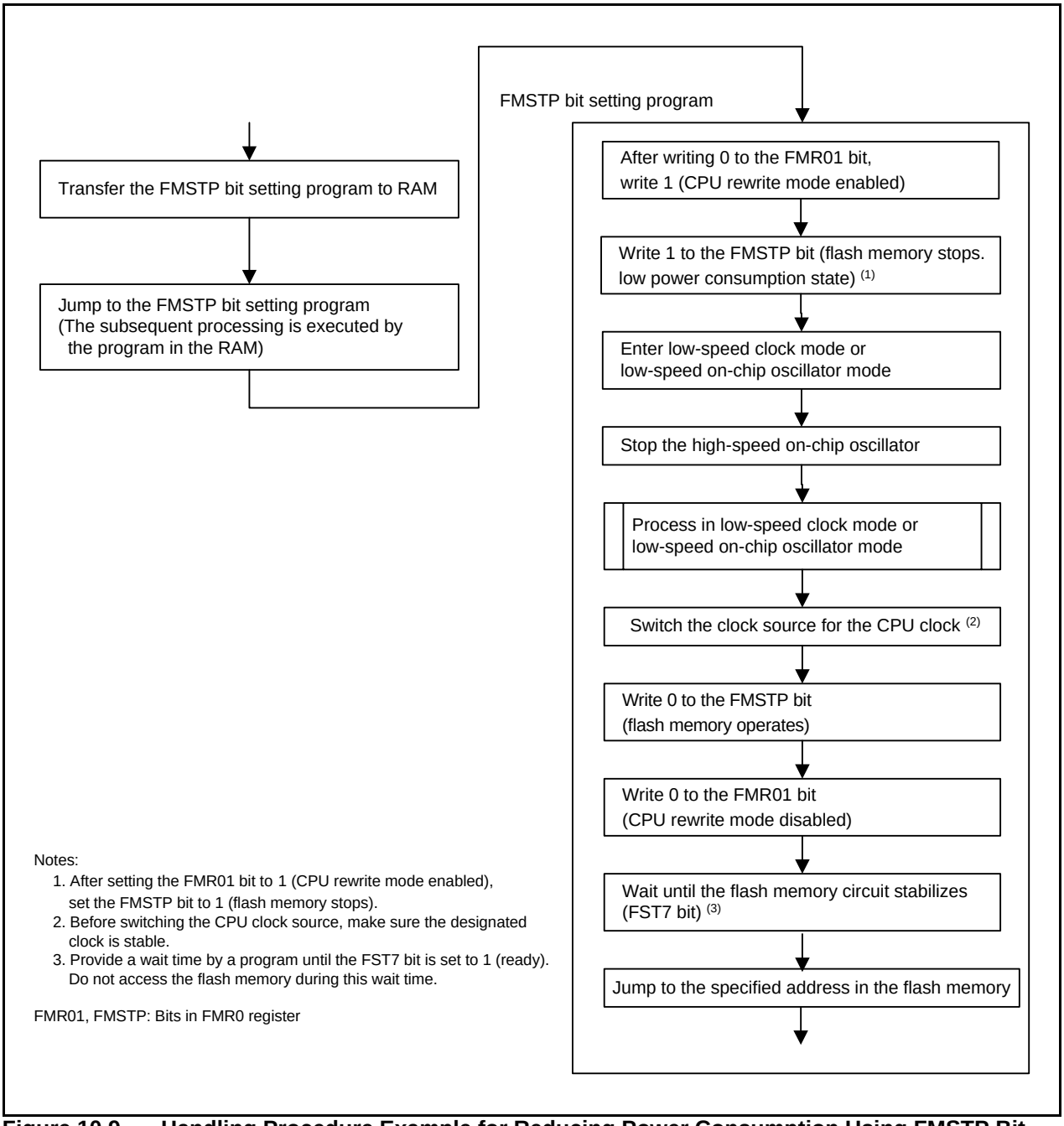

Transfer the FMSTP bit setting program to RAM
Jump to the FMSTP bit setting program
(The subsequent processing is executed by the program in the RAM)
FMSTP bit setting program
After writing 0 to the FMR01 bit, write 1 (CPU rewrite mode enabled)
Write 1 to the FMSTP bit (flash memory stops. low power consumption state) (1)
Enter low-speed clock mode or low-speed on-chip oscillator mode
Stop the high-speed on-chip oscillator
Process in low-speed clock mode or low-speed on-chip oscillator mode
Switch the clock source for the CPU clock (2)
Write 0 to the FMSTP bit (flash memory operates)
Write 0 to the FMR01 bit (CPU rewrite mode disabled)
Wait until the flash memory circuit stabilizes (FST7 bit) (3)
Jump to the specified address in the flash memory
Notes:
1. After setting the FMR01 bit to 1 (CPU rewrite mode enabled), set the FMSTP bit to 1 (flash memory stops).
2. Before switching the CPU clock source, make sure the designated clock is stable.
3. Provide a wait time by a program until the FST7 bit is set to 1 (ready). Do not access the flash memory during this wait time.
FMR01, FMSTP: Bits in FMR0 register

Figure 10.9 Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit

10.8.11 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.

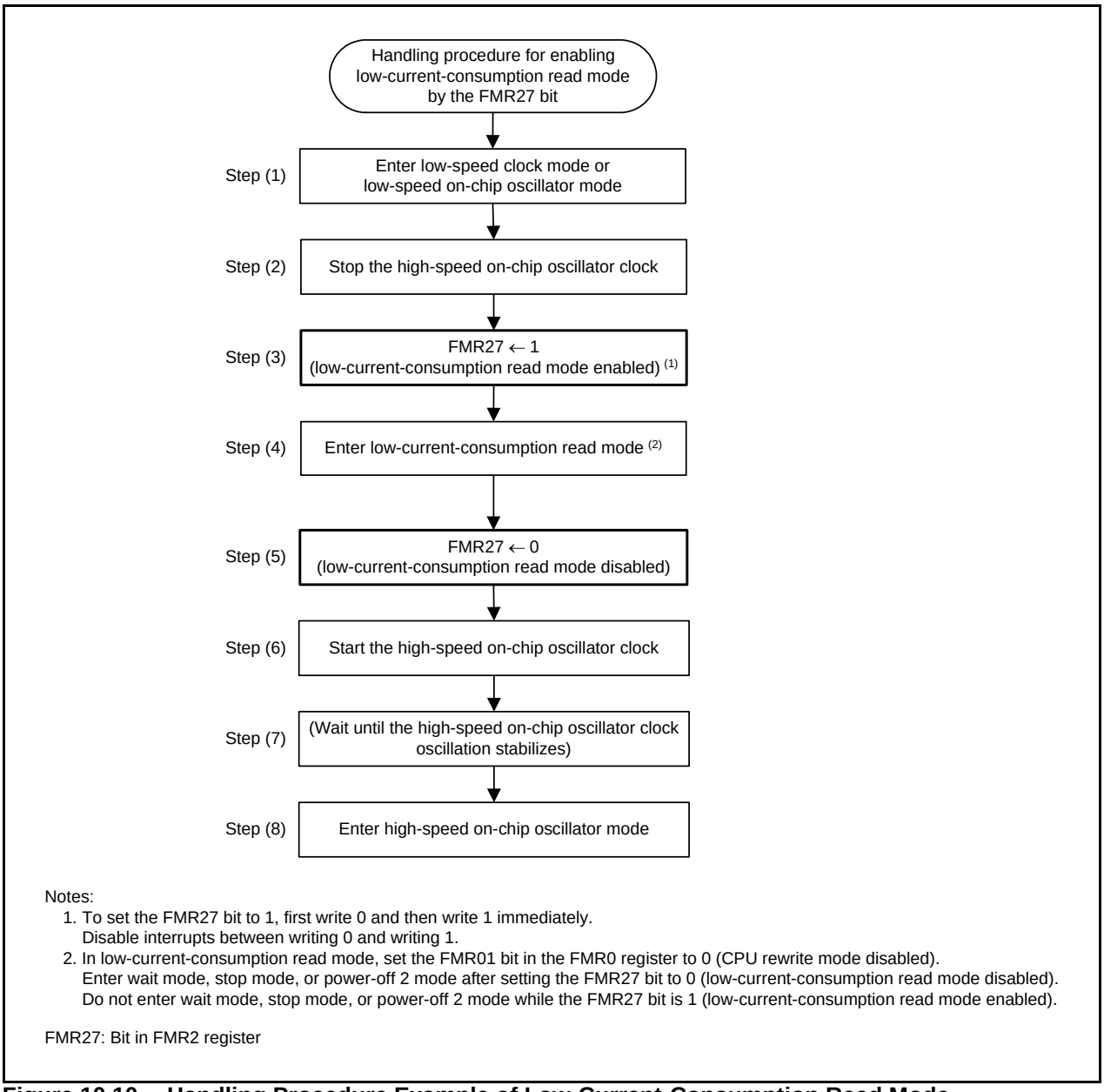
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).

Enter wait mode, stop mode, or power-off 2 mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

Do not use the settings of FMR27 = 1 (low-current-consumption read mode enabled) and FMSTP = 1 (flash memory stops) at the same time.

Figure 10.10 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.


Handling procedure for enabling low-current-consumption read mode by the FMR27 bit
Step (1)
Enter low-speed clock mode or low-speed on-chip oscillator mode
Step (2)
Stop the high-speed on-chip oscillator clock
Step (3)
FMR27 ← 1 (low-current-consumption read mode enabled) (1)
Step (4)
Enter low-current-consumption read mode (2)
Step (5)
FMR27 ← 0 (low-current-consumption read mode disabled)
Step (6)
Start the high-speed on-chip oscillator clock
Step (7)
(Wait until the high-speed on-chip oscillator clock oscillation stabilizes)
Step (8)
Enter high-speed on-chip oscillator mode

Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately.
   Disable interrupts between writing 0 and writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
   Enter wait mode, stop mode, or power-off 2 mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode, stop mode, or power-off 2 mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR27: Bit in FMR2 register

Figure 10.10 Handling Procedure Example of Low-Current-Consumption Read Mode

10.9 Notes on Power Control

10.9.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) first and then set the CM00 bit in the CM0 register to 0 and the CM10 bit in the CM1 register to 1. An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0,PRCR      ; Writing to registers CM0 and CM1 enabled
        FSET    I           ; Interrupt enabled
        BLCR    0,CM0       ; Stop mode selected
        BSET    0,CM1       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

10.9.2 Wait Mode

To enter wait mode by setting the CM30 bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        FSET    I           ; Interrupt enabled
        WAIT                ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

- Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM3 register enabled
        FCLR    I           ; Interrupt disabled
        BSET    0, CM3      ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR     ; Writing to CM3 register disabled
        FSET    I           ; Interrupt enabled
```

10.9.3 Power-Off 0 Mode

To enter power-off mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then access the POMCR0 register. A period of a few microseconds is required between accessing the POMCR0 register and entering power-off 0 mode. As the CPU continues to operate during this period, insert the NOP and the WAIT instructions to stop the program.

• Program example to enter power-off 0 mode

```
BCLR    1, FMR0          ; CPU rewrite mode disabled
MOV.B   #02H, POMCR0     ; Fixed value
MOV.B   #88H, POMCR0     ; Fixed value
MOV.B   #15H, POMCR0     ; Fixed value
MOV.B   #92H, POMCR0     ; Fixed value
MOV.B   #25H, POMCR0     ; Fixed value
NOP;
NOP;
NOP;
NOP                      ; Enter power-off 0 mode
WAIT                     ; Wait mode
```

10.9.4 Power-Off 2 Mode

To enter power-off 2 mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) first, and set the CM00 bit in the CM0 register to 1 and bits CM02 to CM01 to 11b, and then set the CM10 bit in the CM1 register to 1. An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter power-off 2 mode

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0,PRCR      ; Writing to registers CM0 and CM1 enabled
        FSET    I           ; Interrupt enabled
        BSET    0,CM0       ; Power-off 2 mode selected
        BSET    1,CM0       ;
        BSET    2,CM0       ;
        BSET    0,CM1       ; Power-off 2 mode
        JMP.B   LABEL_001
LABEL_001
        NOP
        NOP
        NOP
        NOP
```

11. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control. The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, OCD, FRA0, FRC0, FRA2, and FRC1
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC3 bit: Registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C

11.1 Register

11.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	—	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRC0, FRA2, and FRC1. 0: Write disabled 1: Write enabled (2)	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled (2)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled (2)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:

1. The PRC2 bit is set to 0 after setting it to 1 (write enabled) and writing to the SFR area. Change the register protected by the PRC2 bit with the next instruction after that used to set the PRC2 bit to 1. Do not allow interrupts between the instruction to set to the PRC2 bit to 1 and the next instruction.
2. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.

12. Interrupts

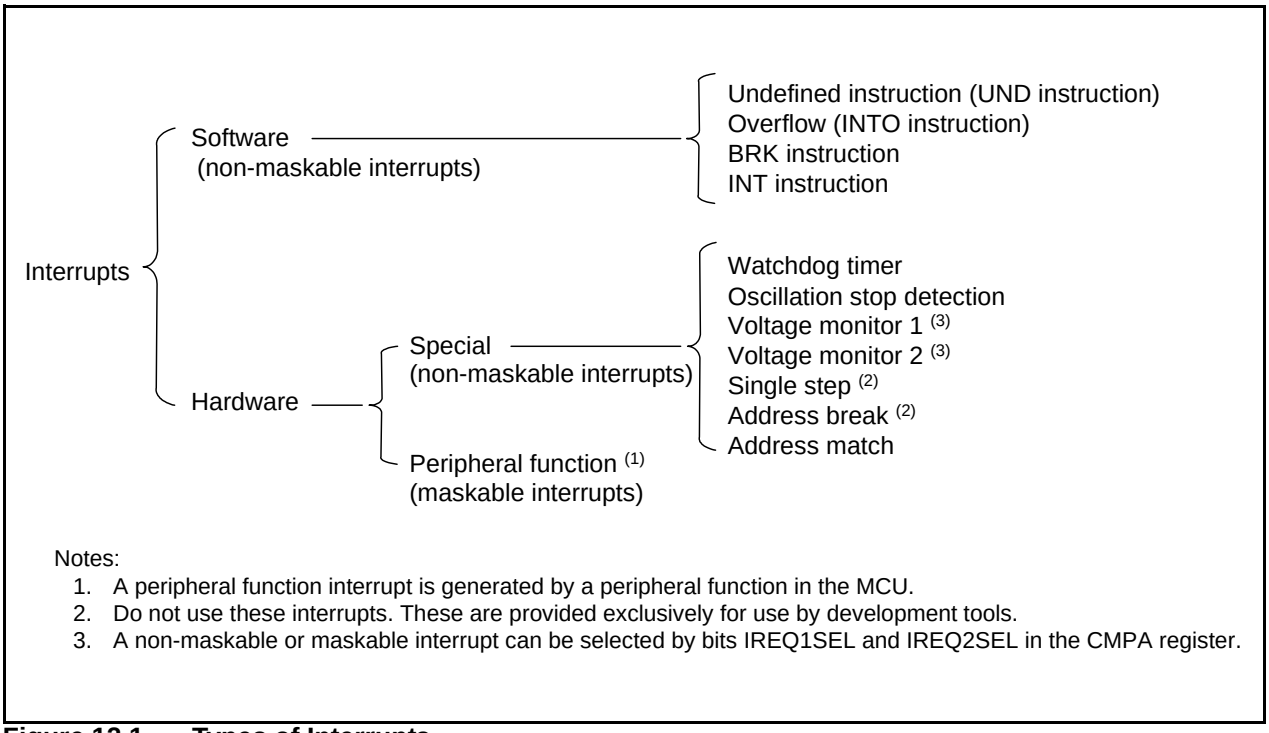
Note

The description offered in this chapter is based on the R8C/LA8A Group.
For other groups, refer to 1.1.2 Differences between Groups.

12.1 Introduction

12.1.1 Types of Interrupts

Figure 12.1 shows the Types of Interrupts.



Notes:
1. A peripheral function interrupt is generated by a peripheral function in the MCU.
2. Do not use these interrupts. These are provided exclusively for use by development tools.
3. A non-maskable or maskable interrupt can be selected by bits IREQ1SEL and IREQ2SEL in the CMPA register.

Figure 12.1 Types of Interrupts

- Maskable interrupts: These interrupts are enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **can be changed** based on the interrupt priority level.
- Non-maskable interrupts: These interrupts are not enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **cannot be changed** based on the interrupt priority level.

12.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

12.1.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt is generated when the UND instruction is executed.

12.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are as follows:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

12.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

12.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified with the INT instruction. Because software interrupt numbers are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

12.1.3 Special Interrupts

Special interrupts are non-maskable.

12.1.3.1 Watchdog Timer Interrupt

A watchdog timer interrupt is generated by the watchdog timer. For details, refer to **15. Watchdog Timer**.

12.1.3.2 Oscillation Stop Detection Interrupt

An oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

12.1.3.3 Voltage Monitor 1 Interrupt

A voltage monitor 1 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

12.1.3.4 Voltage Monitor 2 Interrupt

A voltage monitor 2 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ2SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

12.1.3.5 Single-Step Interrupt, Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use by development tools.

12.1.3.6 Address Match Interrupt

An address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 if the AIER00 bit in the AIER0 register or AIER10 bit in the AIER1 register is set to 1 (address match interrupt enabled).
For details of the address match interrupt, refer to **12.6 Address Match Interrupt**.

12.1.4 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. Refer to **Table 12.2 Relocatable Vector Tables** for sources of the corresponding peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

12.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows an Interrupt Vector.

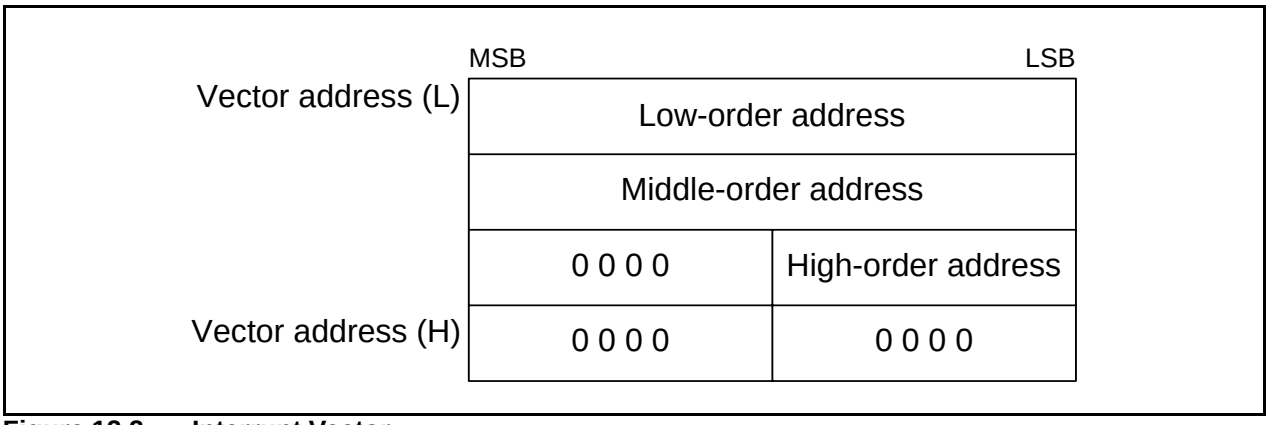


Figure 12.2 Interrupt Vector

12.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 12.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **29.3 Functions to Prevent Flash Memory from being Rewritten**.

Table 12.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction	R8C/Tiny Series User's Manual: Software
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		12.6 Address Match Interrupt
Single step (1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1, Voltage monitor 2	0FFF0h to 0FFF3h		15. Watchdog Timer, 9. Clock Generation Circuit, 6. Voltage Detection Circuit
Address break (1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

Note:
1. Do not use these interrupts. They are provided exclusively for use by development tools.

12.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Table 12.2 lists the Relocatable Vector Tables.

Table 12.2 Relocatable Vector Tables

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction (3)	+0 to +3 (0000h to 0003h)	0	—	R8C/Tiny Series User's Manual: Software
Flash memory ready	+4 to +7 (0004h to 0007h)	1	FMRDYIC	29. Flash Memory
(Reserved)		2	—	—
$\overline{\text{INT7}}$	+12 to +15 (000Ch to 000Fh)	3	INT7IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT6}}$	+16 to +19 (0010h to 0013h)	4	INT6IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT5}}$	+20 to +23 (0014h to 0017h)	5	INT5IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT4}}$	+24 to +27 (0018h to 001Bh)	6	INT4IC	12.4 $\overline{\text{INT}}$ Interrupt
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC	18. Timer RC
(Reserved)		8	—	—
(Reserved)		9	—	
Timer RH	+40 to +43 (0028h to 002Bh)	10	TRHIC	19. Timer RH
UART2 transmit/NACK2	+44 to +47 (002Ch to 002Fh)	11	S2TIC	22. Serial Interface (UART2)
UART2 receive/ACK2	+48 to +51 (0030h to 0033h)	12	S2RIC	
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC	12.5 Key Input Interrupt
A/D conversion	+56 to +59 (0038h to 003Bh)	14	ADIC	26. A/D Converter
Synchronous serial communication unit/ I^2C bus interface (2)	+60 to +63 (003Ch to 003Fh)	15	SSUIC/ IICIC	24. Synchronous Serial Communication Unit (SSU), 25. I^2C bus Interface
(Reserved)		16	—	—
UART0 transmit	+68 to +71 (0044h to 0047h)	17	S0TIC	21. Serial Interface (UART0)
UART0 receive	+72 to +75 (0048h to 004Bh)	18	S0RIC	
(Reserved)		19	—	—
(Reserved)		20	—	
$\overline{\text{INT2}}$	+84 to +87 (0054h to 0057h)	21	INT2IC	12.4 $\overline{\text{INT}}$ Interrupt
Timer RJ0	+88 to +91 (0058h to 005Bh)	22	TRJ0IC	20. Timer RJ
Timer RB1	+92 to +95 (005Ch to 005Fh)	23	TRB1IC	17. Timer RB
Timer RB0	+96 to +99 (0060h to 0063h)	24	TRB0IC	17. Timer RB
$\overline{\text{INT1}}$	+100 to +103 (0064h to 0067h)	25	INT1IC	12.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT3}}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
Timer RJ1	+108 to +111 (006Ch to 006Fh)	27	TRJ1IC	20. Timer RJ
Timer RJ2	+112 to +115 (0070h to 0073h)	28	TRJ2IC	20. Timer RJ
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC	12.4 $\overline{\text{INT}}$ Interrupt
UART2 bus collision detection	+120 to +123 (0078h to 007Bh)	30	U2BCNIC	22. Serial Interface (UART2)
(Reserved)		31	—	—
Software (3)	+128 to +131 (0080h to 0083h) to +164 to +167 (00A4h to 00A7h)	32 to 41	—	R8C/Tiny Series User's Manual: Software
LCD	+168 to +171 (00A8h to 00ABh)	42	LCDIC	28. LCD Drive Control Circuit
(Reserved)		43	—	—
(Reserved)		44 to 49	—	—
Voltage monitor 1	+200 to +203 (00C8h to 00CBh)	50	VCMP1IC	6. Voltage Detection Circuit
Voltage monitor 2	+204 to +207 (00CCh to 00CFh)	51	VCMP2IC	
(Reserved)		52 to 55	—	—
Software (3)	+224 to +227 (00E0h to 00E3h) to +252 to +255 (00FCh to 00FFh)	56 to 63	—	R8C/Tiny Series User's Manual: Software

Notes:
1. These addresses are relative to those in the INTB register.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. These interrupts are not disabled by the I flag.

12.2 Registers

12.2.1 Interrupt Control Register (S2TIC, S2RIC, KUPIC, ADIC, S0TIC, S0RIC, TRJ0IC, TRB1IC, TRB0IC, TRJ1IC, TRJ2IC, U2BCNIC, LCDIC, VCMP1IC, VCMP2IC)

Address 004Bh (S2TIC), 004Ch (S2RIC), 004Dh (KUPIC), 004Eh (ADIC),
0051h (S0TIC), 0052h (S0RIC), 0056h (TRJ0IC), 0057h (TRB1IC),
0058h (TRB0IC), 005Bh (TRJ1IC), 005Ch (TRJ2IC), 005Eh (U2BCNIC),
006Ah (LCDIC), 0072h (VCMP1IC), 0073h (VCMP2IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.2.2 Interrupt Control Register (FMRDYIC, TRCIC, SSUIC/IICIC, TRHIC)

Address 0041h (FMRDYIC), 0047h (TRCIC), 004Ah (TRHIC), 004Fh (SSUIC/IICIC (1))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Selectable by the IICSEL bit in the SSUIICSR register.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.2.3 INTi Interrupt Control Register (INTiIC) (i = 0 to 7)

Address 0043h (INT7IC), 0044h (INT6IC), 0045h (INT5IC), 0046h (INT4IC), 0055h (INT2IC), 0059h (INT1IC), 005Ah (INT3IC), 005Dh (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	POL	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	POL	Polarity switch bit (3)	0: Falling edge selected 1: Rising edge selected (2)	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

Notes:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.
2. When the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (falling edge selected).
3. The IR bit may be set to 1 (interrupt requested) when the POL bit is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

   Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **12.8.5 Rewriting Interrupt Control Register**.

12.3 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the acknowledgement priority. This description does not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

12.3.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

12.3.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RC interrupt, the synchronous serial communication unit interrupt the I^2C bus interface interrupt, and the flash memory interrupt are different. Refer to **12.7 Interrupts of Timer RC, Timer RH, Synchronous Serial Communication Unit, I^2C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)**.

12.3.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 12.3 lists the Settings of Interrupt Priority Levels and Table 12.4 lists the Interrupt Priority Levels Enabled by IPL.

The following are the conditions when an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 12.3 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	—
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	↓
100b	Level 4	↓
101b	Level 5	↓
110b	Level 6	↓
111b	Level 7	High

Table 12.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Level
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts disabled

12.3.4 Interrupt Sequence

The following describes an interrupt sequence which is performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.
Figure 12.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (no interrupt requested). (2)
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before entering the interrupt sequence.
(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

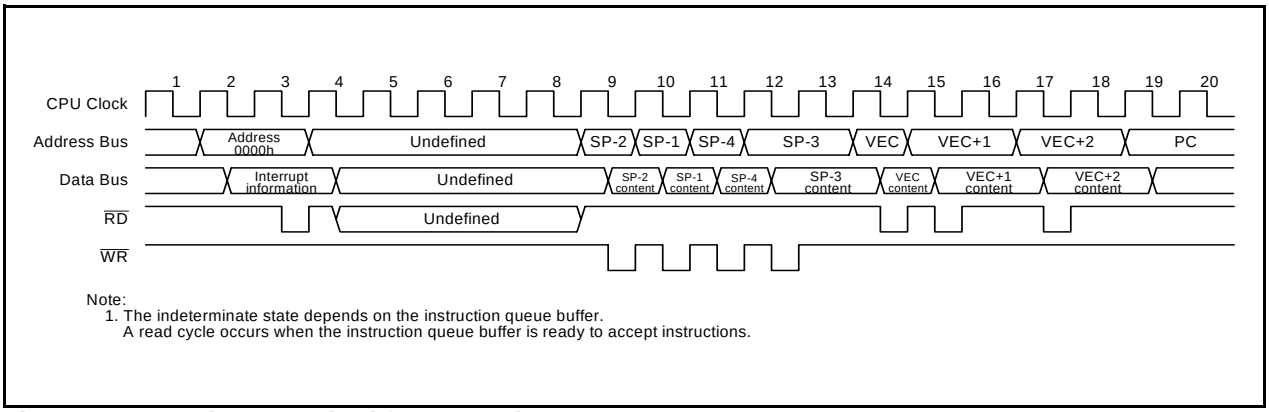
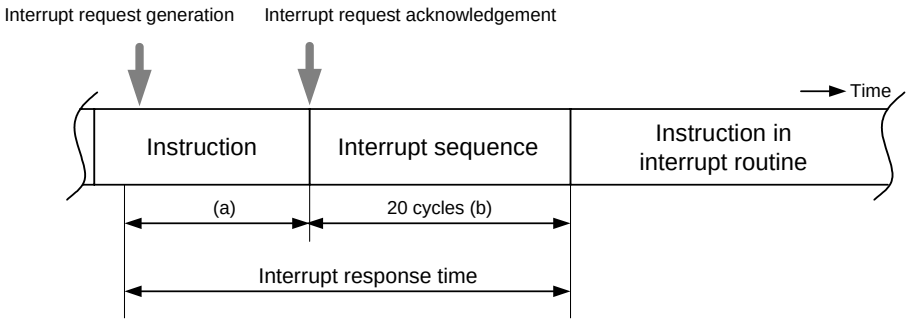


Figure 12.3 Time Required for Executing Interrupt Sequence

Notes:
1. These registers cannot be accessed by the user.
2. Refer to **12.7 Interrupts of Timer RC, Timer RH, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the above interrupts.

12.3.5 Interrupt Response Time

Figure 12.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. The interrupt response time includes the period from when an interrupt request is generated until the currently executing instruction is completed (refer to (a) in Figure 12.4) and the period required for executing the interrupt sequence (20 cycles, refer to (b) in Figure 12.4).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states if the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 12.4 Interrupt Response Time

12.3.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 12.5 is set in the IPL.
Table 12.5 lists the IPL Value When Software or Special Interrupt is Acknowledged.

Table 12.5 IPL Value When Software or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1, voltage monitor 2, address break	7
Software, address match, single-step	No change

12.3.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved on the stack, the 16 low-order bits in the PC are saved.
Figure 12.5 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used (1) with a single instruction.

Note:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

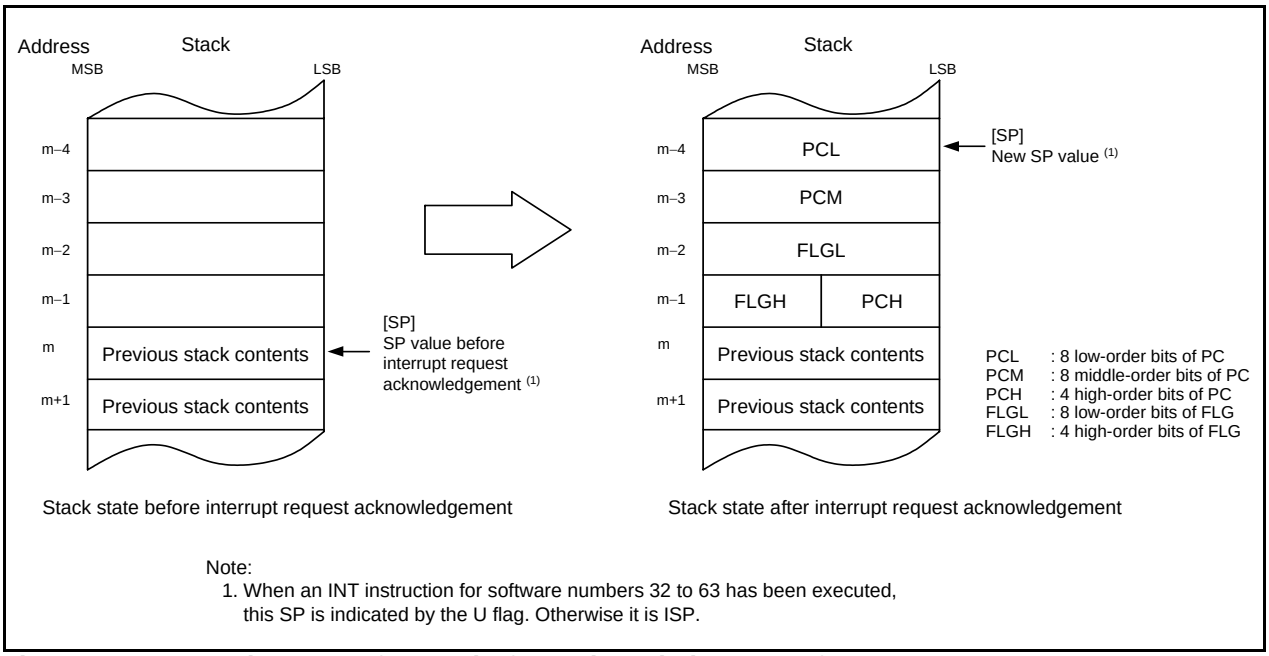
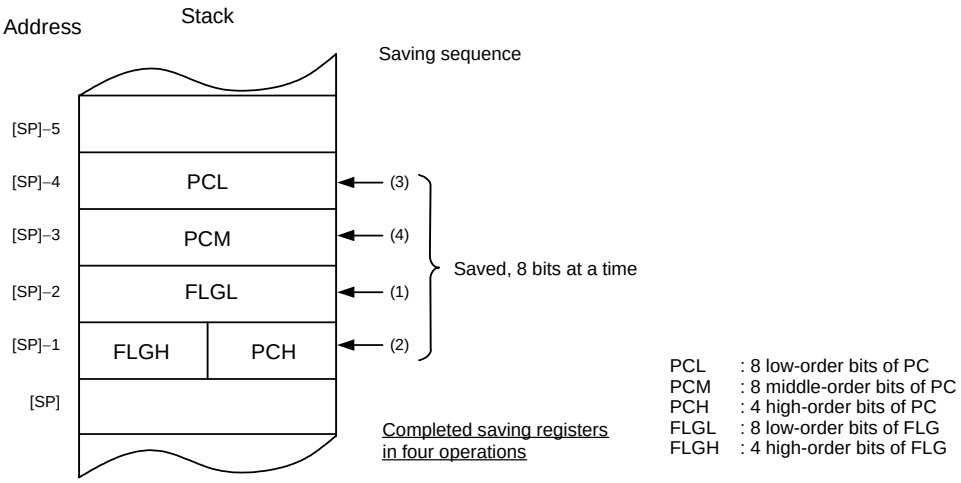


Figure 12.5 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 12.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged.
After registers are saved, the SP content is [SP] minus 4.
When an INT instruction for software numbers 32 to 63 has been executed,
this SP is indicated by the U flag. Otherwise it is ISP.

Figure 12.6 Register Saving Operation

12.3.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.

Registers saved by a program in an interrupt routine should be saved using the POPM instruction or a similar instruction before executing the REIT instruction.

12.3.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Set bits ILVL2 to ILVL0 to select any priority level for maskable interrupts (peripheral function). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.

The priority of the watchdog timer and other special interrupts is set by hardware.

Figure 12.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. When an instruction is executed, the MCU executes the interrupt routine.

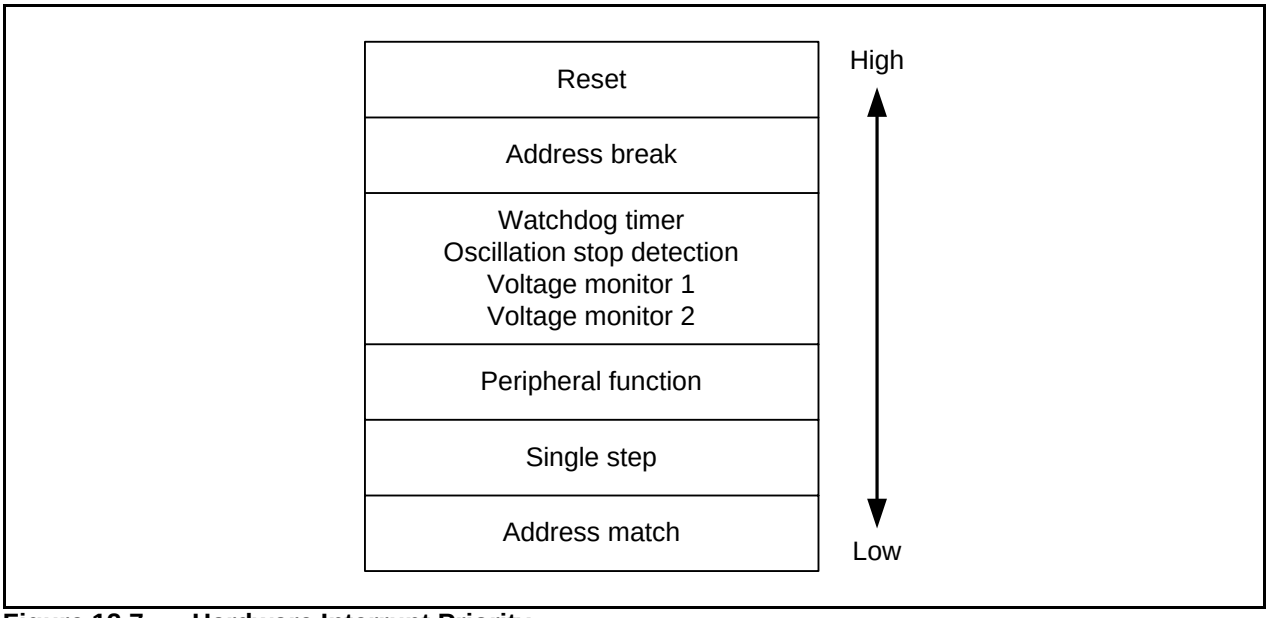


Figure 12.7 Hardware Interrupt Priority

12.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt.
Figure 12.8 shows the Interrupt Priority Level Selection Circuit.

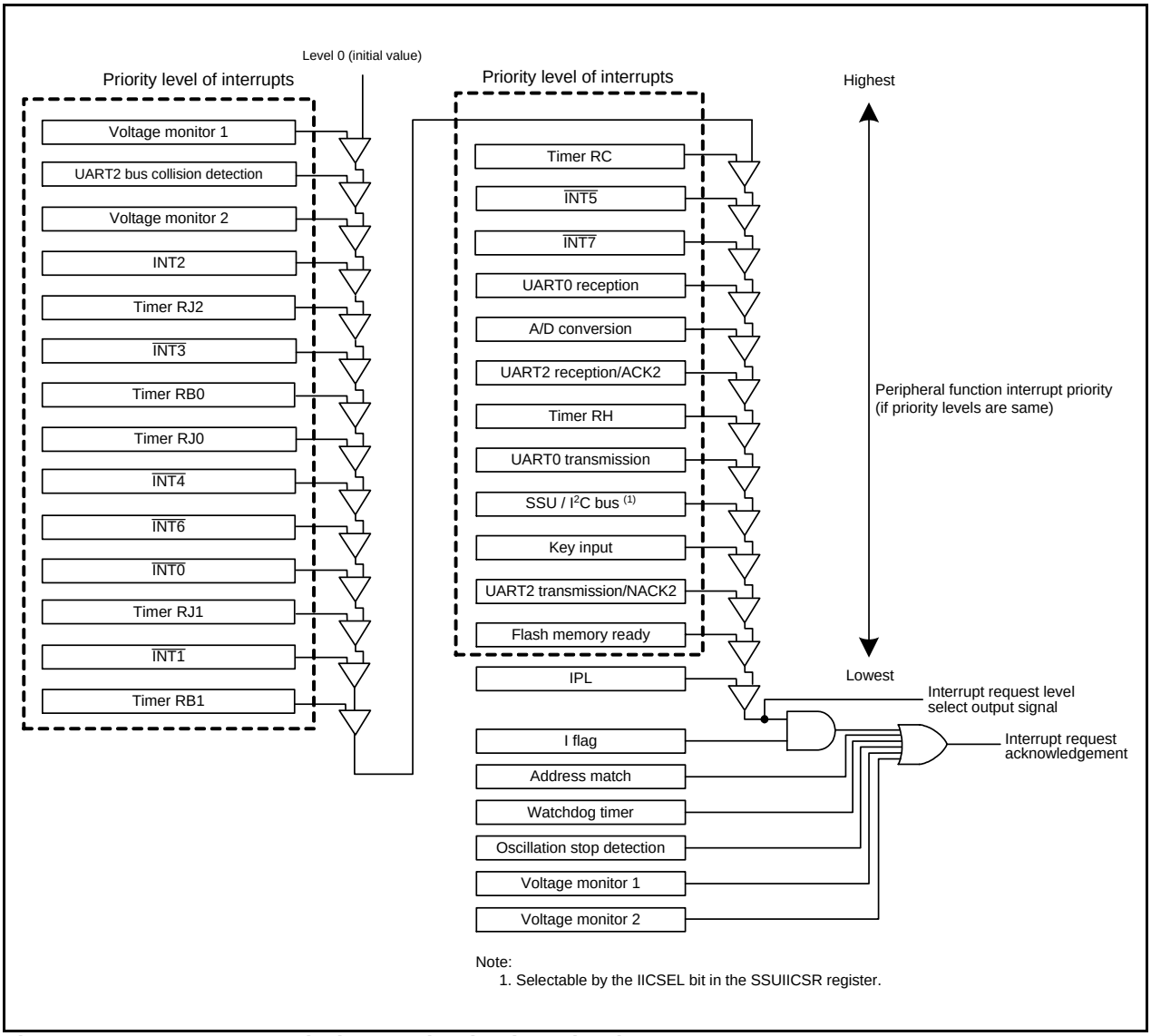


Figure 12.8 Interrupt Priority Level Selection Circuit

12.4 $\overline{\text{INT}}$ Interrupt

12.4.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 7)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register. The input pin used as the $\overline{\text{INTi}}$ input can be selected.
Also, inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff input of timer RC, and the external trigger input of timer RB0.
The $\overline{\text{INT2}}$ pin is shared with the event input of timer RJ.
The $\overline{\text{INT5}}$ pin is shared with the external trigger input of timer RB1.
Table 12.6 lists the Pin Configuration of $\overline{\text{INT}}$ Interrupt.

Table 12.6 Pin Configuration of $\overline{\text{INT}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P0_3 or P3_0	Input	$\overline{\text{INT0}}$ interrupt input, timer RB0 external trigger input, timer RC pulse output forced cutoff input
$\overline{\text{INT1}}$	P8_0 or P3_1	Input	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P8_7 or P3_2	Input	$\overline{\text{INT2}}$ interrupt input, timer RJ event control
$\overline{\text{INT3}}$	P8_1 or P3_3	Input	$\overline{\text{INT3}}$ interrupt input
$\overline{\text{INT4}}$	P1_4 or P3_4	Input	$\overline{\text{INT4}}$ interrupt input
$\overline{\text{INT5}}$	P1_5 or P3_5	Input	$\overline{\text{INT5}}$ interrupt input, timer RB1 external trigger input
$\overline{\text{INT6}}$	P1_6 or P3_6	Input	$\overline{\text{INT6}}$ interrupt input
$\overline{\text{INT7}}$	P0_1 or P3_7	Input	$\overline{\text{INT7}}$ interrupt input

12.4.2 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7SEL0	INT6SEL0	INT5SEL0	INT4SEL0	INT3SEL0	INT2SEL0	INT1SEL0	INT0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0SEL0	$\overline{\text{INT0}}$ pin select bit	0: P0_3 assigned 1: P3_0 assigned	R/W
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	0: P8_0 assigned 1: P3_1 assigned	R/W
b2	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	0: P8_7 assigned 1: P3_2 assigned	R/W
b3	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	0: P8_1 assigned 1: P3_3 assigned	R/W
b4	INT4SEL0	$\overline{\text{INT4}}$ pin select bit	0: P1_4 assigned 1: P3_4 assigned	R/W
b5	INT5SEL0	$\overline{\text{INT5}}$ pin select bit	0: P1_5 assigned 1: P3_5 assigned	R/W
b6	INT6SEL0	$\overline{\text{INT6}}$ pin select bit	0: P1_6 assigned 1: P3_6 assigned	R/W
b7	INT7SEL0	$\overline{\text{INT7}}$ pin select bit	0: P0_1 assigned 1: P3_7 assigned	R/W

The INTSR register selects which pin is assigned as the $\overline{\text{INTi}}$ (i = 0 to 7) input. To use the $\overline{\text{INTi}}$, set this register. Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

12.4.3 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.4.4 External Input Enable Register 1 (INTEN1)

Address 01FBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7PL	INT7EN	INT6PL	INT6EN	INT5PL	INT5EN	INT4PL	INT4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4EN	$\overline{\text{INT4}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT4PL	$\overline{\text{INT4}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT5EN	$\overline{\text{INT5}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT5PL	$\overline{\text{INT5}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT6EN	$\overline{\text{INT6}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT6PL	$\overline{\text{INT6}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT7EN	$\overline{\text{INT7}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT7PL	$\overline{\text{INT7}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 4 to 7) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN1 register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.4.5 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

12.4.6 INT Input Filter Select Register 1 (INTF1)

Address 01FDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7F1	INT7F0	INT6F1	INT6F0	INT5F1	INT5F0	INT4F1	INT4F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4F0	$\overline{\text{INT4}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT4F1			R/W
b2	INT5F0	$\overline{\text{INT5}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT5F1			R/W
b4	INT6F0	$\overline{\text{INT6}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT6F1			R/W
b6	INT7F0	$\overline{\text{INT7}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT7F1			R/W

12.4.7 $\overline{\text{INTi}}$ Input Filter (i = 0 to 7)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected using bits INTiF0 and INTiF1 in registers INTF and INTF1. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).
Figure 12.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 12.10 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

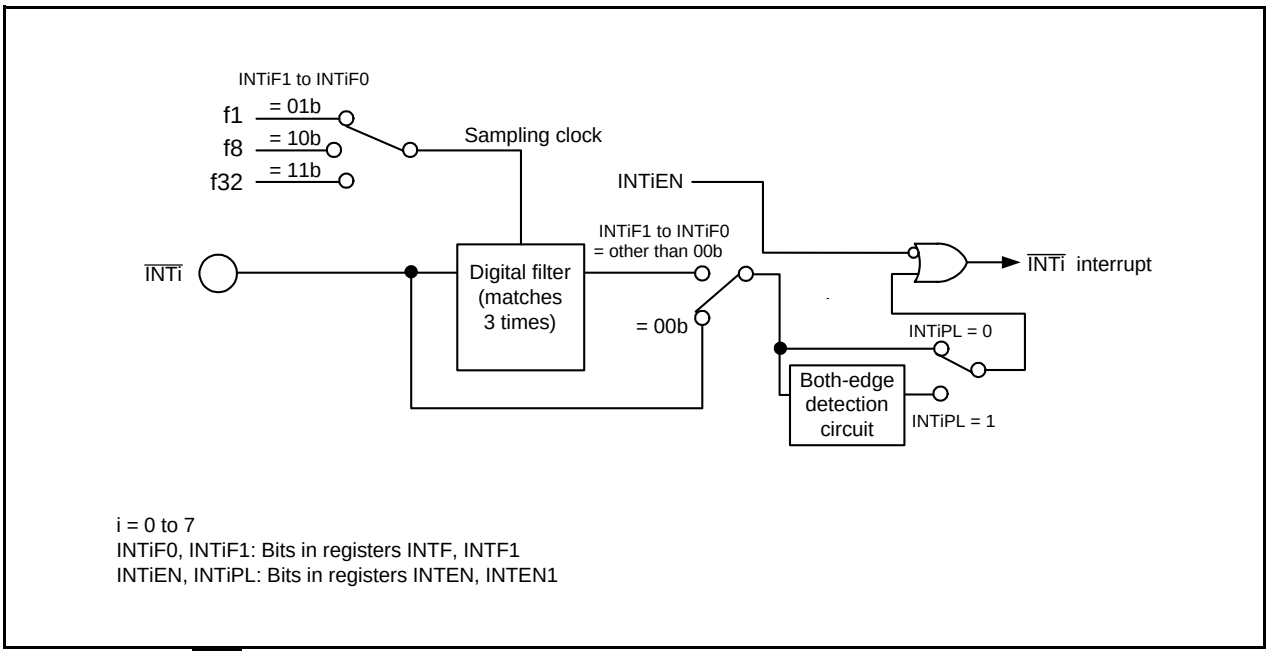


Figure 12.9 $\overline{\text{INTi}}$ Input Filter Configuration

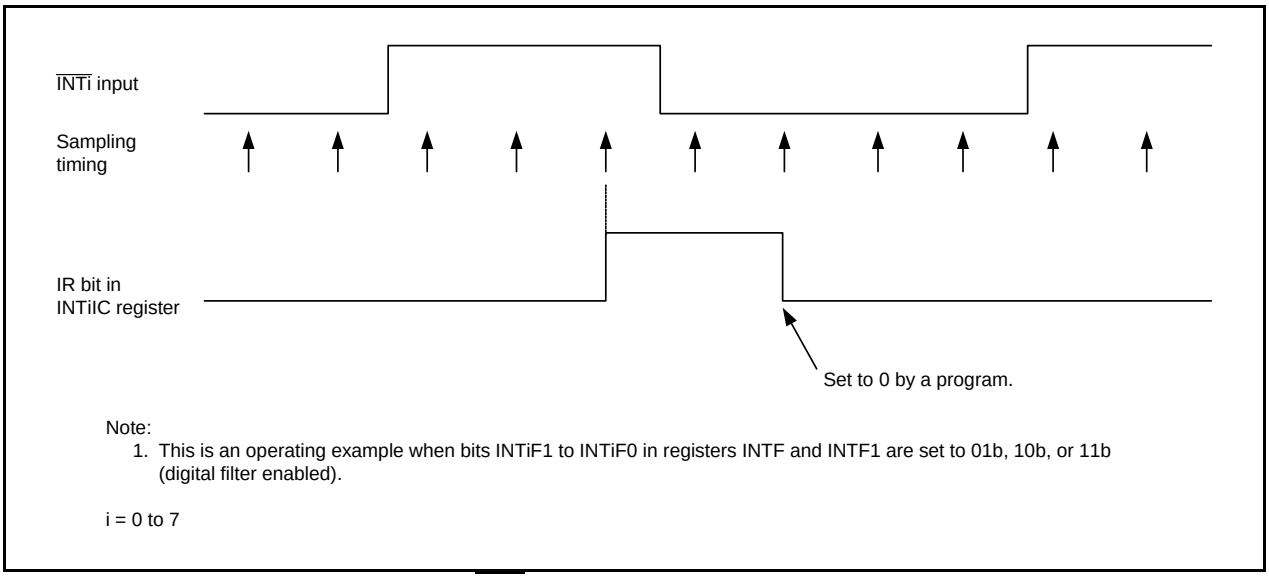

INTi input
Sampling
timing
IR bit in
INTiIC register
Set to 0 by a program.
Note:
1. This is an operating example when bits INTiF1 to INTiF0 in registers INTF and INTF1 are set to 01b, 10b, or 11b
(digital filter enabled).
i = 0 to 7

Figure 12.10 Operating Example of $\overline{\text{INTi}}$ Input Filter

12.5 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins $\overline{K10}$ to $\overline{K17}$. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN bit (i = 0 to 7) in the KIEN register is be used to select whether or not the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is also be used to select the input polarity.

When inputting a low signal to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), the input to the other pins $\overline{K10}$ to $\overline{K17}$ is not detected as interrupts. When inputting a high signal to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input to the other pins $\overline{K10}$ to $\overline{K17}$ is also not detected as interrupts.

Figure 12.11 shows a Block Diagram of Key Input Interrupt. Table 12.7 lists the Key Input Interrupt Pin Configuration.

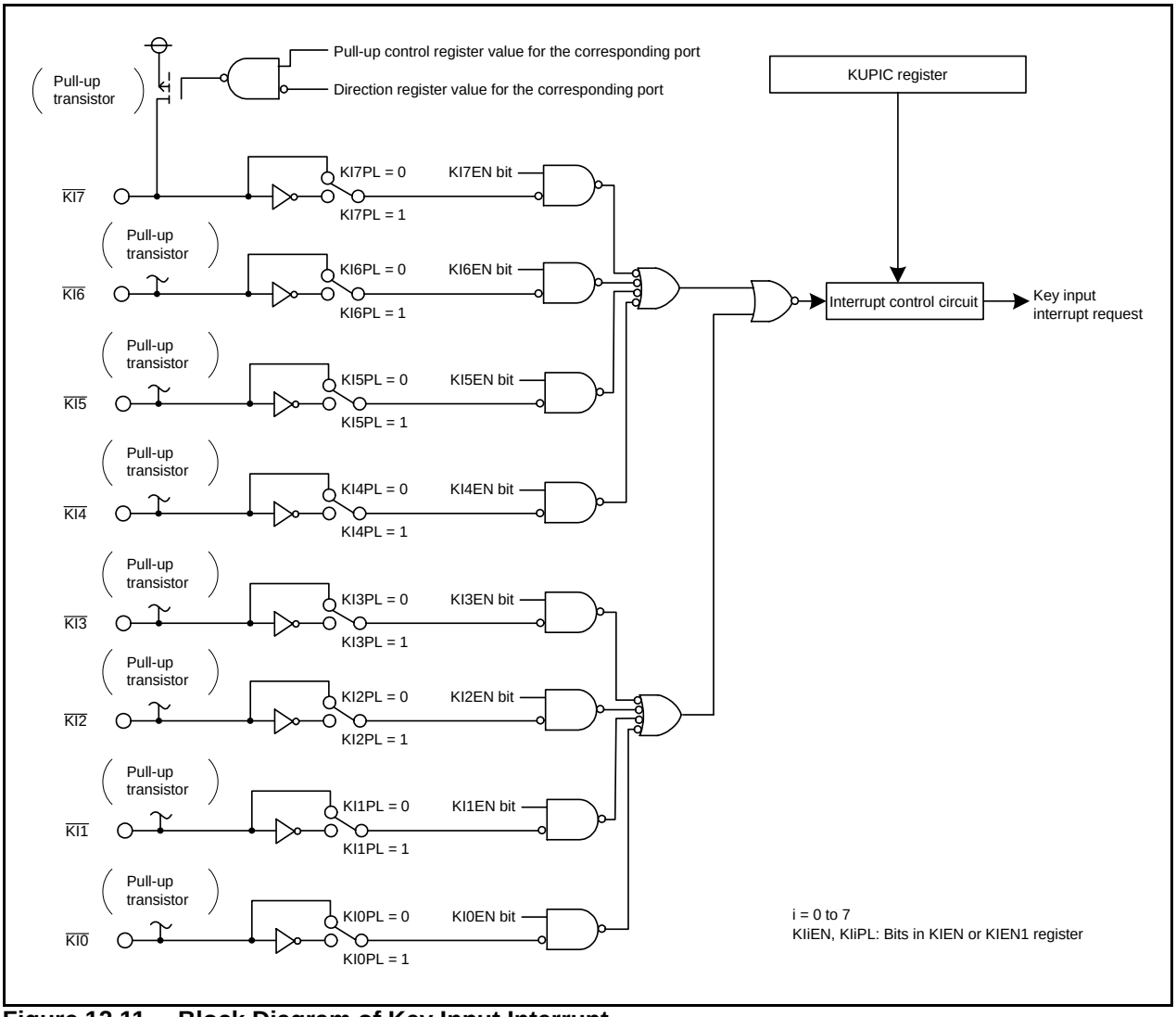


Figure 12.11 Block Diagram of Key Input Interrupt

Table 12.7 Key Input Interrupt Pin Configuration

Pin Name	I/O	Function
$\overline{KI0}$	Input	$\overline{KI0}$ interrupt input
$\overline{KI1}$	Input	$\overline{KI1}$ interrupt input
$\overline{KI2}$	Input	$\overline{KI2}$ interrupt input
$\overline{KI3}$	Input	$\overline{KI3}$ interrupt input
$\overline{KI4}$	Input	$\overline{KI4}$ interrupt input
$\overline{KI5}$	Input	$\overline{KI5}$ interrupt input
$\overline{KI6}$	Input	$\overline{KI6}$ interrupt input
$\overline{KI7}$	Input	$\overline{KI7}$ interrupt input

12.5.1 Key Input Enable Register 0 (KIEN)

Address 01FEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	KI0 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	KI0 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	KI1 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	KI1 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	KI2 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	KI2 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	KI3 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	KI3 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.5.2 Key Input Enable Register 1 (KIEN1)

Address 01FFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI7PL	KI7EN	KI6PL	KI6EN	KI5PL	KI5EN	KI4PL	KI4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI4EN	KI4 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI4PL	KI4 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI5EN	KI5 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI5PL	KI5 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI6EN	KI6 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI6PL	KI6 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI7EN	KI7 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI7PL	KI7 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN1 register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

12.6 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi (i = 0 or 1) register. This interrupt is used as a break function by the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi (i = 0 or 1) register. The AIERi bit in the AIERi register can be used to select the interrupt enabled or disabled. The address match interrupt is not affected by the I flag and IPL.

The PC value (refer to **12.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 12.8 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged.

Table 12.8 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
• Instructions other than listed above	Address indicated by RMADi register + 1

Notes:
1. Refer to the **12.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series User's Manual: Software** (REJ09B0001). **Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 12.9 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER00	RMAD0
Address match interrupt 1	AIER10	RMAD1

12.6.1 Address Match Interrupt Enable Register i (AIERi) (i = 0 or 1)

Address 01C3h (AIER0), 01C7h (AIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	AIER00	AIER0 register
After Reset	0	0	0	0	0	0	0	0	

Symbol	—	—	—	—	—	—	—	AIER10	AIER1 register
After Reset	0	0	0	0	0	0	0	0	

Bit	Symbol	Bit Name	Function	R/W
b0	AIERi0	Address match interrupt i enable bit	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

12.6.2 Address Match Interrupt Register i (RMADi) (i = 0 or 1)

Address 01C2h to 01C0h (RMAD0), 01C6h to 01C4h (RMAD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	X	X	X	X

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Address setting register for address match interrupt	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b21	—			
b22	—			
b23	—			

12.7 Interrupts of Timer RC, Timer RH, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory (Interrupts with Multiple Interrupt Request Sources)

The interrupts of timer RC, timer RH, the synchronous serial communication unit, the I²C bus interface, and the flash memory each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register). Table 12.10 lists the Registers Associated with Interrupts of Timer RC, Timer RH, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory.

Table 12.10 Registers Associated with Interrupts of Timer RC, Timer RH, Synchronous Serial Communication Unit, I²C bus Interface, and Flash Memory

Peripheral Function Name	Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RC	TRCSR	TRCIER	TRCIC
Timer RH	ALIF (bit 0 of TRHIFR) (1), RTCF (bit 1 of TRHIFR) (1), INTF (bit 7 of TRHICR), CMIF (bit 0 of TRHIFR) (2), OVIF (bit 1 of TRHIFR) (2)	TRHIER	TRHIC
		SLINT (bit 5 of TRHICR)	
		ALIE (bit 2 of TRHIFR)	
Synchronous serial communication unit	SSSR	SSER	SSUIC
I²C bus interface	ICSR	ICIER	IICIC
Flash memory	RDYSTI (bit 0 of FST)	RDYSTIE (bit 7 of FMR0)	FMRDYIC
	BSYAEI (bit 1 of FST)	BSYAEIE (bit 6 of FMR0)	
		CMDERIE (bit 5 of FMR0)	

Notes:
1. In real-time clock mode.
2. In output compare mode.

As with other maskable interrupts, the interrupts of timer RC, timer RH, the synchronous serial communication unit, the I2C bus interface, and the flash memory are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).
  That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
  Also, the IR bit is not set to 0 even if 0 is written to this bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.
  The IR bit is also not automatically set to 0 when the interrupt is acknowledged.
  Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.

Refer to chapters of the individual peripheral functions (**18. Timer RC**, **19. Timer RH**, **24. Synchronous Serial Communication Unit (SSU), 25. I2C bus Interface,** and **29. Flash Memory**) for the status register and enable register.
For the interrupt control register, refer to **12.3 Interrupt Control**.

12.8 Notes on Interrupts

12.8.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

12.8.2 SP Setting

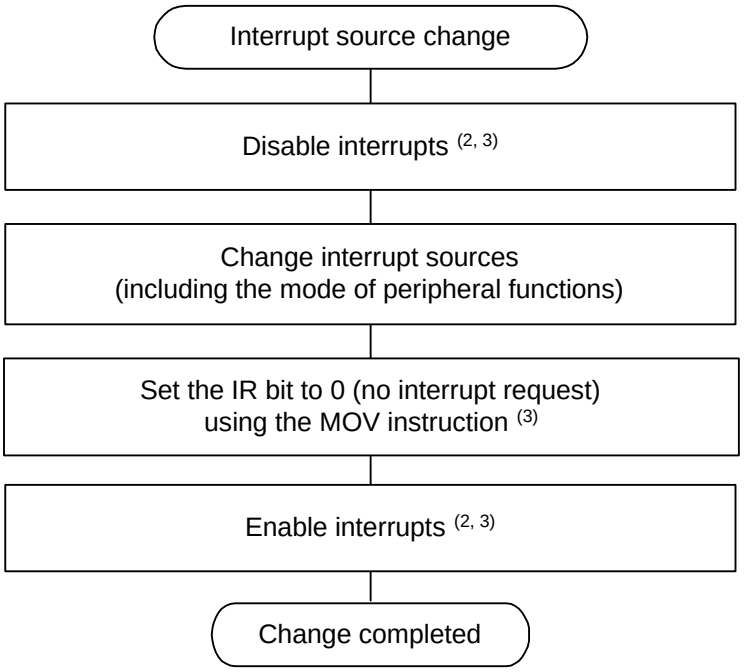
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

12.8.3 External Interrupt, Key Input Interrupt

Either the low-level width or high-level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT7}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$, regardless of the CPU clock.
For details, refer to Table 30.28 **Timing Requirements of External Interrupt $\overline{\text{INTi}}$ (i = 0 to 7) and Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 7)**.

12.8.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 12.12 shows a Procedure Example for Changing Interrupt Sources.


Interrupt source change
Disable interrupts (2, 3)
Change interrupt sources
(including the mode of peripheral functions)
Set the IR bit to 0 (no interrupt request)
using the MOV instruction (3)
Enable interrupts (2, 3)
Change completed

IR bit: Bit in the interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt request). Refer to **12.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 12.12 Procedure Example for Changing Interrupt Sources

12.8.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.

Changing any bit other than the IR bit

If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register:
AND, OR, BCLR, and BSET.

Changing the IR bit

Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.
Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set the TRJ0IC register to 00h
    NOP                 ;
    NOP
    FSET    I           ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set the TRJ0IC register to 00h
    MOV.W   MEM,R0      ; Dummy read
    FSET    I           ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I           ; Disable interrupts
    AND.B   #00H,0056H  ; Set the TRJ0IC register to 00h
    POPC    FLG         ; Enable interrupts
```

13. ID Code Areas

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from being read, rewritten, or erased.

13.1 Introduction

The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 13.1 shows the ID Code Areas.

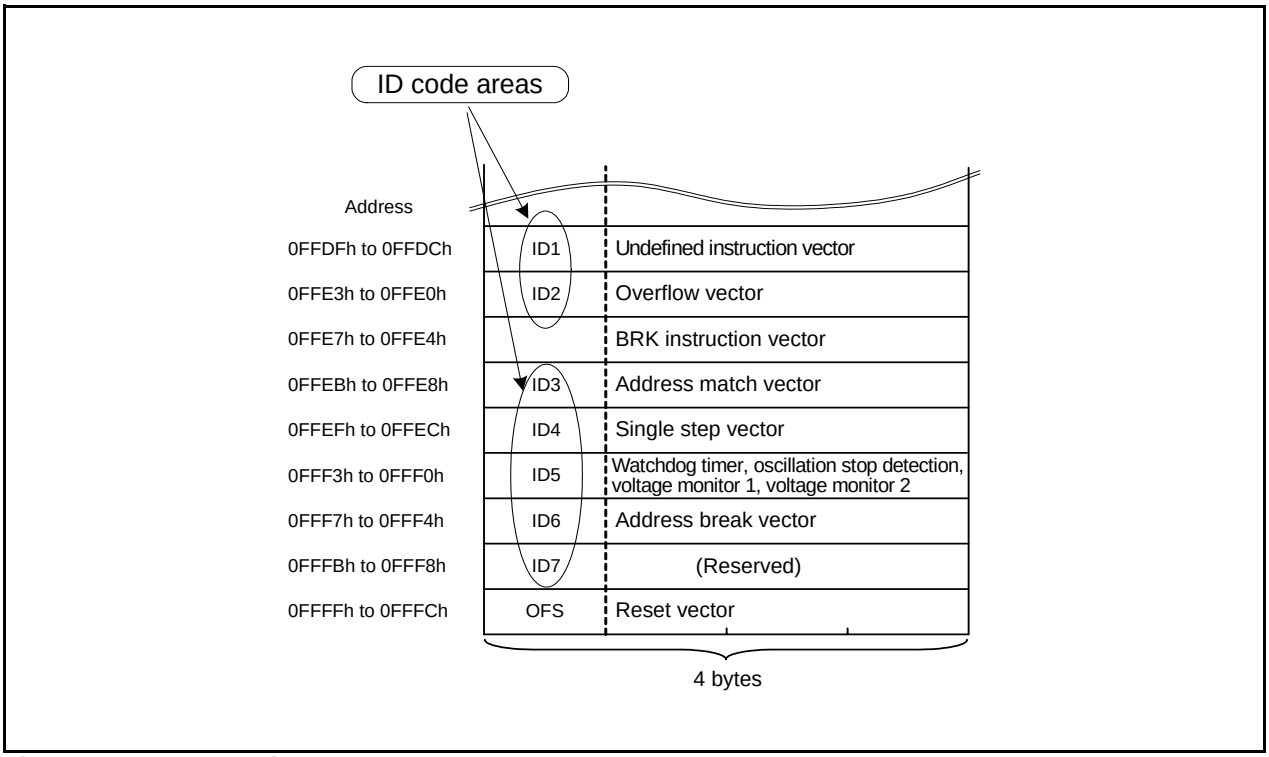


Figure 13.1 ID Code Areas

13.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging emulator, first write predetermined ID codes to the ID code areas.
If 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes are not checked and all commands are accepted.

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

The character sequence of the ASCII codes “ALeRASE” is the reserved word used for the forced erase function. The character sequence of the ASCII codes “Protect” is the reserved word used for the standard serial I/O mode disabled function. Table 13.1 shows the ID Code Reserved Word. The reserved word is a set of reserved characters when all the addresses and data in the ID code storage addresses sequentially match Table 13.1. When the forced erase function or standard serial I/O mode disabled function is not used, use another character sequence of the ASCII codes.

Table 13.1 ID Code Reserved Word

ID Code Storage Address		ID Code Reserved Word (ASCII) (1)	
		ALeRASE	Protect
0FFDFh	ID1	41h (upper-case “A”)	50h (upper-case “P”)
0FFE3h	ID2	4Ch (upper-case “L”)	72h (lower-case “r”)
0FFEBh	ID3	65h (lower-case “e”)	6Fh (lower-case “o”)
0FFEFh	ID4	52h (upper-case “R”)	74h (lower-case “t”)
0FFF3h	ID5	41h (upper-case “A”)	65h (lower-case “e”)
0FFF7h	ID6	53h (upper-case “S”)	63h (lower-case “c”)
0FFFBh	ID7	45h (upper-case “E”)	74h (lower-case “t”)

Note:
1. Reserve word:
   A set of characters when all the addresses and data in the ID code storage addresses sequentially match Table 13.1.

13.3 Forced Erase Function

This function is used in standard serial I/O mode. When the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE” in ASCII code, the content of the user ROM area will be erased at once. However, if the contents of the ID code addresses are set to other than “ALeRASE” (other than **Table 13.1 ID Code Reserved Word**) when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), forced erasure is not executed and the ID codes are checked with the ID code check function. Table 13.2 lists the Conditions and Operations of Forced Erase Function.

When the contents of the ID code addresses are set to “ALeRASE” in ASCII code, if the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE”, the content of the user ROM area will be erased. If the ID codes sent from the serial programmer are other than “ALeRASE”, the ID codes do not match and no command is acknowledged, thus the user ROM area remains protected.

Table 13.2 Conditions and Operations of Forced Erase Function

Condition			Operation
ID code from serial programmer or on-chip debugging emulator	ID code in ID code storage address	Bits ROMCP1 and ROMCR in OFS register	
ALeRASE	ALeRASE	–	All erasure of user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	–	ID code check (ID code check function. No ID code match)
	Other than ALeRASE (1)	–	ID code check (ID code check function)

Note:
1. For “Protect”, refer to **13.4 Standard Serial I/O Mode Disabled Function**.

13.4 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the I/D codes in the ID code storage addresses are set to the reserved character sequence of the ASCII codes “Protect” (refer to **Table 13.1 ID Code Reserved Word**), communication with the serial programmer or the on-chip debugging emulator is not performed. This does not allow the flash memory to be read, rewritten, or erased using the serial programmer or the on-chip debugging emulator.

Also, if the ID codes are also set to the reserved character sequence of the ASCII codes “Protect” when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, rewritten, or erased using the serial programmer, the on-chip debugging emulator, or the parallel programmer.

13.5 Notes on ID Code Areas

13.5.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

14. Option Function Select Area

14.1 Introduction

The option function select area is used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation. The reset vector highest-order-addresses, 0FFFFh and 0FFDBh, are assigned as the option function select area. Figure 14.1 shows the Option Function Select Area.

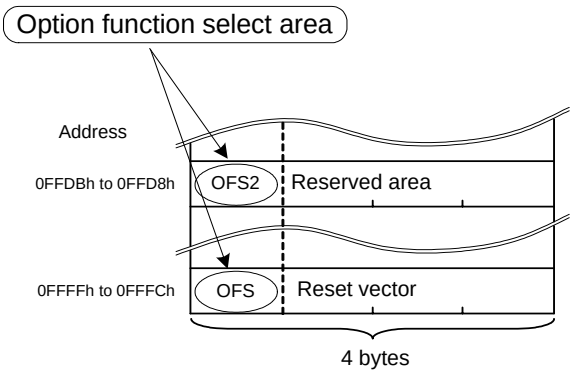


Figure 14.1 Option Function Select Area

14.2 Registers

Registers OFS and OFS2 are used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation.

14.2.1 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

14.2.2 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **14.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

14.3 Notes on Option Function Select Area

14.3.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h) ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

15. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

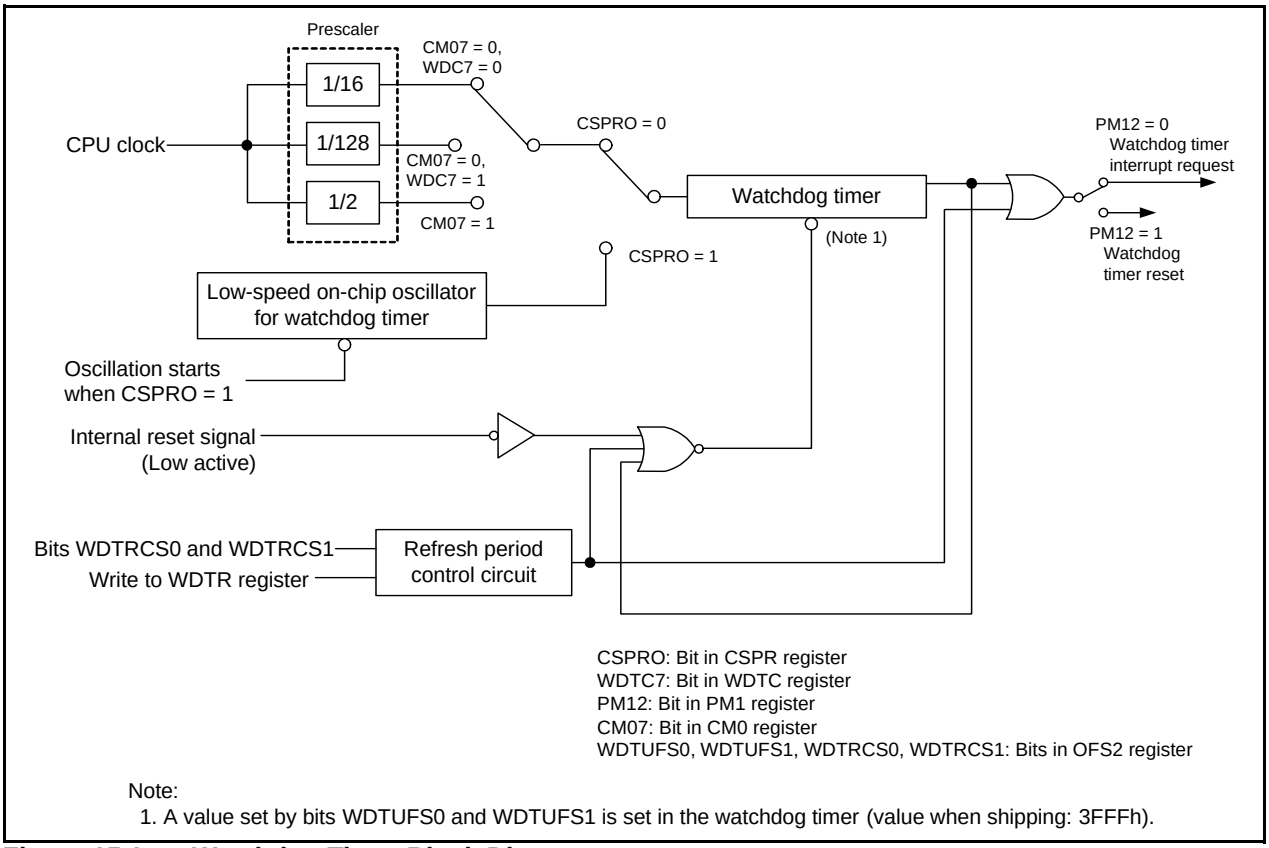
15.1 Introduction

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 15.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 15.1 shows the Watchdog Timer Block Diagram.

Table 15.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting). (1) • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selectable by the WDTC7 bit in the WDTC register or the CM07 bit in the CM0 register. • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selectable by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Note:
1. Write the WDTR register during the count operation of the watchdog timer.



Note:
1. A value set by bits WDTUFS0 and WDTUFS1 is set in the watchdog timer (value when shipping: 3FFFh).

Figure 15.1 Watchdog Timer Block Diagram

15.2 Registers

15.2.1 Processor Mode Register 1 (PM1)

Address 0005h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PM12	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	PM12	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (1)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. The PM12 bit is set to 1 when 1 is written by a program (and remains unchanged even if 0 is written to it). This bit is automatically set to 1 when the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled).

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM1 register.

15.2.2 Watchdog Timer Reset Register (WDTR)

Address 000Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	Writing 00h and then FFh into this register initializes the watchdog timer. The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUF1 in the OFS2 register. (1)	W

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

15.2.3 Watchdog Timer Start Register (WDTS)

Address 000Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	A write instruction to this register starts the watchdog timer.	W

15.2.4 Watchdog Timer Control Register (WDTC)

Address 000Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	—	—	—	—	—	—	—
After Reset	0	0	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	The following bits of the watchdog timer can be read. When bits WDTUFS1 to WDTUFS0 in the OFS2 register are 00b (03FFh): b5 to b0 01b (0FFFh): b7 to b2 10b (1FFFh): b8 to b3 11b (3FFFh): b9 to b4		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—	Reserved bit	When read, the content is 0.	R
b7	WDTC7	Prescaler select bit	0: Divide-by-16 1: Divide-by-128	R/W

15.2.5 Count Source Protection Mode Register (CSPR)

Address 001Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 1.

After Reset	1	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode selected	R/W

Note:
1. To set the CSPRO bit to 1, write 0 and then 1 to it. This bit cannot be set to 0 by a program. Disable interrupts between writing 0 and writing 1.

15.2.6 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

15.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **14.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **15.3.1.1 Refresh Acknowledgment Period**.

15.3 Functional Description

15.3.1 Common Items for Multiple Modes

15.3.1.1 Refresh Acknowledgment Period

The period for acknowledging refreshment operation to the watchdog timer (write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 15.2 shows the Refresh Acknowledgement Period for Watchdog Timer.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgement period is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset (selectable by the PM12 bit in the PM1 register) is generated.

Do not execute any refresh operation while the count operation of the watchdog timer is stopped.

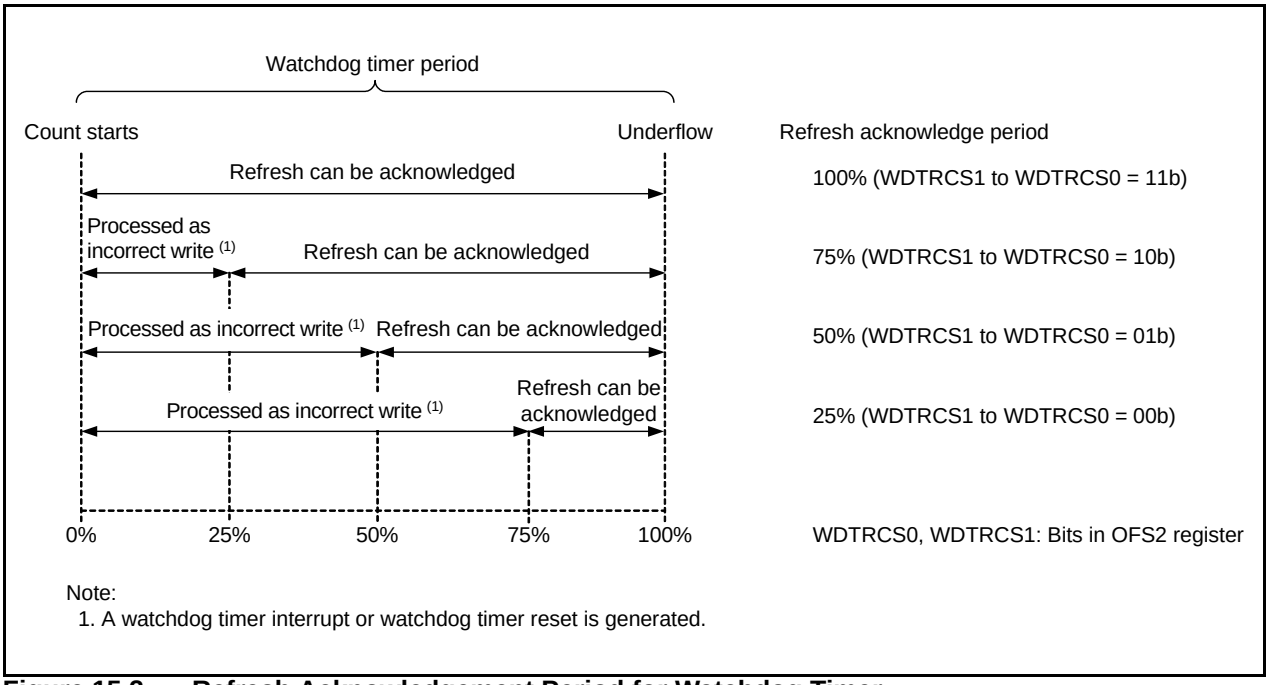


Figure 15.2 Refresh Acknowledgement Period for Watchdog Timer

15.3.2 Count Source Protection Mode Disabled

The count source for the watchdog timer is the CPU clock when count source protection mode is disabled. Table 15.2 lists the Watchdog Timer Specifications (Count Source Protection Mode Disabled).

Table 15.2 Watchdog Timer Specifications (Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	$\frac{\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (m)}}{\text{CPU clock}}$ (1) n: 16 or 128 (selected by the WDTC7 bit in the WDTC register), or 2 when the low-speed clock is selected (CM07 bit in CM0 register = 1) m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 13.1 ms when: - The CPU clock frequency is set to 20 MHz. - The prescaler is divided by 16. - Bits WDTUFS1 to WDTUFS0 are set to 11b (3FFFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (2) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	Stop mode, wait mode (Count resumes from the retained value after exiting.)
Operations at underflow	• When the PM12 bit in the PM1 register is set to 0. Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1. Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)

Notes:
1. The watchdog timer is initialized when 00h and then FFh is written to the WDTR register. The prescaler is initialized after a reset. This may cause some errors due to the prescaler during the watchdog timer period.
2. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

15.3.3 Count Source Protection Mode Enabled

The count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 15.3 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

Table 15.3 Watchdog Timer Specifications (Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value of watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock for the watchdog timer}}$ m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 8.2 ms when: - The on-chip oscillator clock for the watchdog timer is set to 125 kHz. - Bits WDTUFS1 to WDTUFS0 are set to 00b (03FFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (1) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	None (Count does not stop even in wait mode and stop mode once it starts.)
Operation at underflow	Watchdog timer reset (Refer to **5.5 Watchdog Timer Reset.**)
Registers, bits	• When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled) (2), the following are set automatically: - The low-speed on-chip oscillator for the watchdog timer is on. - The PM12 bit in the PM1 register is set to 1 (watchdog timer reset when the watchdog timer underflows).

Notes:
1. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

16. Timers

The following four types of seven timers are available:

- Timer RB: Two 8-bit timer with an 8-bit prescalers
- Timer RC: 16-bit timer
- Timer RH: 3-bit counter, 4-bit counter and 8-bit counter
- Timer RJ: Three 16-bit timers

All these timers operate independently.

Table 16.1 Functional Comparison of Timers (1)

Item		Timer RJ(0)	Timer RJ(1)	Timer RJ(2)	Timer RB(0)	Timer RB(1)	Timer RC	Timer RH
Configuration		16-bit timer (with reload register)	16-bit timer (with reload register)	16-bit timer (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit timer (with input capture and output compare)	3-bit counter 4-bit counter 8-bit counter
Count		Decrement	Decrement	Decrement	Decrement	Decrement	Increment/ Decrement	Increment
Count sources		• f1 • f2 • f8 • fOCO • fC32 • fC	• f1 • f2 • f8 • fOCO • fC32 • fC • Timer RJ(0) underflow	• f1 • f2 • f8 • fOCO • fC32 • fC • Timer RJ(1) underflow	• f1 • f2 • f8 • Timer RJ(0) underflow	• f1 • f2 • f8 • Timer RJ(1) underflow	• f1 • f2 • f4 • f8 • f32 • fOCO8M • fOCO-F • TRCCLK	• f8 • f32 • f128 • f256 • f512 • f2048 • f4096 • f8192 • fC-TRH
Function	Count of the internal count source	Timer mode	Timer mode	Timer mode	Timer mode	Timer mode	Timer mode (output compare function)	—
	Count of the external count source	Event counter mode	Event counter mode	Event counter mode	—	—	Timer mode (output compare function)	—
	External pulse width/period measurement	Pulse width measurement mode, pulse period measurement mode	Pulse width measurement mode, pulse period measurement mode	Pulse width measurement mode, pulse period measurement mode	—	—	Timer mode (input capture function; 4 pins)	—
	PWM output	Pulse output mode (1) Event counter mode (1)	Pulse output mode (1) Event counter mode (1)	Pulse output mode (1) Event counter mode (1)	Programmable waveform generation mode	Programmable waveform generation mode	Timer mode (output compare function; 4 pins) (1) PWM mode (3 pins) PWM2 mode (1 pin)	Output compare mode
	One-shot waveform output	—	—	—	Programmable one-shot generation mode Programmable wait one-shot generation mode	Programmable one-shot generation mode Programmable wait one-shot generation mode	PWM mode (3 pins)	—
	Three-phase waveforms output	—	—	—	—	—	—	—
	Timer	Timer mode (only fC32 count)	Timer mode (only fC32 count)	Timer mode (only fC32 count)	—	—	—	Real-time clock mode

Note:
1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.

Table 16.2 Functional Comparison of Timers (2)

Item	Timer RJ(0)	Timer RJ(1)	Timer RJ(2)	Timer RB(0)	Timer RB(1)	Timer RC	Timer RH
Input pin	RJ0IO	TRJ1IO	TRJ2IO	$\overline{\text{INT0}}$	$\overline{\text{INT5}}$	$\overline{\text{INT0}}$, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD	—
Output pin	TRJ0O TRJ0IO	TRJ1O TRJ1IO	TRJ2O TRJ2IO	TRB0O	TRB1O	TRCIOA, TRCIOB, TRCIOC, TRCIOD	TRHO
Related interrupt	Timer RJ0 interrupt	Timer RJ1 interrupt	Timer RJ2 interrupt	Timer RB0 interrupt, $\overline{\text{INT0}}$ interrupt	Timer RB1 interrupt, $\overline{\text{INT5}}$ interrupt	Compare match/input capture A to D interrupt, Overflow interrupt, $\overline{\text{INT0}}$ interrupt	Timer RH interrupt
Timer stop	Provided	Provided	Provided	Provided	Provided	Provided	Provided

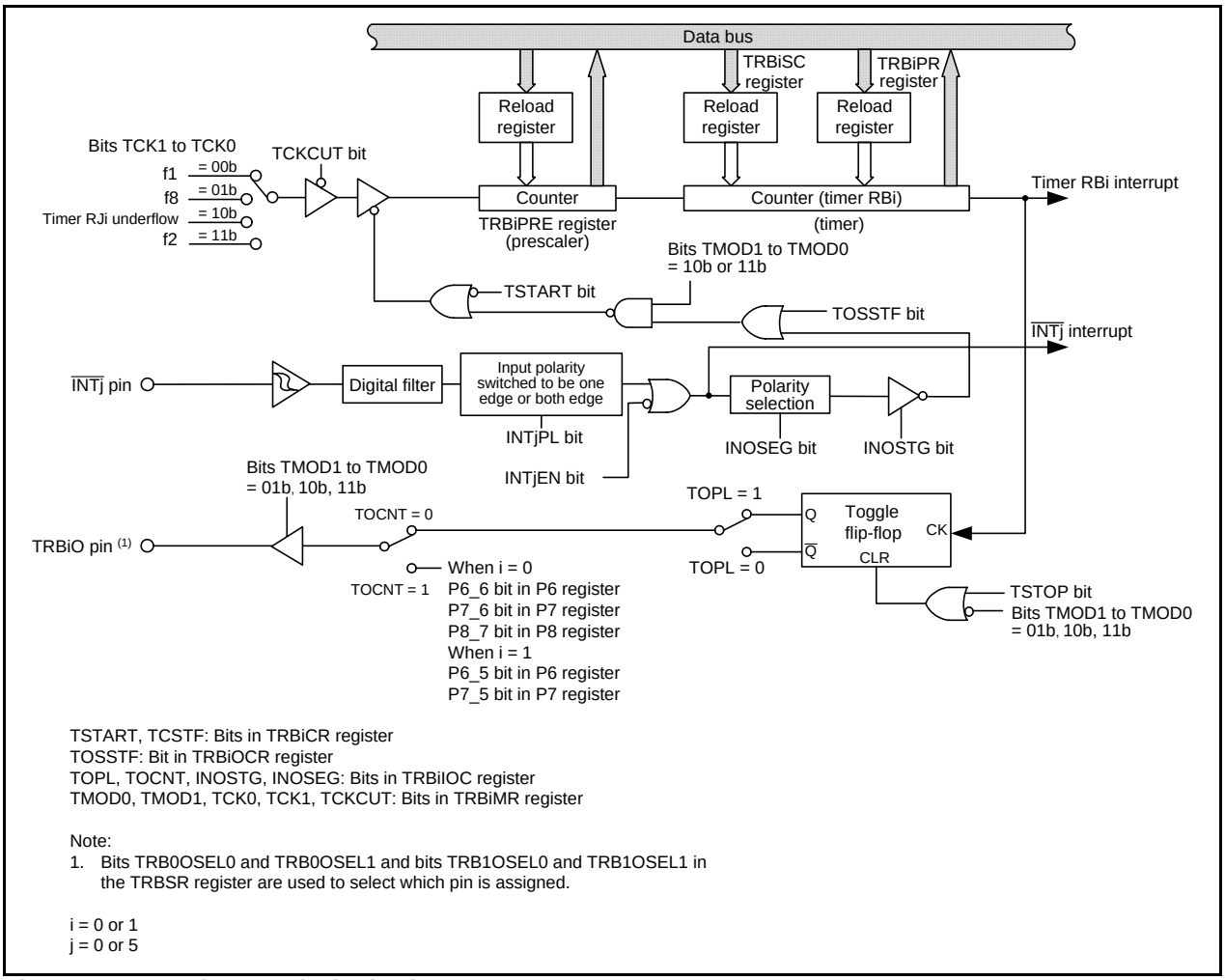
17. Timer RB

17.1 Introduction

Timer RB has two timers (RB0 and RB1).
Timer RB0 and timer RB1 are 8-bit timers with an 8-bit prescaler.
Timer RB has two 8-bit timers (timer RB0 and timer RB1) with an 8-bit prescaler.
The prescaler and timer each consist of a reload register and counter (refer to **Tables 17.3 to 17.6 for the Specifications of Each Mode** for accessing the reload register and counter). Timer RBi (i = 0 or 1) has timer RBi primary and timer RBi secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 17.1 shows the Timer RBi Block Diagram. Table 17.1 lists the Timer RBi Pin Configuration.

Timer RB supports the four operating modes:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RJi underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.



TSTART, TCSTF: Bits in TRBiCR register
TOSSTF: Bit in TRBiOCR register
TOPL, TOCNT, INOSTG, INOSEG: Bits in TRBiIOC register
TMOD0, TMOD1, TCK0, TCK1, TCKCUT: Bits in TRBiMR register

Note:
1. Bits TRB0OSEL0 and TRB0OSEL1 and bits TRB1OSEL0 and TRB1OSEL1 in the TRBSR register are used to select which pin is assigned.

i = 0 or 1
j = 0 or 5

Figure 17.1 Timer RBi Block Diagram

Table 17.1 Timer RBi Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRBO	P6_6, P7_6, P8_7	Output	Pulse output (programmable waveform generation mode, programmable one-shot generation mode, programmable wait one-shot generation mode)
TRB1O	P6_5, P7_5		

Table 17.2 Assigned $\overline{\text{INTj}}$ Pin and Internal Count Source for Each Timer RBi Channel (i = 0 or 1, j = 0 or 5)

Channel	$\overline{\text{INTj}}$ pin	Internal count source (Underflow)
Timer RB0	$\overline{\text{INT0}}$ pin	Timer RJ0
Timer RB1	$\overline{\text{INT5}}$ pin	Timer RJ1

17.2 Registers

17.2.1 Module Standby Control Register 1 (MSTCR1)

Address 0010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRJ2	MSTTRJ1	MSTTRJ0	MSTTRH	MSTTRB1	MSTTRB0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRB0	Timer RB0 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB1	Timer RB1 standby bit	0: Active 1: Standby (2)	R/W
b2	MSTTRH	Timer RH standby bit	0: Active 1: Standby (3)	R/W
b3	MSTTRJ0	Timer RJ0 standby bit	0: Active 1: Standby (4)	R/W
b4	MSTTRJ1	Timer RJ1 standby bit	0: Active 1: Standby (5)	R/W
b5	MSTTRJ2	Timer RJ2 standby bit	0: Active 1: Standby (6)	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. When the MSTTRB0 bit is set to 1 (standby), any access to the timer RB0 associated registers (addresses 0108h to 010Eh) is disabled.
2. When the MSTTRB1 bit is set to 1 (standby), any access to the timer RB1 associated registers (addresses 0098h to 009Eh) is disabled.
3. When the MSTTRH bit is set to 1 (standby), any access to the timer RH associated registers (addresses 0110h to 011Fh) is disabled.
4. When the MSTTRJ0 bit is set to 1 (standby), any access to the timer RJ0 associated registers (addresses 0080h to 0086h) is disabled.
5. When the MSTTRJ1 bit is set to 1 (standby), any access to the timer RJ1 associated registers (addresses 0088h to 008Eh) is disabled.
6. When the MSTTRJ2 bit is set to 1 (standby), any access to the timer RJ2 associated registers (addresses 0090h to 0096h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

17.2.2 Timer RBi Control Register (TRBiCR) (i = 0 or 1)

Address 0108h (TRB0CR), 0098h (TRB1CR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RBi count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RBi count status flag (1)	0: Count stops 1: During count operation (3)	R
b2	TSTOP	Timer RBi count forcible stop bit (1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Refer to **17.7 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When 1 is written to the TSTOP bit, registers TRBiPRE, TRBiSC, TRBiPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBiOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, it indicates that a one-shot pulse trigger has been acknowledged.

17.2.3 Timer RBi One-Shot Control Register (TRBiOCR) (i = 0 or 1)

Address 0109h (TRB0OCR), 0099h (TRB1OCR),

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RBi one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, the content is 0.	R/W
b1	TOSSP	Timer RBi one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0.	R/W
b2	TOSSTF	Timer RBi one-shot status flag (1)	0: One-shot stopped 1: One-shot operating (including wait period)	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When 1 is written to the TSTOP bit in the TRBiCR register, the TOSSTF bit is set to 0.

The TRBiOCR register is enabled when bits TMOD1 to TMOD0 in the TRBiMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

17.2.4 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1)

Address 010Ah (TRB0IOC), 009Ah (TRB1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	Function varies according to the operating mode.	R/W
b1	TOCNT	Timer RBi output enable/disable bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

17.2.5 Timer RBi Mode Register (TRBiMR) (i = 0 or 1)

Address 010Bh (TRB0MR), 009Bh (TRB1MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	TWRC	—	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RBi operating mode select bit (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	TWRC	Timer RBi write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RBi count source select bit (1)	b5 b4 0 0: f1 0 1: f8 1 0: Timer RJi underflow (3) 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	TCKCUT	Timer RBi count source cutoff bit (1)	0: Count source provided 1: Count source cut off	R/W

Notes:
1. Change bits TMOD0 and TMOD1, TCK0 and TCK1, and TCKCUT when both the TSTART and TCSTF bits in the TRBiCR register set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).
3. To use the underflow signal of timer RJi as the count source for timer RB, set timer RJi in timer mode, pulse output mode, or event counter mode.

17.2.6 Timer RBi Prescaler Register (TRBiPRE) (i = 0 or 1)

Address 010Ch (TRB0PRE), 009Ch (TRB1PRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source or timer RJi underflows.	00h to FFh	R/W
	Programmable waveform generation mode		00h to FFh	R/W
	Programmable one-shot generation mode		00h to FFh	R/W
	Programmable wait one-shot generation mode		00h to FFh	R/W

When 1 is written to the TSTOP bit in the TRBiCR register, the TRBiPRE register is set to FFh.

17.2.7 Timer RBi Secondary Register (TRBiSC) (i = 0 or 1)

Address 010Dh (TRB0SC), 009Dh (TRB1SC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Disabled	00h to FFh	—
	Programmable waveform generation mode	Counts timer RBi prescaler underflows (1)	00h to FFh	W (2)
	Programmable one-shot generation mode	Disabled	00h to FFh	—
	Programmable wait one-shot generation mode	Counts timer RBi prescaler underflows (one-shot width is counted)	00h to FFh	W (2)

Notes:
1. The values of registers TRBiPR and TRBiSC are reloaded to the counter alternately and counted.
2. The count value can be read by reading the TRBiPR register even when the secondary period is being counted.

When 1 is written to the TSTOP bit in the TRBiCR register, the TRBiSC register is set to FFh.
To write to the TRBiSC register, perform the following steps.
(1) Write the value into the TRBiSC register.
(2) Write the value into the TRBiPR register. (If the value does not change, write the same value second time.)

17.2.8 Timer RBi Primary Register (TRBiPR) (i = 0 or 1)

Address 010Eh (TRB0PR), 009Eh (TRB1PR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts timer RBi prescaler underflows.	00h to FFh	R/W
	Programmable waveform generation mode	Counts timer RBi prescaler underflows. (1)	00h to FFh	R/W
	Programmable one-shot generation mode	Counts timer RBi prescaler underflows (one-shot width is counted)	00h to FFh	R/W
	Programmable wait one-shot generation mode	Counts timer RBi prescaler underflows (wait period width is counted)	00h to FFh	R/W

Note:
1. The values of registers TRBiPR and TRBiSC are reloaded to the counter alternately and counted.

When 1 is written to the TSTOP bit in the TRBiCR register, the TRBiPR register is set to FFh.

17.2.9 Timer RB Pin Select Register (TRBSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRB1OSEL1	TRB1OSEL0	TRB0OSEL1	TRB0OSEL0	—	—	TRJ2IOSEL1	TRJ2IOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJ2IOSEL0	TRJ2IO pin select bit	b1 b0 0 0: TRJ2IO pin not used 0 1: P6_0 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b1	TRJ2IOSEL1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	TRB0OSEL0	TRB0O pin select bit	b5 b4 0 0: P8_7 assigned 0 1: P7_6 assigned 1 0: P6_6 assigned 1 1: Do not set.	R/W
b5	TRB0OSEL1			R/W
b6	TRB1OSEL0	TRB1O pin select bit	b7 b6 0 0: P7_5 assigned 0 1: P6_5 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b7	TRB1OSEL1			R/W

To use the output pins for timer RJi, set the TRBSR register.
Set this register before setting the timer RJi associated registers. Also, do not change the setting value of this register during timer RJi operation.

17.3 Timer Mode

In timer mode, a internally generated count source or timer RJi (i = 0 or 1) underflows are counted (refer to **Table 17.3**). Registers TRBiOCR and TRBiSC are not used in this mode.

Table 17.3 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RJi underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register content before the count continues (when timer RBi underflows, the content of timer RBi primary reload register is reloaded).
Division ratio	1/(n+1)(m+1) n: Value set in TRBiPRE register, m: Value set in TRBiPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBiCR register.
Interrupt request generation timing	When timer RBi underflows [timer RBi interrupt].
TRBiO pin function	Programmable I/O port
$\overline{\text{INTi}}$ pin function	Programmable I/O port or $\overline{\text{INTi}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBiPR and TRBiPRE.
Write to timer	• When registers TRBiPRE and TRBiPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBiPRE and TRBiPR are written during count operation: If the TWRC bit in the TRBiMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only. (Refer to **17.3.2 Timer Write Control during Count Operation**.)

i = 0 or 1, j = 0 or 5

17.3.1 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1) in Timer Mode

Address 010Ah

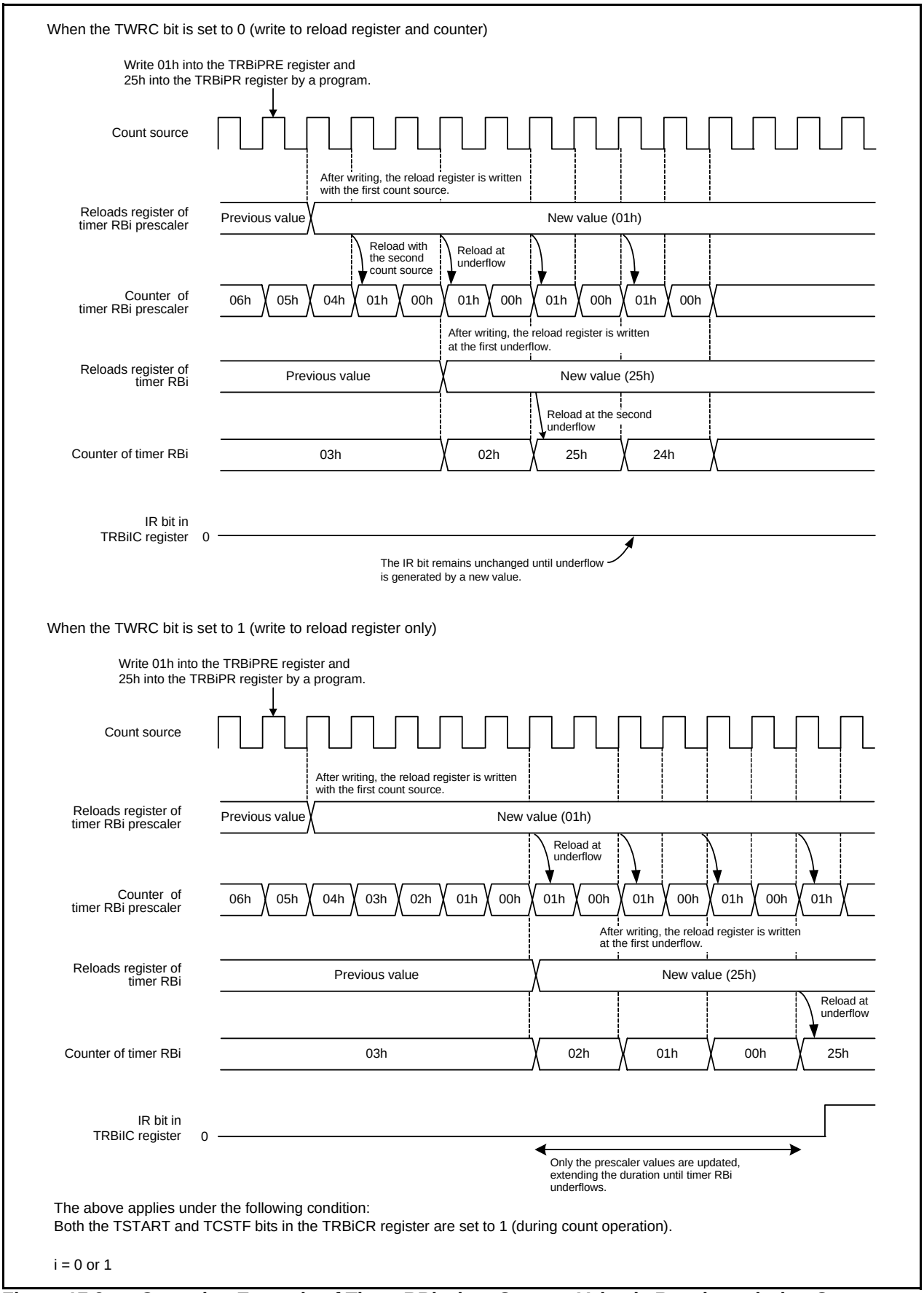
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	Set to 0 in timer mode.	R/W
b1	TOCNT	Timer RBi output enable/disable bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

17.3.2 Timer Write Control during Count Operation

Timer RBi (i = 0 or 1) has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBiMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. If the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted when the prescaler value changes. Figure 17.2 shows an Operating Example of Timer RBi when Counter Value is Rewritten during Count Operation.



The above applies under the following condition:
Both the TSTART and TCSTF bits in the TRBiCR register are set to 1 (during count operation).

i = 0 or 1

Figure 17.2 Operating Example of Timer RBi when Counter Value is Rewritten during Count Operation

17.4 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBiO pin is inverted each time the counter underflows, while the values in registers TRBiPR (i = 0 or 1) and TRBiSC are counted alternately (refer to **Table 17.4**). Counting starts by counting the setting value of the TRBiPR register. The TRBiOCR register is unused in this mode.
Figure 17.3 shows an Operating Example in Timer RBi in Programmable Waveform Generation Mode.

Table 17.4 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RJi underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Frequency of count source n: Value set in TRBiPRE register m: Value set in TRBiPR register p: Value set in TRBiSC register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBiCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RBi underflows during the secondary period (at the same time as the TRBiO output change) [timer RBi interrupt]
TRBiO pin function	Programmable output port or pulse output
$\overline{\text{INTj}}$ pin function	Programmable I/O port or $\overline{\text{INTj}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBiPR and TRBiPRE (1).
Write to timer	• When registers TRBiPRE, TRBiSC, and TRBiPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBiPRE, TRBiSC, and TRBiPR are written to during count operation, values are written to the reload registers only. (2)
Selectable function	• Output level select function The output level during primary and secondary periods is selected by the TOPL bit in the TRBiIOC register. • Waveform output enable/disable function The timer RB waveform output enabled or disabled is selected by the TOCNT bit in the TRBiIOC register. (3)

Notes:
1. Even when the secondary period is being counted, the TRBiPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBiPR register.
3. The value written to the TOCNT bit is enabled by the following.
   • When count starts.
   • When a timer RBi interrupt request is generated.
   The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

i = 0 or 1, j = 0 or 5

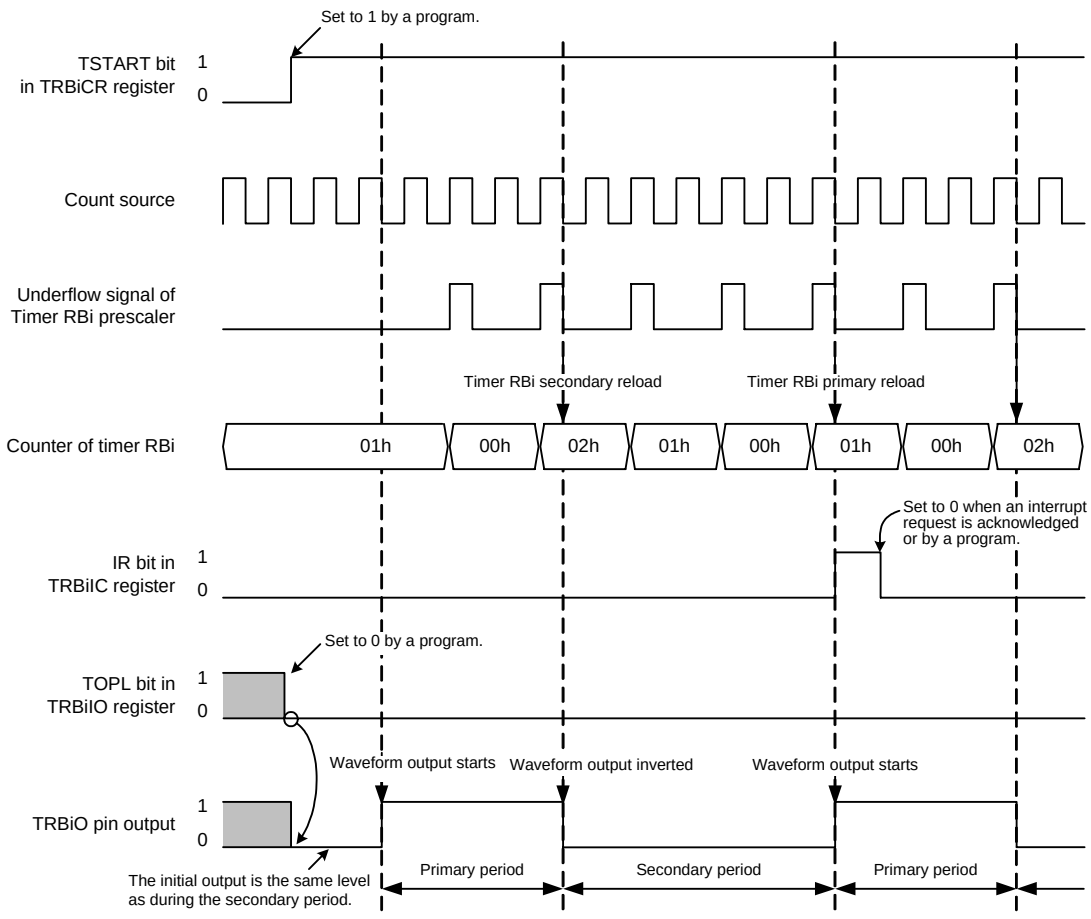
17.4.1 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1) in Programmable Waveform Generation Mode

Address 010Ah (TRB0IOC), 009Ah (TRB1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	0: High-level output for the primary period, low-level output for the secondary period Low-level output when the timer is stopped 1: Low-level output for the primary period, high-level output for the secondary period High-level output when the timer is stopped	R/W
b1	TOCNT	Timer RBi output enable/disable bit	0: Timer RB waveform output enabled 1: Timer RB waveform output disabled	R/W
b2	INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

17.4.2 Operating Example



The above applies under the following conditions:

TRBiPRE = 01h, TRBiPR = 01h, TRBiSC = 02h
TOCNT in TRBiIOC register = 0 (timer RBi waveform output from the TRBiO pin)

i = 0 or 1

Figure 17.3 Operating Example in Timer RBi in Programmable Waveform Generation Mode

17.5 Programmable One-shot Generation Mode

In programmable one-shot generation mode, a one-shot pulse is output from the TRBiO (i = 0 or 1) pin by a program or an external trigger input (input to the $\overline{\text{INTj}}$ (j = 0 or 5) pin) (refer to **Table 17.5**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBiPR register. The TRBiSC register is not used in this mode.
Figure 17.4 shows an Operating Example in Programmable One-Shot Generation Mode.

Table 17.5 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RJi underflow
Count operations	• The setting value of the TRBiPR register is decremented. • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the content of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Frequency of count source n: Value set in TRBiPRE register, m: Value set in TRBiPR register
Count start conditions	• The TSTART bit in the TRBiCR register is set to 1 (count starts) and the next trigger is generated. • 1 (one-shot starts) is written to the TOSST bit in the TRBiOCR register. • Trigger input to the $\overline{\text{INTj}}$ pin
Count stop conditions	• When reloading completes after timer RBi underflows during the primary period • 1 (one-shot stops) is written to the TOSSP bit in the TRBiOCR register. • 0 (count stops) is written to the TSTART bit in the TRBiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBiCR register.
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the waveform output from the TRBiO pin ends) [timer RBi interrupt]
TRBiO pin function	Pulse output
$\overline{\text{INTj}}$ pin functions	• When the INOSTG bit in the TRBiIOC register is set to 0 ($\overline{\text{INTj}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INTj}}$ (j = 0 or 5) interrupt input • When the INOSTG bit in the TRBiIOC register is set to 1 ($\overline{\text{INTj}}$ one-shot trigger enabled): external trigger ($\overline{\text{INTj}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBiPR and TRBiPRE.
Write to timer	• When registers TRBiPRE and TRBiPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBiPRE and TRBiPR are written during count operation, values are written to the reload register only (1).
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBiIOC register. • One-shot trigger select function Refer to **17.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to the TRBiPR register.

i = 0 or 1, j = 0 or 5

17.5.1 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1) in Programmable One-Shot Generation Mode

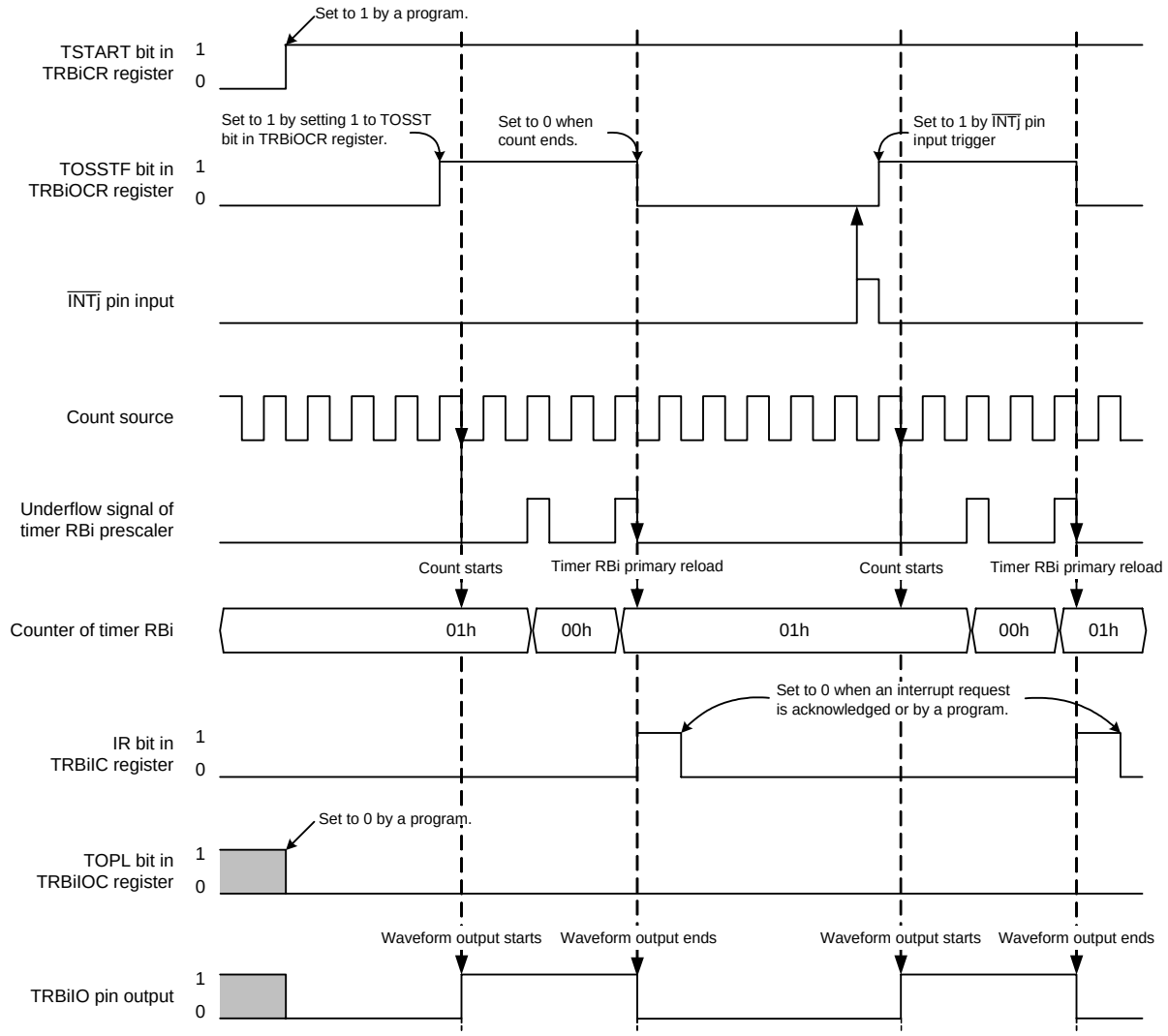
Address 010Ah (TRB0IOC), 009Ah (TRB1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	0: High-level output of a one-shot pulse, low-level output when the timer is stopped 1: Low-level output of a one-shot pulse, high-level output when the timer is stopped	R/W
b1	TOCNT	Timer RBi output enable/disable bit	Set to 0 in programmable one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INTj}}$ (j = 0 or 5) pin one-shot trigger disabled (2) 1: $\overline{\text{INTj}}$ (j = 0 or 5) pin one-shot trigger enabled (2)	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **17.5.3 One-Shot Trigger Selection**.
2. A one-shot trigger is input from the $\overline{\text{INT0}}$ pin for timer RB0 and the $\overline{\text{INT5}}$ pin for timer RB1.

17.5.2 Operating Example



The above applies under the following conditions:

TRBiPRE = 01h, TRBiPR = 01h
TOPL in TRBiIOC register = 0, TOCNT = 0
INOSTG = 1 (INTj one-shot trigger enabled)
INOSEG = 1 (edge trigger at the rising edge)

i = 0 or 1
j = 0 or 5

Figure 17.4 Operating Example in Programmable One-Shot Generation Mode

17.5.3 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBiCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:
- 1 is written to the TOSST bit in the TRBiOCR register by a program.
- Trigger input from the $\overline{\text{INTj}}$ (j = 0 or 5) pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBiOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INTj}}$ pin, input the trigger after making the following settings:

(1) When i = $\overline{\text{INT0}}$
- Select either P0_3 or P3_0 to be assigned as the $\overline{\text{INT0}}$ input with the INT0SEL0 bit in the INTSR register.
- Set the port direction bit in the port direction register corresponding to the pin assigned as the $\overline{\text{INT0}}$ input to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F0 and INT0F1 in the INTF register.
- Set the INT0PL bit in the INTEN register to 0 (one edge) and set the POL bit in the INT0IC register to 0 (falling edge). Furthermore, set the INOSEG bit in the TRB0IOC register to select a falling or rising edge.
- Set the INT0EN bit in the INTEN register to 1 (enabled).
- After completing the above, set the INOSTG bit in the TRB0IOC register to 1 ($\overline{\text{INT0}}$ pin one-shot trigger enabled).

(2) When i = $\overline{\text{INT5}}$
- Select either P1_5 or P3_5 to be assigned as the $\overline{\text{INT5}}$ input with the INT5SEL0 bit in the INTSR register.
- Set the port direction bit in the port direction register corresponding to the pin assigned as the $\overline{\text{INT5}}$ input to 0 (input mode).
- Select the $\overline{\text{INT5}}$ digital filter with bits INT5F0 and INT5F1 in the INTF1 register.
- Set the INT5PL bit in the INTEN1 register to 0 (one edge) and set in the POL bit in the INT5IC register to 0 (falling edge). Furthermore, set the INOSEG bit in the TRB1IOC register to select a falling or rising edge.
- Set the INT5EN bit in the INTEN1 register to 0 (enabled).
- After completing the above, set the INOSTG bit in the TRB1IOC register to 1 ($\overline{\text{INT5}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INTj}}$ pin.
- Processing to handle the interrupts is required. Refer to **12. Interrupts**, for details.
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INTjIC register changes.

17.6 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBiO (i = 0 or 1) pin by a program or an external trigger input (input to the $\overline{\text{INTj}}$ (j = 0 or 5) pin) (refer to **Table 17.6**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value of the TRBiSC register after waiting for a given length of time equal to the setting value of the TRBiPR register. Figure 17.5 shows an Operating Example in Programmable Wait One-Shot Generation Mode.

Table 17.6 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RJi underflow
Count operations	• The setting value of the timer RBi primary is decremented. • When a count of the timer RBi primary underflows, the timer reloads the contents of timer RBi secondary before the count continues. • When a count of the timer RBi secondary underflows, the timer reloads the contents of timer RBi primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the content of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Frequency of count source n: Value set in TRBiPRE register, m: Value set in TRBiPR register
One-shot pulse output time	(n+1)(p+1)/fi fi: Frequency of count source n: Value set in TRBiPRE register, p: Value set in TRBiSC register
Count start conditions	• The TSTART bit in the TRBiCR register is set to 1 (count starts) and the next trigger is generated. • 1 (one-shot starts) is written to the TOSST bit in the TRBiOCR register. • Trigger input to the $\overline{\text{INTj}}$ pin
Count stop conditions	• When reloading completes after timer RBi underflows during the secondary period. • 1 (one-shot stops) is written to the TOSSP bit in the TRBiOCR register. • 0 (count stops) is written to the TSTART bit in the TRBiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBiCR register.
Interrupt request generation timing	In half a cycle of the count source after timer RBi underflows during secondary period (at the same time as the waveform output from the TRBiO pin ends) [timer RBi interrupt].
TRBiO pin function	Pulse output
$\overline{\text{INTj}}$ pin functions	• When the INOSTG bit in the TRBiIOC register is set to 0 ($\overline{\text{INTj}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INTj}}$ interrupt input • When the INOSTG bit in the TRBiIOC register is set to 1 ($\overline{\text{INTj}}$ one-shot trigger enabled): external trigger ($\overline{\text{INTj}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBiPR and TRBiPRE.
Write to timer	• When registers TRBiPRE, TRBiSC, and TRBiPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBiPRE, TRBiSC, and TRBiPR are written during count operation, values are written to the reload registers only. (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBiIOC register. • One-shot trigger select function Refer to **17.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBiSC and TRBiPR.

i = 0 or 1, j = 0 or 5

17.6.1 Timer RBi I/O Control Register (TRBiIOC) (i = 0 or 1) in Programmable Wait One-Shot Generation Mode

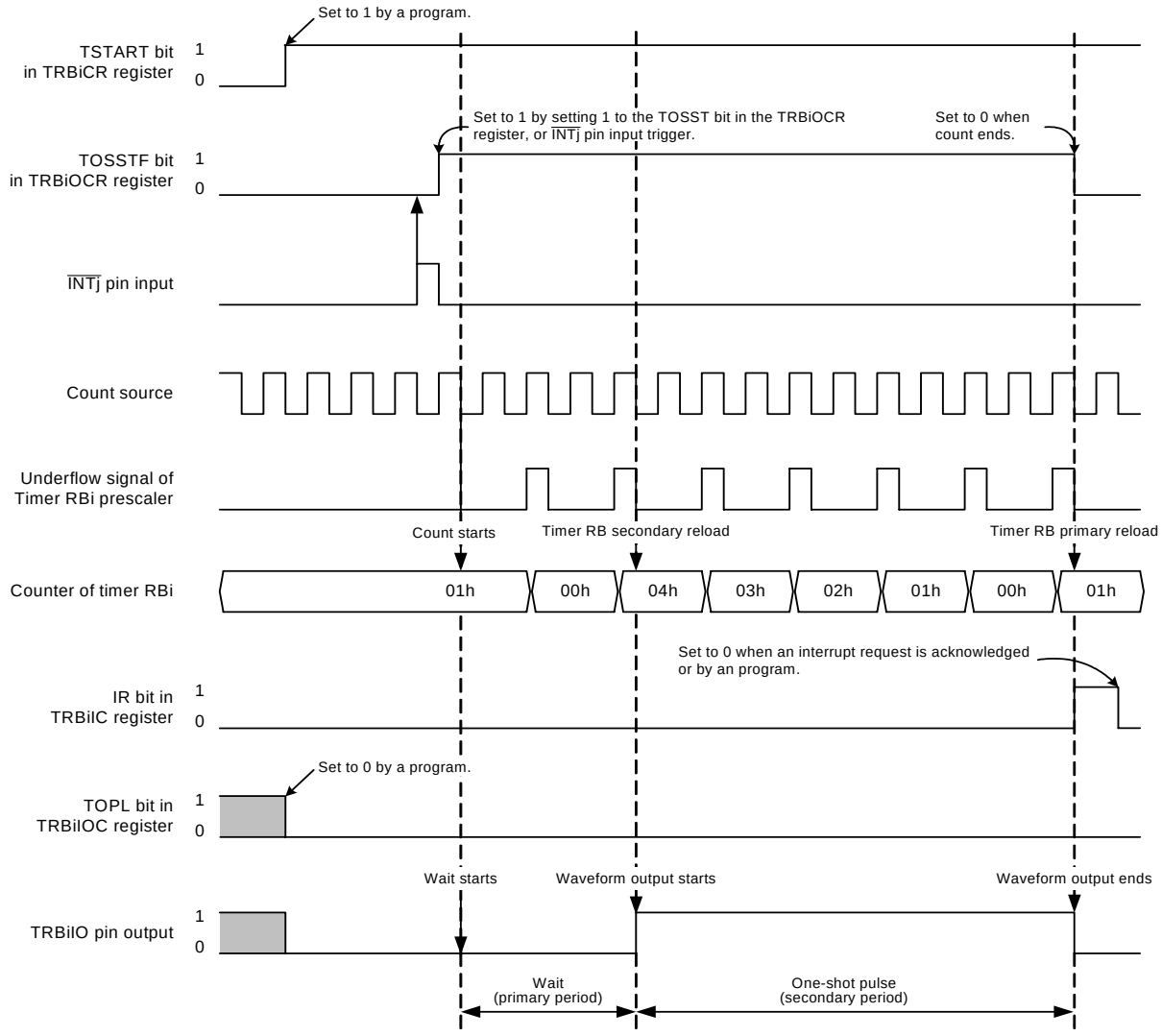
Address 010Ah (TRB0IOC), 009Ah (TRB1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RBi output level select bit	0: High-level output of a one-shot pulse, low-level output when the timer stops or during wait 1: Low-level output of a one-shot pulse, low-level output when the timer stops or during wait	R/W
b1	TOCNT	Timer RBi output enable/disable bit	Set to 0 in programmable wait one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INTj}}$ (j = 0 or 5) pin one-shot trigger disabled (2) 1: $\overline{\text{INTj}}$ (j = 0 or 5) pin one-shot trigger enabled (2)	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **17.5.3 One-Shot Trigger Selection**.
2. A one-shot trigger is input from the $\overline{\text{INT0}}$ pin for timer RB0 and the $\overline{\text{INT5}}$ pin for timer RB1.

17.6.2 Operating Example



The above applies under the following conditions:

TRBiPRE = 01h, TRBiPR = 01h, TRBiSC = 04h
INOSTG = 1 (INTj one-shot trigger enabled)
INOSEG = 1 (edge trigger at the rising edge)

i = 0 or 1
j = 0 or 5

Figure 17.5 Operating Example in Programmable Wait One-Shot Generation Mode

17.7 Notes on Timer RB

- Timer RBi stops counting after a reset. Set the values in the timer RBi and timer RBi prescalers before the count starts.
- Even if the prescaler and timer RBi is read out in 16-bit units, these registers are read 1 byte at a time in the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBiCR register to 0 (count stops) or setting the TOSSP bit in the TRBiOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for one or two cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RBi (1) other than the TCSTF bit. Timer RB starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for one or two cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RBi counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RBi (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RBi:
     TRBiCR, TRBiOCR, TRBiIOC, TRBiMR, TRBiPRE, TRBiSC, and TRBiPR

- When the TSTOP bit in the TRBiCR register is set to 1 during timer operation, timer RBi stops immediately.
- When 1 is written to the TOSST or TOSSP bit in the TRBiOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. When 1 is written to the TOSSP bit during the period between when 1 is written to the TOSST bit and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, when 1 is written to the TOSST bit during the period between when 1 is written to the TOSSP bit and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RJi as the count source for timer RB, set timer RJi in timer mode, pulse output mode, or event counter mode.

17.7.1 Timer Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR register (i = 0 or 1) is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

17.7.2 Programmable Waveform Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

17.7.3 Programmable One-Shot Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously during count operation, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously during count operation, allow three or more cycles of the prescaler underflow for each write interval.

17.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18. Timer RC

Timer RC is a 16-bit timer with four I/O pins.

18.1 Introduction

Timer RC uses either f1, fOCO20M or fOCO-F as its operating clock. Table 18.1 lists the Timer RC Operating Clocks.

Table 18.1 Timer RC Operating Clocks

Condition	Timer RC Operating Clock
The count source is f1, f2, f4, f8, f32, or TRCCLK input. (Bits TCK2 to TCK0 in the TRCCR1 register are set to 000b to 101b.)	f1
The count source is fOCO20M. (Bits TCK2 to TCK0 in the TRCCR1 register are set to 110b.)	fOCO20M
Count source is fOCO-F (bits TCK2 to TCK0 in TRCCR1 register are set to 111b)	fOCO-F

Table 18.2 lists the Timer RC Pin Configuration. Figure 18.1 shows the Timer RC Block Diagram.

Timer RC supports the following three modes:

- Timer mode
  - Input capture function — The counter value is captured to a register, using an external signal as the trigger.
  - Output compare function — A match between the values of a counter and a register is detected. (Pin output can be changed at detection.)

The following two modes use the output compare function:

- PWM mode — Pulses of a given width are output continuously.
- PWM2 mode — A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

For the input capture function, the output compare function, and in PWM mode, settings may be selected independently for each pin.
In PWM2 mode, waveforms are output based on a combination of the counter or the register.

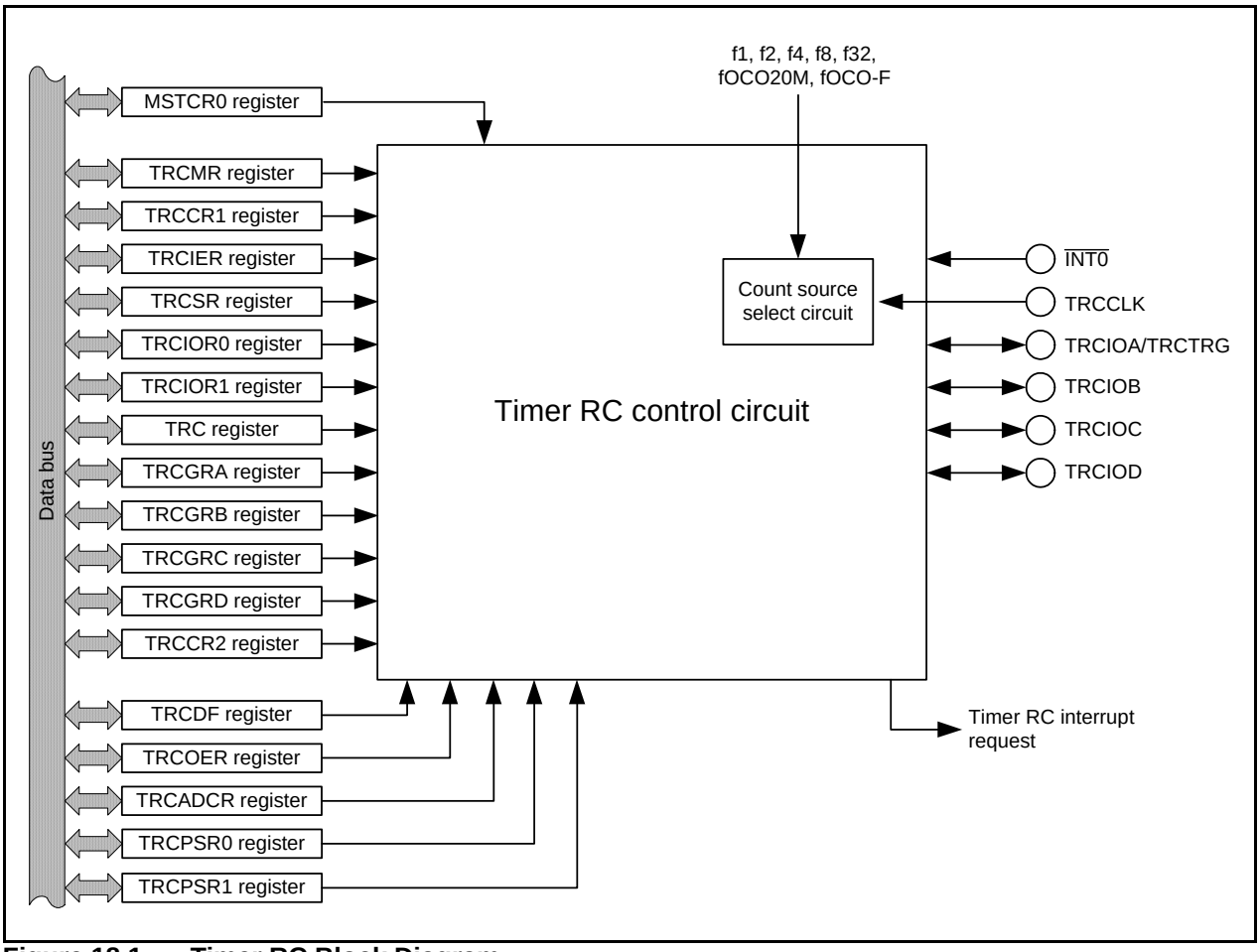


Figure 18.1 Timer RC Block Diagram

Table 18.2 Timer RC Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRCIOA	P0_0	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRCIOB	P6_7, P6_6, or P6_5		
TRCIOC	P6_6		
TRCIOD	P6_5		
TRCCLK	P0_1	Input	External clock input
TRCTRG	P0_0, P0_1, or P0_2	Input	PWM2 mode external trigger input

18.2 Registers

Table 18.3 lists the Registers Associated with Timer RC.

Table 18.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0008h	MSTCR0	Valid	Valid	Valid	Valid	18.2.1 Module Standby Control Register 0 (MSTCR0)
0120h	TRCMR	Valid	Valid	Valid	Valid	18.2.2 Timer RC Mode Register (TRCMR)
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 18.2.3 Timer RC Control Register 1 (TRCCR1) 18.5.1 Timer RC Control Register 1 (TRCCR1) in Timer Mode (Output Compare Function) 18.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode 18.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode
0122h	TRCIER	Valid	Valid	Valid	Valid	18.2.4 Timer RC Interrupt Enable Register (TRCIER)
0123h	TRCSR	Valid	Valid	Valid	Valid	18.2.5 Timer RC Status Register (TRCSR)
0124h	TRCIOR0	Valid	Valid	–	–	Timer RC I/O control register 0, timer RC I/O control register 1 18.2.6 Timer RC I/O Control Register 0 (TRCIOR0) 18.2.7 Timer RC I/O Control Register 1 (TRCIOR1) 18.4.1 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Input Capture Function) 18.4.2 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Input Capture Function) 18.5.2 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Output Compare Function) 18.5.3 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Output Compare Function)
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	18.2.8 Timer RC Counter (TRC)
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	18.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2	–	Valid	Valid	Valid	18.2.10 Timer RC Control Register 2 (TRCCR2)
0131h	TRCDF	Valid	–	–	Valid	18.2.11 Timer RC Digital Filter Function Select Register (TRCDF)
0132h	TRCOER	–	Valid	Valid	Valid	18.2.12 Timer RC Output Master Enable Register (TRCOER)
0133h	TRCADCR	–	Valid	Valid	Valid	18.2.13 Timer RC Trigger Control Register (TRCADCR)
0182h	TRCPSR0	Valid	Valid	Valid	Valid	18.2.14 Timer RC Pin Select Register 0 (TRCPSR0)
0183h	TRCPSR1	Valid	Valid	Valid	Valid	18.2.15 Timer RC Pin Select Register 1 (TRCPSR1)

–: Invalid

18.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	MSTURT2	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	UART0 standby bit	0: Active 1: Standby (1)	R/W
b2	MSTURT2	UART2 standby bit	0: Active 1: Standby (2)	R/W
b3	MSTIIC	SSU, I^2C bus standby bit	0: Active 1: Standby (3)	R/W
b4	MSTLCD	LCD standby bit	0: Active 1: Standby (4)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (5)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	A/D standby bit (6)	0: Active 1: Standby	R/W

Notes:

1. When the MSTURT0 bit is set to 1 (standby), any access to the UART0 associated registers (addresses 00A0h to 00A7h) is disabled.
2. When the MSTURT2 bit is set to 1 (standby), any access to the timer UART2 associated registers (addresses 00A8h to 00BFh) is disabled.
3. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I^2C bus associated registers (addresses 0193h to 019Dh) is disabled.
4. When the MSTLCD bit is set to 1 (standby), any access to the timer LCD associated registers (addresses 0200h to 0237h) is disabled.
5. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
6. When the MSTADC bit is set to 1 (standby), any access to the timer A/D associated registers (addresses 00C0h to 00D9h, 00DCh to 00DFh) is disabled.
   Set the MSTADC bit to 0 (active) when the temperature sensor is used.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

18.2.2 Timer RC Mode Register (TRCMR)

Address 0120h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	BFD	BFC	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	PWM mode of TRCIOB select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	PWM mode of TRCIOC select bit (1)	0: Timer mode 1: PWM mode	R/W
b2	PWMD	PWM mode of TRCIOD select bit (1)	0: Timer mode 1: PWM mode	R/W
b3	PWM2	PWM2 mode select bit	0: PWM 2 mode 1: Timer mode or PWM mode	R/W
b4	BFC	TRCGRC register function select bit (2)	0: General register 1: Buffer register of TRCGRA register	R/W
b5	BFD	TRCGRD register function select bit	0: General register 1: Buffer register of TRCGRB register	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRC count start bit	0: Count stops 1: Count starts	R/W

Notes:
1. These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
2. Set the BFC bit to 0 (general register) in PWM2 mode.

For notes on the TRCMR register in PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.

18.2.3 Timer RC Control Register 1 (TRCCR1)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO20M 1 1 1: fOCO-F (2)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: TRC counter cleared by input capture or by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

18.2.4 Timer RC Interrupt Enable Register (TRCIER)

Address 0122h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by IMFD bit enabled	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVIE	Overflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W

18.2.5 Timer RC Status Register (TRCSR)

Address 0123h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading. (1) [Condition for setting to 1] Refer to **Table 18.4 Conditions for Setting Bit of Each Flag to 1**.	R/W
b1	IMFB	Input-capture/compare-match flag B		R/W
b2	IMFC	Input-capture/compare-match flag C		R/W
b3	IMFD	Input-capture/compare-match flag D		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVF	Overflow flag	[Condition for setting to 0] Write 0 after reading. (1) [Condition for setting to 1] Refer to **Table 18.4 Conditions for Setting Bit of Each Flag to 1**.	R/W

Note:
1. The results of writing to these bits are as follows:
   - The bit is set to 0 when it is first read as 1 and then 0 is written to it.
   - The bit remains unchanged even if it is first read as 0 and then 0 is written to it. (The bit's value remains 1 even if it is set to 1 from 0 after being read as 0 and having 0 written to it.)
   - The bit's value remains unchanged if 1 is written to it.

Table 18.4 Conditions for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input capture Function	Output Compare Function		
IMFA	TRCIOA pin input edge (1)	When the values of registers TRC and TRCGRA match.		
IMFB	TRCIOB pin input edge (1)	When the values of registers TRC and TRCGRB match.		
IMFC	TRCIOC pin input edge (1)	When the values of registers TRC and TRCGRC match. (2)		
IMFD	TRCIOD pin input edge (1)	When the values of registers TRC and TRCGRD match. (2)		
OVF	When the TRC register overflows.			

Notes:
1. Edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in registers TRCIOR0 and TRCIOR1.
2. Includes the condition that bits BFC and BFD are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

18.2.6 Timer RC I/O Control Register 0 (TRCIOR0)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	Function varies according to the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA input pin	R/W
b4	IOB0	TRCGRB control bit	Function varies according to the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

The TRCIOR0 register is enabled in timer mode. It is disabled in PWM mode and PWM2 mode.

18.2.7 Timer RC I/O Control Register 1 (TRCIOR1)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	Function varies according to the operating mode (function).	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	Function varies according to the operating mode (function).	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR1 register is enabled in timer mode. It is disabled in PWM mode and PWM2 mode.

18.2.8 Timer RC Counter (TRC)

Address 0127h to 0126h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Counts a count source. Count operation is increment. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

Access the TRC register in 16-bit units. Do not access it in 8-bit units.

18.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0129h to 0128h (TRCGRA), 012Bh to 012Ah (TRCGRB),
012Dh to 012Ch (TRCGRC), 012Fh to 012Eh (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies according to the operating mode.	R/W

Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

18.2.10 Timer RC Control Register 2 (TRCCR2)

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

18.2.11 Timer RC Digital Filter Function Select Register (TRCDF)

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)	0: Function is not used 1: Function is used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Digital filter function clock select bit (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK0 to TCK2 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

18.2.12 Timer RC Output Master Enable Register (TRCOER)

Address 0132h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOA pin functions as a programmable I/O port)	R/W
b1	EB	TRCIOB output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOB pin functions as a programmable I/O port)	R/W
b2	EC	TRCIOC output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOC pin functions as a programmable I/O port)	R/W
b3	ED	TRCIOD output disable bit (1)	0: Output enabled 1: Output disabled (TRCIOD pin functions as a programmable I/O port)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (output disabled) when a low or high-level signal is applied to the $\overline{\text{INT0}}$ pin depending on POL bit in INT0IC register.)	R/W

Note:
1. These bits are disabled for pins set as input-capture input.

18.2.13 Timer RC Trigger Control Register (TRCADCR)

Address 0133h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	ADTRGDE	ADTRGCE	ADTRGBE	ADTRGAE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGAE	A/D trigger A enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match between registers TRC and TRCGRA	R/W
b1	ADTRGBE	A/D trigger B enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match between registers TRC and TRCGRB	R/W
b2	ADTRGCE	A/D trigger C enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match between registers TRC and TRCGRC	R/W
b3	ADTRGDE	A/D trigger D enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match between registers TRC and TRCGRD	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.2.14 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	TRCIOASEL1	TRCIOASEL0	—	TRCCLKSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCCLKSEL0	TRCCLK pin select bit (1)	0: TRCCLK pin not used 1: P0_1 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b3 b2 0 0: TRCIOA/TRCTRG pin not used 0 1: TRCIOA/TRCTRG pin assigned to P0_0 1 0: TRCTRG pin assigned to P0_1 (1) 1 1: TRCTRG pin assigned to P0_2	R/W
b3	TRCIOASEL1			R/W
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P6_7 assigned 1 0: P6_6 assigned (2) 1 1: P6_5 assigned (3)	R/W
b5	TRCIOBSEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Pins TRCCLK and TRCTRG cannot be assigned to P0_1 at the same time.
2. When the TRCIOCSEL0 bit in the TRCPSR1 register is set to 1 (TRCIOC pin assigned to P6_6), P6_6 functions as the TRCIOC pin regardless of the content of bits TRCIOBSEL1 to TRCIOBSEL0.
3. When the TRCIODSEL0 bit in the TRCPSR1 register is set to 1 (TRCIOD pin assigned to P6_5), P6_5 functions as the TRCIOD pin regardless of the content of bits TRCIOBSEL1 to TRCIOBSEL0.

The TRCPSR0 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation. If the assignment of the timer RC pins is changed, an edge may occur depending on the changed pin level, causing the TRC register to be set to 0000h.

18.2.15 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TRCIODSEL0	—	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	0: TRCIOC pin not used 1: P6_6 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRCIODSEL0	TRCIOD pin select bit	0: TRCIOD pin not used 1: P6_5 assigned	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

The TRCPSR1 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

18.3 Common Items for Multiple Modes

18.3.1 Count Source

The method of selecting the count source is common to all modes.
Table 18.5 lists the Count Source Selection, and Figure 18.2 shows the Count Source Block Diagram.

Table 18.5 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	The count source is selected by bits TCK2 to TCK0 in TRCCR1 register
fOCO20M fOCO-F	- The FRA00 bit in the FRA0 register set to 1 (high-speed on-chip oscillator on). - Bits TCK2 to TCK0 in the TRCCR1 register are set to 110b (fOCO20M). - Bits TCK2 to TCK0 in TRCCR1 register are set to 111b (fOCO-F)
External signal input to TRCCLK pin	- Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) - The corresponding direction bit in the direction register is set is set to 0 (input mode)

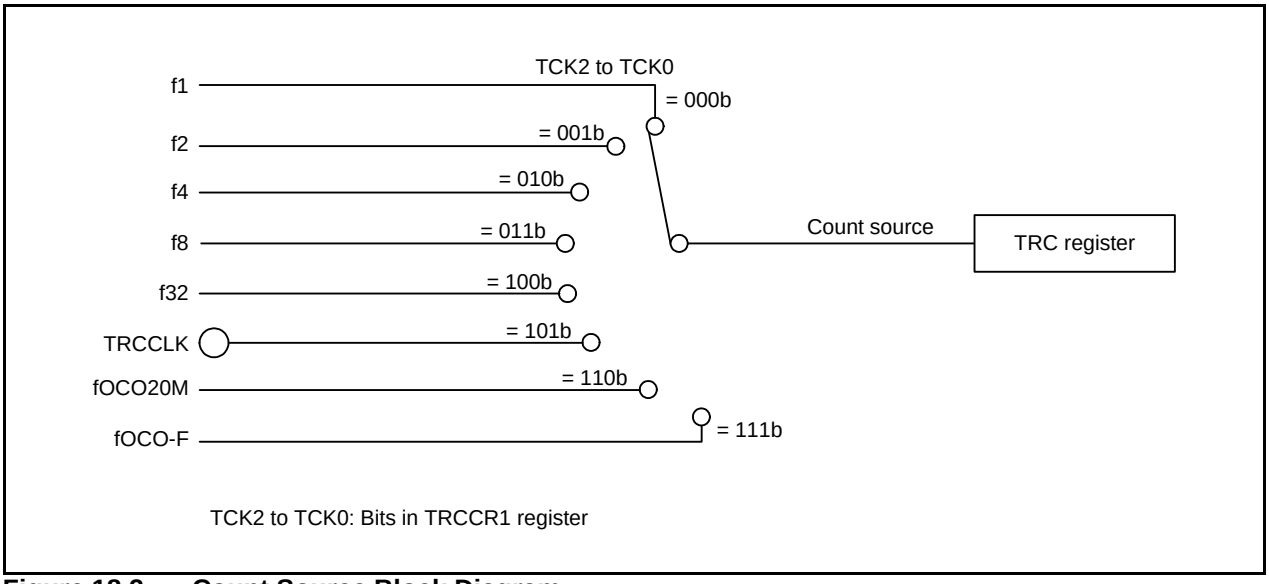


Figure 18.2 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be set to three cycles or more of the timer RC operation clock. (See **Table 18.1 Timer RC Operating Clocks.**)
To select fOCO20M or fOCO-F as the count source, set the FRA00 bit in the FRA0 register set to 1 (high-speed on-chip oscillator on), and then set bits TCK2 to TCK0 in the TRCCR1 register to 110b (fOCO20M) or 111b (fOCO-F).

18.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register of the TRCGRA or TRCGRB register.

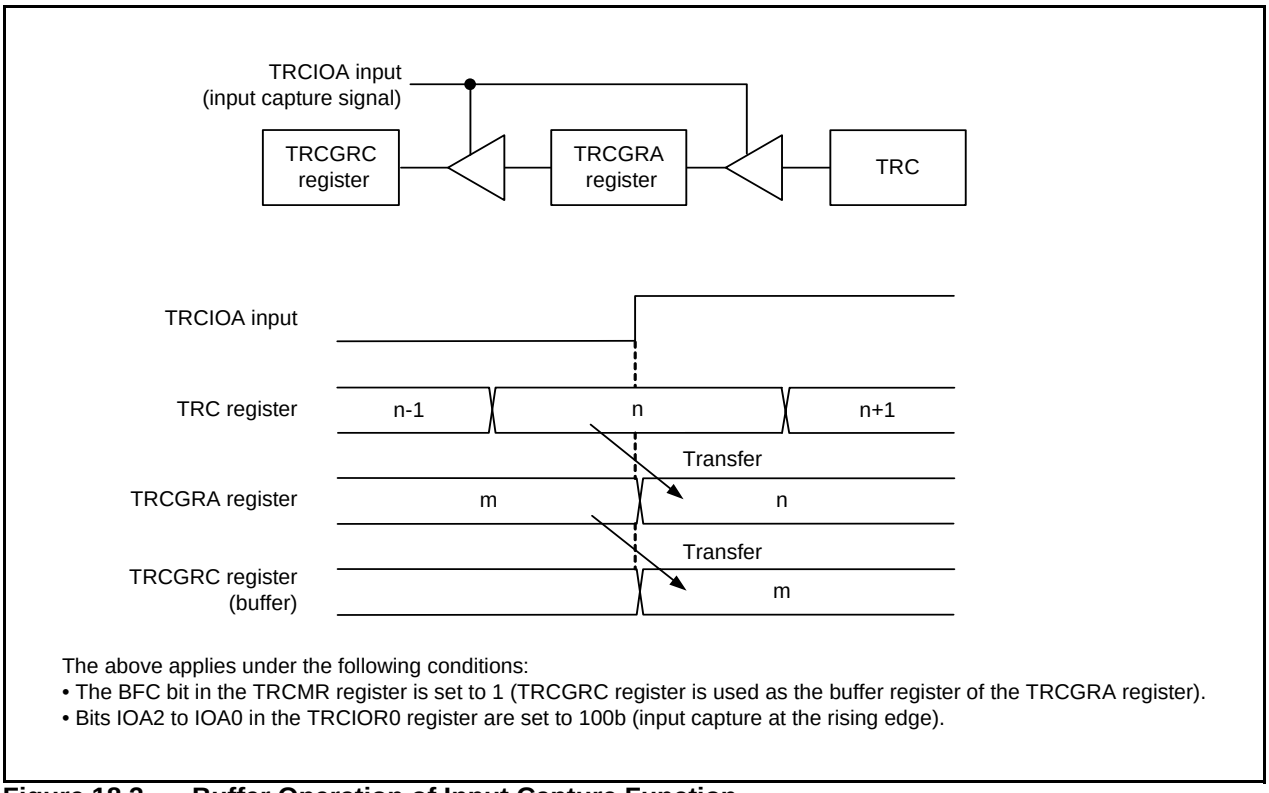
- Buffer register of TRCGRA register: TRCGRC register
- Buffer register of TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 18.6 lists the Buffer Operation in Each Mode, Figure 18.3 shows the Buffer Operation of Input Capture Function, and Figure 18.4 shows the Buffer Operation of Output Compare Function.

Table 18.6 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	The content of the TRCGRA (TRCGRB) register is transferred to the buffer register.
Output compare function PWM mode	Compare match between the TRC register and the TRCGRA (TRCGRB) register	The content of the buffer register is transferred to the TRCGRA (TRCGRB) register.
PWM2 mode	• Compare match between the TRC register and the TRCGRA register • TRCTRG pin trigger input	The content of the buffer register (TRCGRD) is transferred to the TRCGRB register.



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (TRCGRC register is used as the buffer register of the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 100b (input capture at the rising edge).

Figure 18.3 Buffer Operation of Input Capture Function

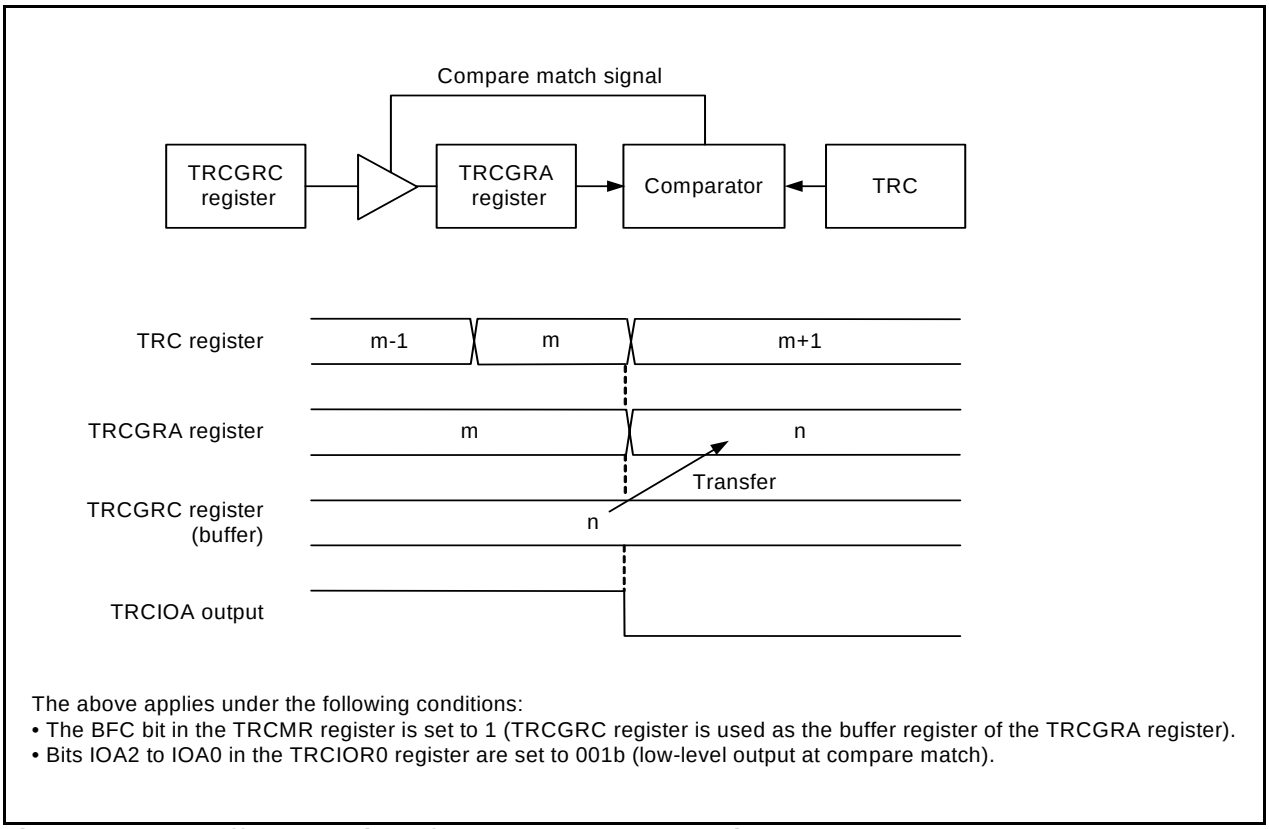


Figure 18.4 Buffer Operation of Output Compare Function

Make the following settings in timer mode.

- To use the TRCGRC register as the buffer register of the TRCGRA register:
  Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register of the TRCGRB register:
  Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

When the TRCGRC or TRCGRD register is also used as the buffer register for the output compare function, in PWM mode, or PWM2 mode, the IMFC or IMFD bit in the TRCSR register is set to 1 by a compare match with the TRC register.

When the TRCGRC register or TRCGRD register is also used as the buffer register for the input capture function, the IMFC or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIOC or TRCIOD pin.

18.3.3 Digital Filter

The input to TRCTRG or TRCIOj (j = A, B, C, or D) is sampled, and the level is determined when three matches occur. The digital filter function and sampling clock can be selected using the TRCDF register. Figure 18.5 shows a Block Diagram of Digital Filter.

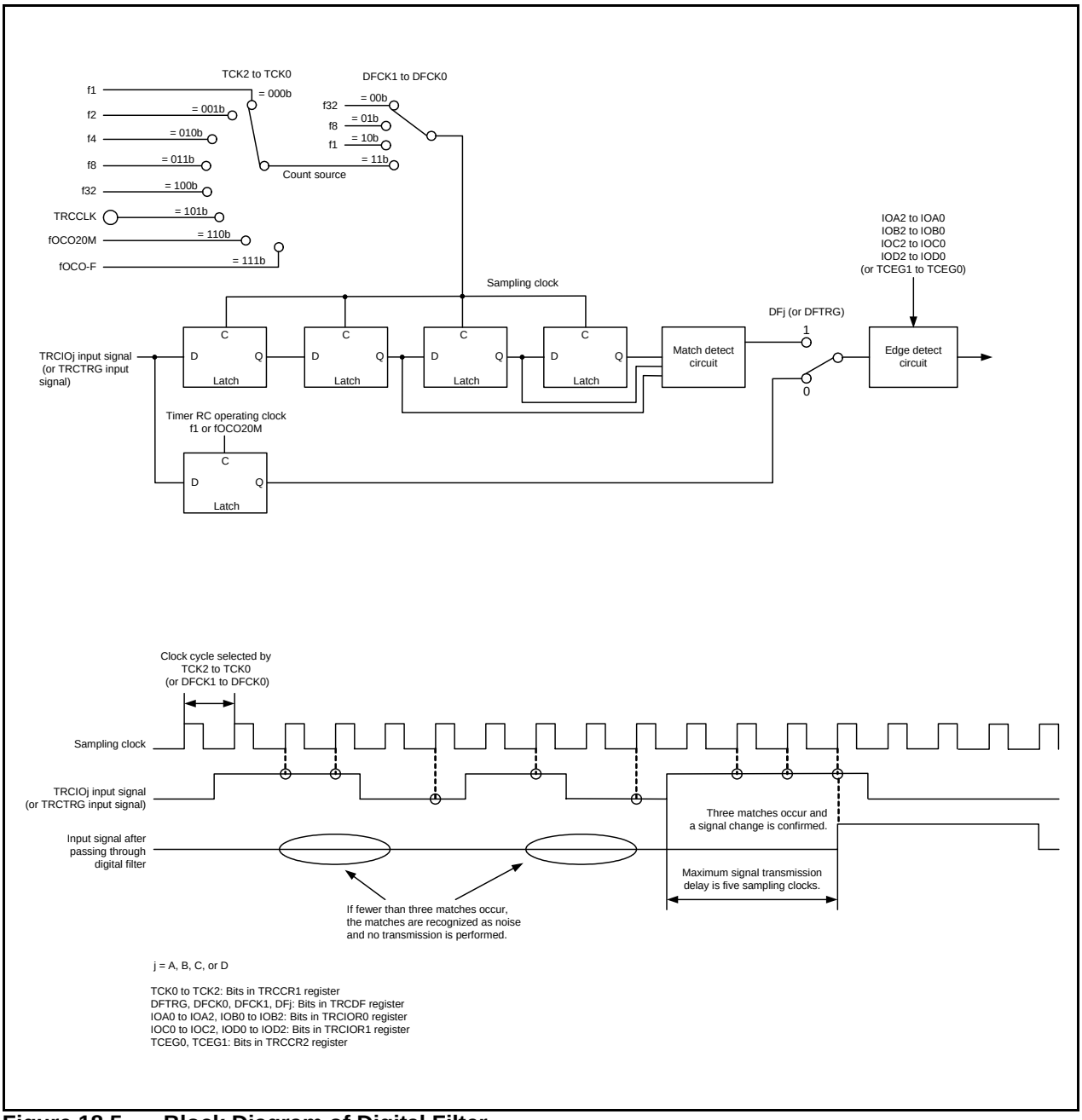


Figure 18.5 Block Diagram of Digital Filter

18.3.4 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, PWM mode, or PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the $\overline{\text{INT0}}$ pin.
A pin used for output by the timer mode's output compare function, PWM mode, or PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled).
When the PTO bit in the TRCOER register is 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), if a low-level (or high-level) signal is input to the $\overline{\text{INT0}}$ pin, bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as a programmable I/O port) after one or two cycles of the timer RC operating clock. For details of the timer RC operating clock, refer to **Table 18.1 Timer RC Operating Clocks**.

Make the following settings to use this function.

- Set the pin state following forced cutoff of pulse output (high impedance (input), low-level output, or high-level output). (Refer to **7. I/O Ports**.)
- Set the INT0EN bit to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge) in the INTEN register.
- Set the POL bit in the INT0IC register to select a rising or falling edge.
  When the POL bit is set to 0 (falling edge), the pulse output is forcibly cut off at the falling edge of the $\overline{\text{INT0}}$ pin.
  When the POL bit is set to 1 (rising edge), the pulse output is forcibly cut off at the rising edge of the $\overline{\text{INT0}}$ pin.
- Set the direction registers for the I/O ports selected as $\overline{\text{INT0}}$ to input mode:
  When INT0 is assigned to P3_0 by the INT0SEL0 bit in the INTSR register, set the PD3_0 bit in the PD3 register to 0 (input mode).
  When INT0 is assigned to P0_3 by the INT0SEL0 bit in the INTSR register, set the PD0_3 bit in the PD0 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F0 and INT0F1 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt requested) in accordance with the setting of the POL bit and a change in the $\overline{\text{INT0}}$ pin input (refer to **12.8 Notes on Interrupts**).
For details on interrupts, refer to **12. Interrupts**.

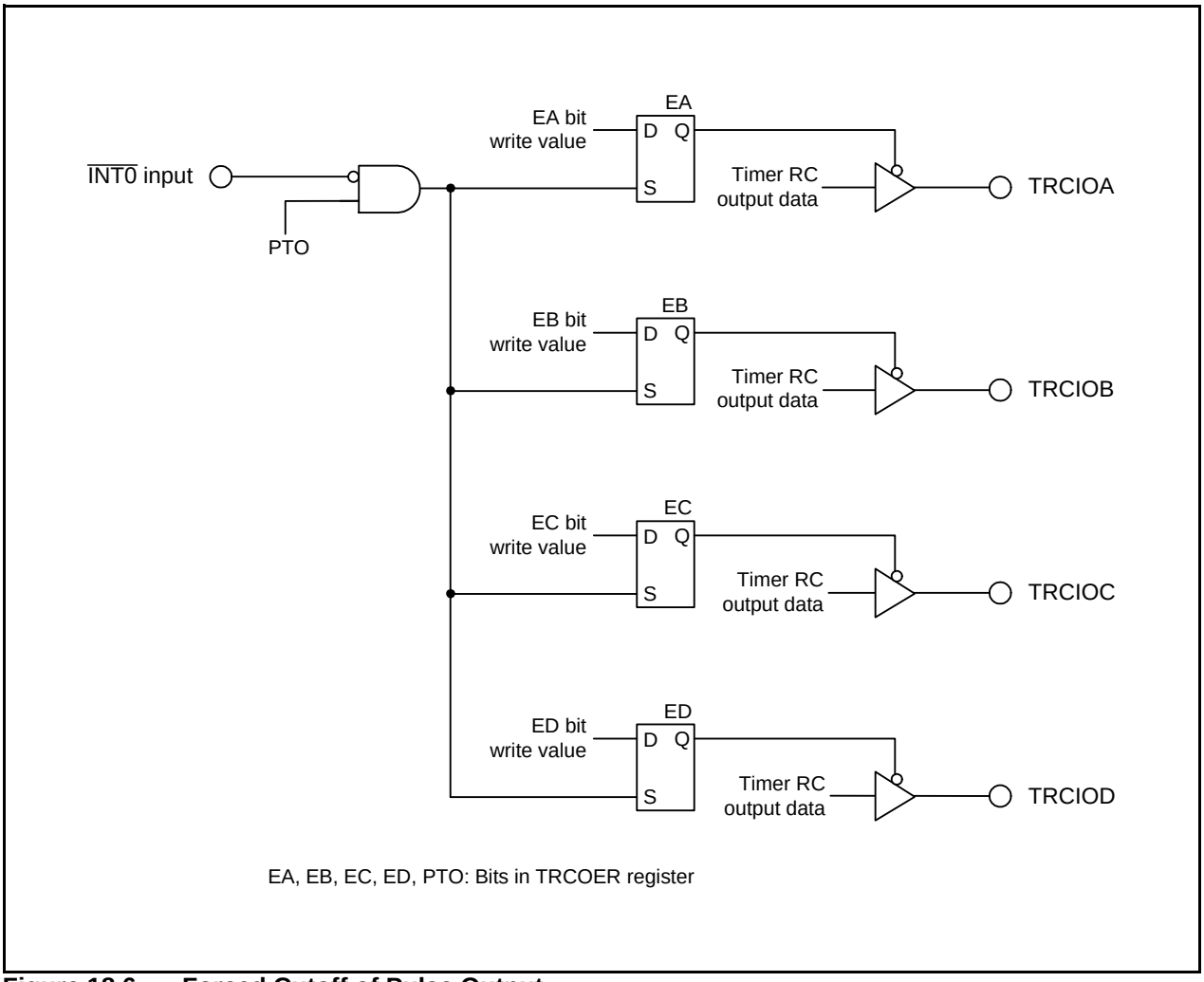


Figure 18.6 Forced Cutoff of Pulse Output

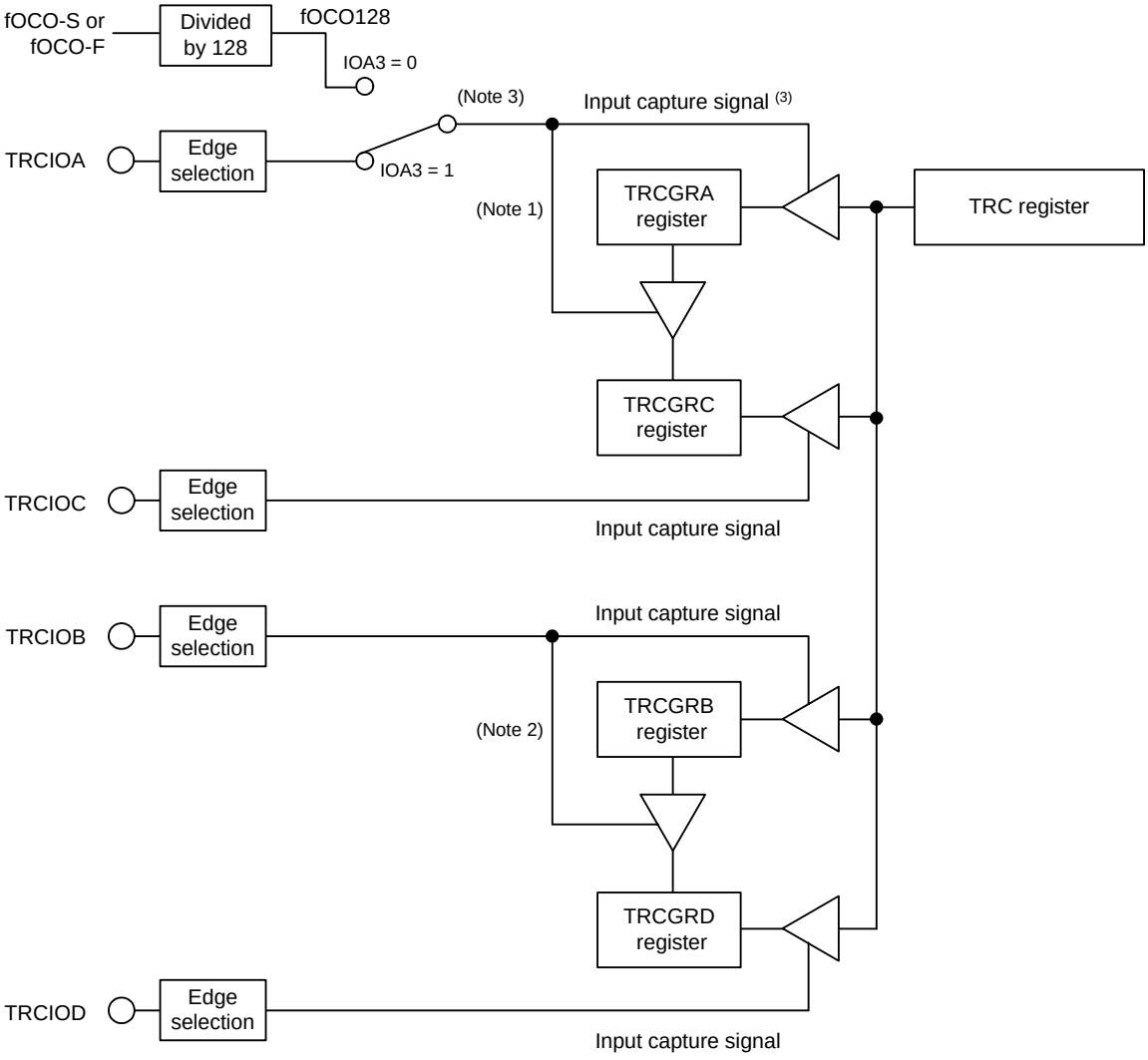
18.4 Timer Mode (Input Capture Function)

This function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the content of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin. Table 18.7 lists the Input Capture Function Specifications, Figure 18.7 shows a Block Diagram of Input Capture Function, Table 18.8 lists the Functions of TRCGRj Register when Using Input Capture Function, and Figure 18.8 shows an Operating Example of Input Capture Function.

Table 18.7 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO20M, fOCO-F, or external signal (rising edge) input to the TRCCLK pin
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free-running operation): 1/fk × 65,536 fk: Frequency of count source • The CCLR bit in the TRCCR1 register is set to 1 (TRC register is set to 0000h by TRCGRA compare match): 1/fk × (n + 1) n: Value set in TRCGRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before the count stops.
Interrupt request generation timing	• Input capture (active edge of the TRCIOj input) • TRC register overflows
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or input capture input (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Input-capture input pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Input-capture input active edge selection Rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **18.3.2 Buffer Operation**.) • Digital filter (Refer to **18.3.3 Digital Filter**.) • Timing for setting the TRC register to 0000h Overflow or input capture

j = A, B, C, or D



IOA3: Bit in TRCIOR0 register

Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)
3. The trigger input of the TRCGRA register can select the TRCIOA pin input or fOCO128 signal.

Figure 18.7 Block Diagram of Input Capture Function

18.4.1 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Input Capture Function)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Input capture to the TRCGRA register at the rising edge 0 1: Input capture to the TRCGRA register at the falling edge 1 0: Input capture to the TRCGRA register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 1 (input capture) for the input capture function.	R/W
b3	IOA3	TRCGRA input-capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Input capture to the TRCGRB register at the rising edge 0 1: Input capture to the TRCGRB register at the falling edge 1 0: Input capture to the TRCGRB register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

18.4.2 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Input Capture Function)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Input capture to the TRCGRC register at the rising edge 0 1: Input capture to the TRCGRC register at the falling edge 1 0: Input capture to the TRCGRC register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 1 (input capture) for the input capture function.	R/W
b3	IOC3	TRCGRC register function select bit	Set to 1.	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Input capture to the TRCGRD register at the rising edge 0 1: Input capture to the TRCGRD register at the falling edge 1 0: Input capture to the TRCGRD register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b7	IOD3	TRCGRD register function select bit	Set to 1.	R/W

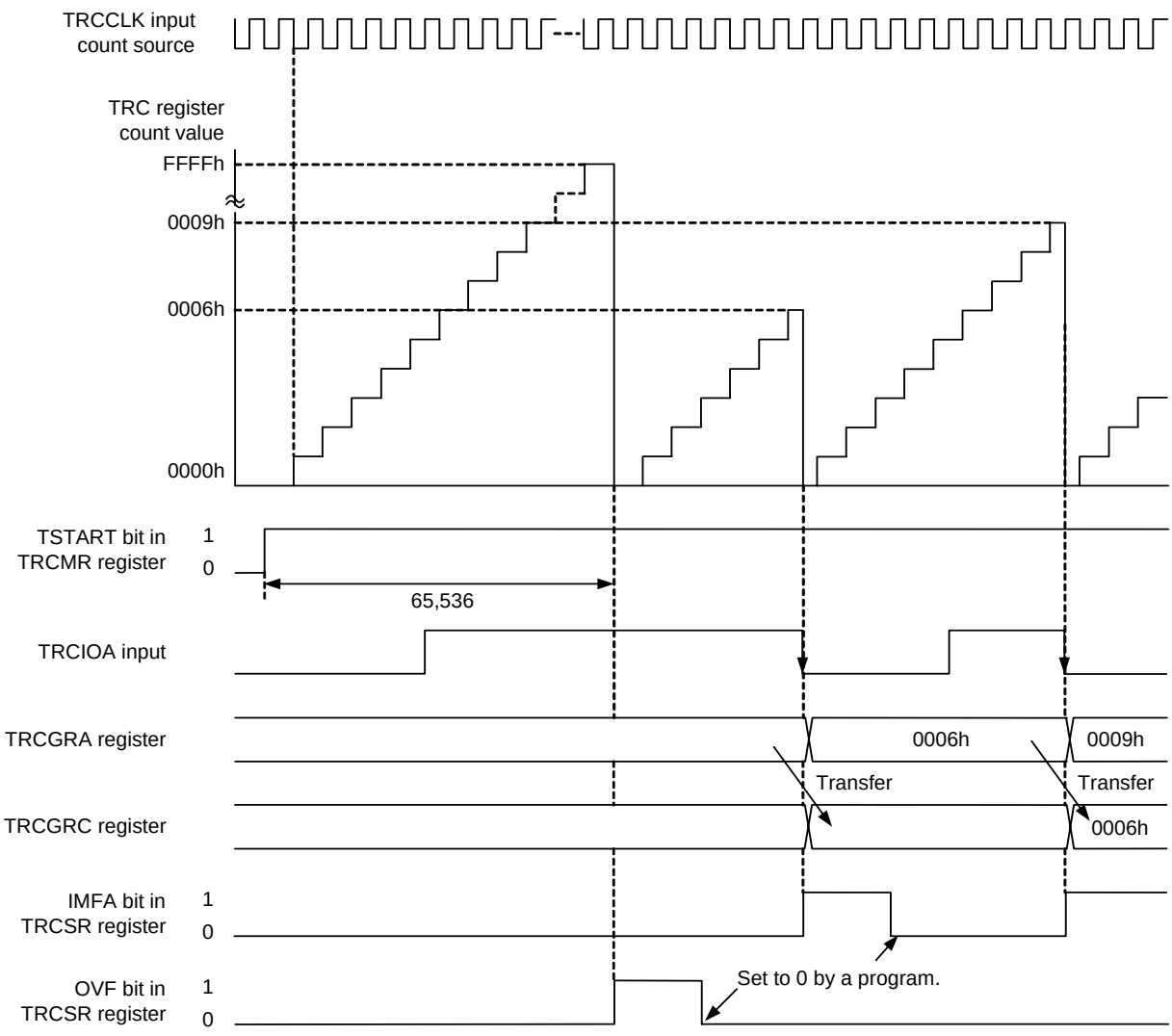
Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Table 18.8 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	–	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer registers. Can be used to retain the transferred value from the general register. (Refer to **18.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

18.4.3 Operating Example



The above applies under the following conditions:

- The CCLR bit in the TRCCR1 register is set to 1 (TRC counter cleared by input capture).
- Bits TCK2 to TCK0 in the TRCCR1 register are set to 101b (TRCCLK input selected as the count source).
- Bits IOA2 to IOA0 in the TRCIORA register are set to 101b (input capture at the falling edge of the TRCIOA input).
- The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register of the TRCGRA register).

Figure 18.8 Operating Example of Input Capture Function

18.5 Timer Mode (Output Compare Function)

This function detects when the contents of the TRC register (counter) and the TRCGRj register (j = A, B, C, or D) match (compare match). When a match occurs, a signal is output from the TRCIOj pin at a given level. The output compare function, or other mode or function, can be selected for each individual pin.
Table 18.9 lists the Output Compare Function Specifications, Figure 18.9 shows a Block Diagram of Output Compare Function, Table 18.10 lists the Functions of TRCGRj Register when Using Output Compare Function, and Figure 18.10 shows an Operating Example of Output Compare Function.

Table 18.9 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO20M, fOCO-F, or external signal input to the TRCCLK pin (rising edge)
Count operation	Increment
Count periods	• The CCLR bit in the TRCCR1 register is set to 0 (free-running operation): 1/fk × 65,536 fk: Frequency of count source • The CCLR bit in the TRCCR1 register is set to 1 (TRC register is set to 0000h by TRCGRA compare match): 1/fk × (n + 1) n: Value set in TRCGRA register
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with the TRCGRA register). 0 (count stops) is written to the TSTART bit in the TRCMR register. The output compare output pin retains the output level before the count stops, the TRC register retains a value before the count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register). The count stops at a compare match with the TRCGRA register. The output-compare output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match.) • TRC register overflow
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or output compare output (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Output-compare output pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Output level selection at the compare match Low-level output, High-level output, or toggle output • Initial output level selection Selectable output level for the period from the count start to the compare match • Timing for setting the TRC register to 0000h Overflow or compare match with the TRCGRA register • Buffer operation (Refer to **18.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **18.3.4 Forced Cutoff of Pulse Output**.) • Timer RC can be used as an internal timer by disabling the timer RC output • Changing output pins for registers TRCGRC and TRCGRD TRCGRC can be used for output control of the TRCIOA pin and TRCGRD can be used for output control of the TRCIOB pin. • A/D trigger generation

j = A, B, C, or D

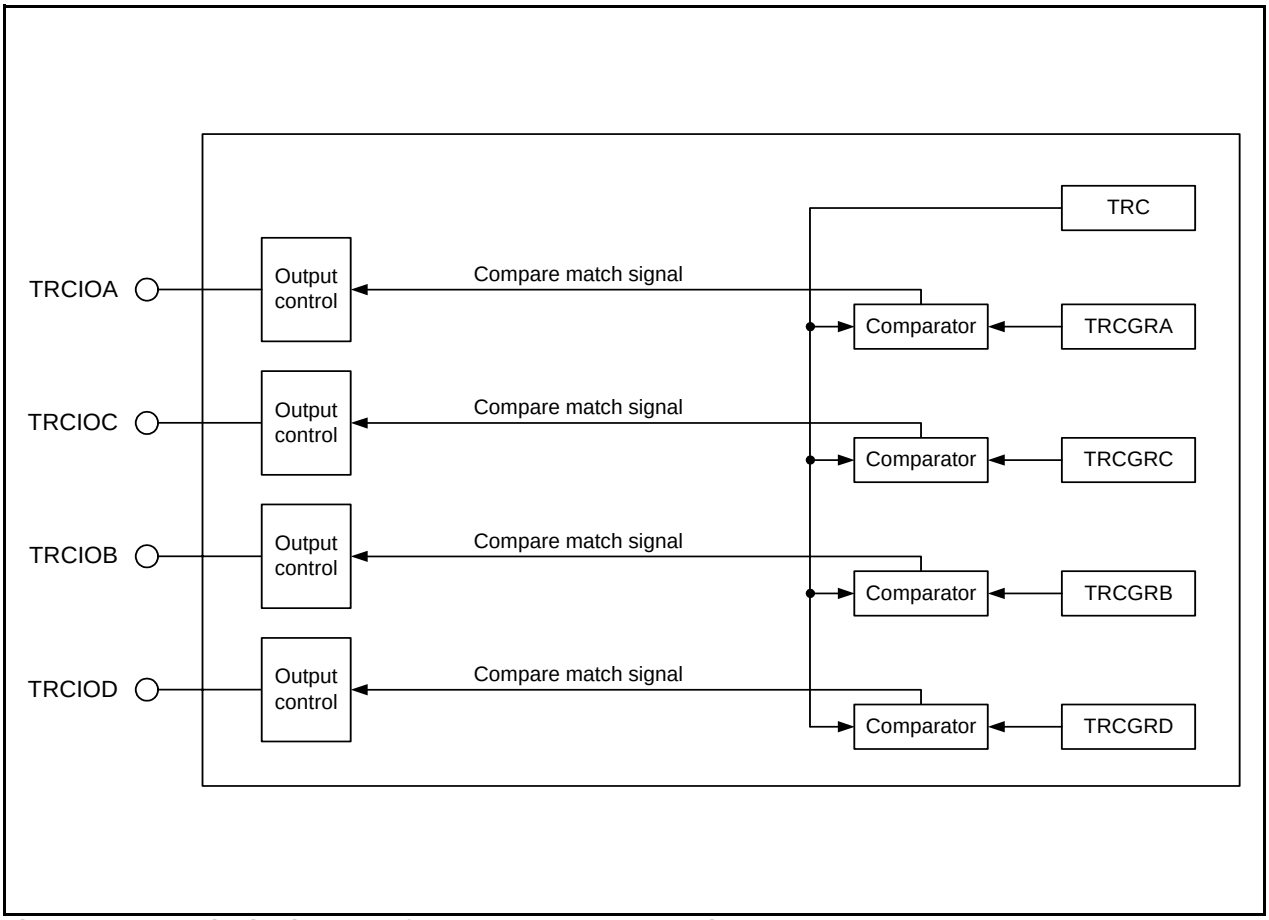


Figure 18.9 Block Diagram of Output Compare Function

18.5.1 Timer RC Control Register 1 (TRCCR1) in Timer Mode (Output Compare Function)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1, 2)	0: Initial output at low 1: Initial output at high	R/W
b1	TOB	TRCIOB output level select bit (1, 2)		R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO20M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.6 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

Table 18.10 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	–	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Write the next compare value to one of these registers. (Refer to **18.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

18.5.2 Timer RC I/O Control Register 0 (TRCIOR0) in Timer Mode (Output Compare Function)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Pin output by compare match is disabled (TRCIOA pin functions as a programmable I/O port) 0 1: Low-level output at compare match with the TRCGRA register 1 0: High-level output at compare match with the TRCGRA register 1 1: Toggle output at compare match with the TRCGRA register	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	IOA3	TRCGRA input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Pin output by compare match is disabled (TRCIOB pin functions as a programmable I/O port) 0 1: Low-level output at compare match with the TRCGRB register 1 0: High-level output at compare match with the TRCGRB register 1 1: Toggle output at compare match with the TRCGRB register	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 0 (output compare) for the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

18.5.3 Timer RC I/O Control Register 1 (TRCIOR1) in Timer Mode (Output Compare Function)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Pin output by compare match is disabled 0 1: Low-level output at compare match with the TRCGRC register 1 0: High-level output at compare match with the TRCGRC register 1 1: Toggle output at compare match with the TRCGRC register	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Pin output by compare match is disabled 0 1: Low-level output at compare match with the TRCGRD register 1 0: High-level output at compare match with the TRCGRD register 1 1: Toggle output at compare match with the TRCGRD register	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 0 (output compare) for the output compare function.	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in theTRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

18.5.4 Timer RC Control Register 2 (TRCCR2) in Timer Mode (Output Compare Function)

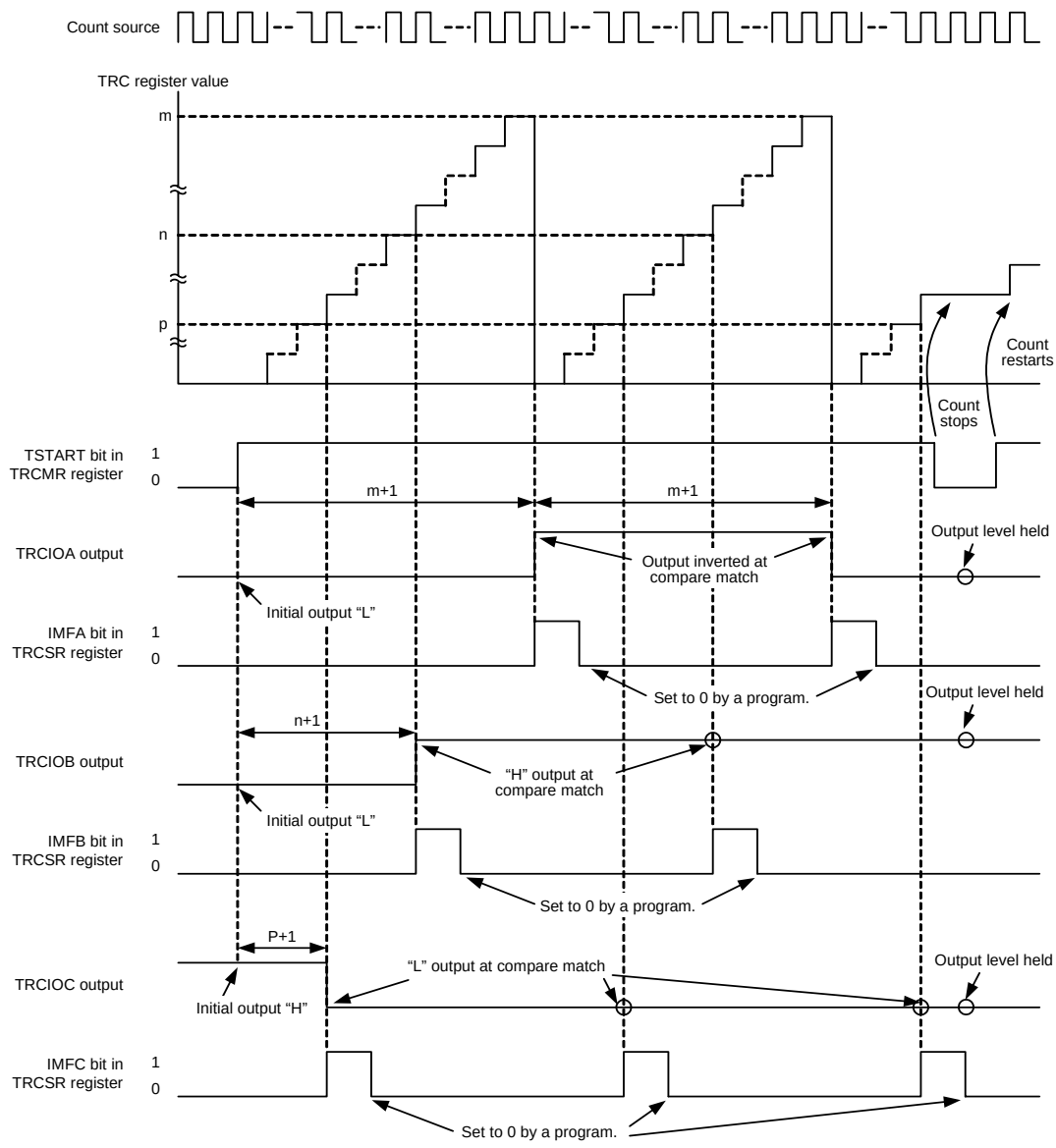
Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

18.5.5 Operating Example



m: Value set in TRCGRA register
n: Value set in TRCGRB register
p: Value set in TRCGRC register

The above applies under the following conditions:

- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
- Bits EA, EB, and EC in the TRCOER register are set to 0 (TRCIOA, TRCIOB, and TRCIOC pin output enabled).
- The CCLR bit in the TRCCR1 register is set to 1 (TRC register is set to 0000h by compare match with TRCGRA register).
- Bits TOA and TOB in the TRCCR1 register are are set to 0 (initial output at low until compare match) and the TOC bit is set to 1 (initial output at high until compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted by TRCGRA compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 010b (TRCIOB high-level output at TRCGRB compare match).
- Bits IOC2 to IOC2 in the TRCIOR1 register are set to 001b (TRCIOC low-level output at TRCGRC compare match).
- The CSEL bit in the TRCCR2 register is set to 0 (TRC count continues after TRCGRA compare match).

Figure 18.10 Operating Example of Output Compare Function

18.5.6 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Each pin output can be controlled as follows:

- TRCIOA output is controlled by the values of registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values of registers TRCGRB and TRCGRD.

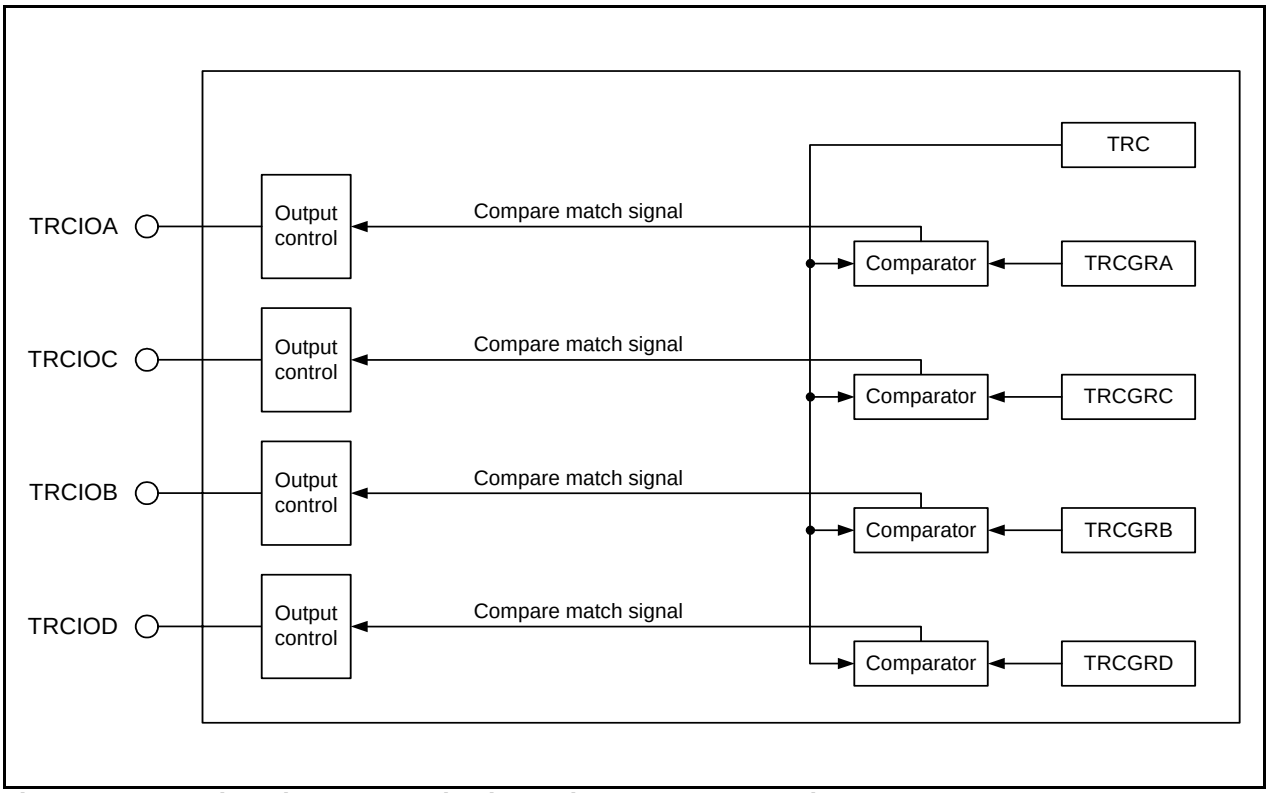
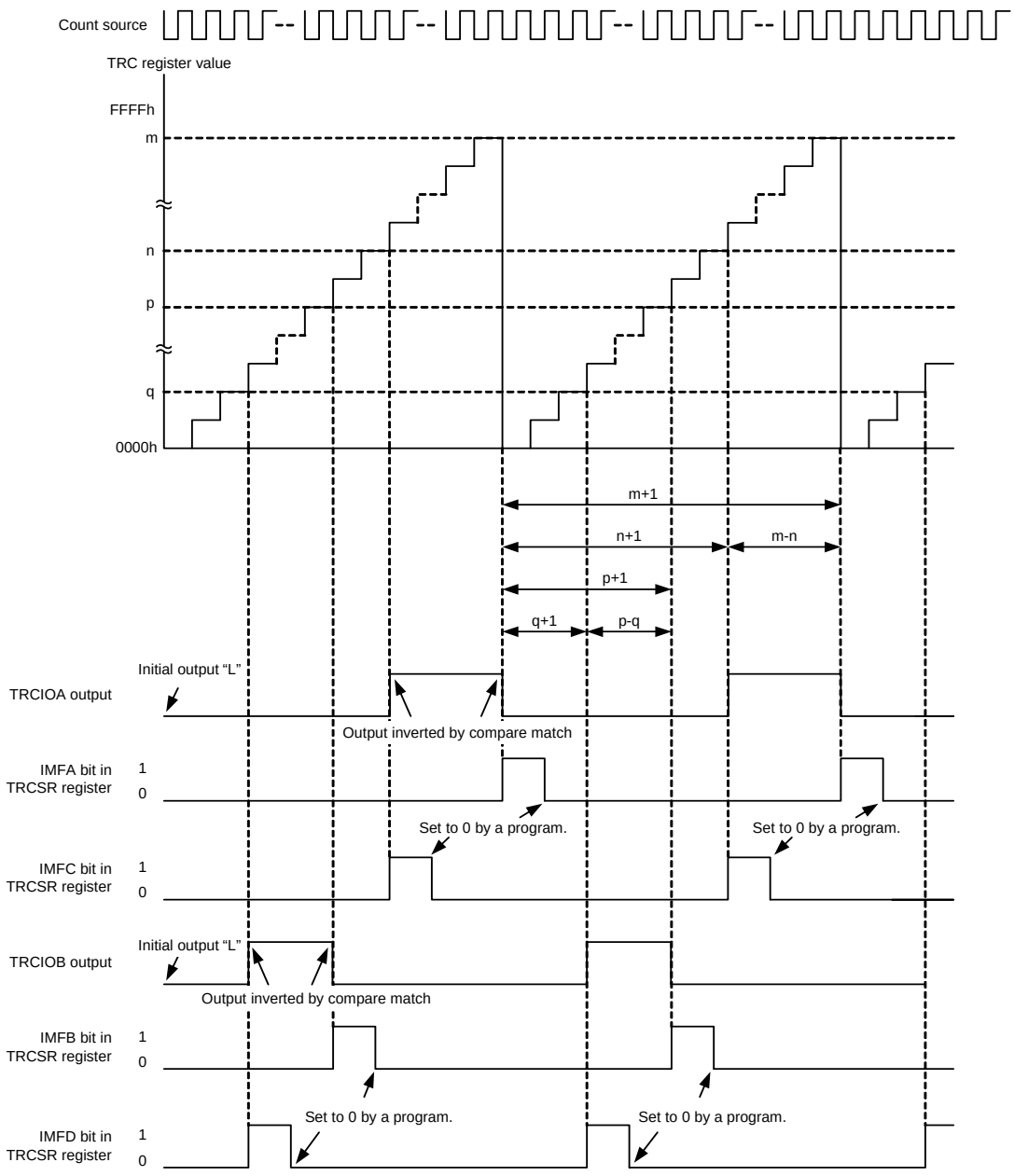


Figure 18.11 Changing Output Pins in Registers TRCGRC and TRCGRD

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 18.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.



m: Value set in TRCGRA register
n: Value set in TRCGRC register
p: Value set in TRCGRB register
q: Value set in TRCGRD register

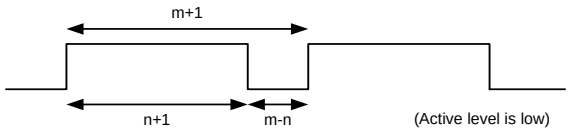
The above applies under the following conditions:
Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
Bits EA and EB in the TRCOER register are set to 0 (TRCIOA and TRCIOB pin output enabled).
The CCLR bit in the TRCCR1 register are set to 1 (TRC register is set to 0000h by compare match with the TRCGRA register).
Bits TOA and TOB in the TRCCR1 register are set to 0 (initial output at low until compare match).
Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted by TRCGRA register compare match).
Bits IOB2 to IOB0 in the TRCIOR0 register are set to 011b (TRCIOB output inverted by TRCGRB register compare match).
Bits IOC2 to IOC0 in the TRCIOR1 register are set to 011b (TRCIOA output inverted by TRCGRC register compare match).
The IOC3 bit in the TRCIOR1 register are set to 0 (TRCIOA output register).
Bits IOD2 to IOD0 in the TRCIOR1 register are set to 011b (TRCIOB output inverted by TRCGRD register compare match).
The IOD3 bit in the TRCIOR1 register are set to 0 (TRCIOB output register).
The CSEL bit in the TRCCR2 register are set to 0 (TRC count continues after compare match).

Figure 18.12 Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin

18.6 PWM Mode

This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. PWM mode or timer mode can be selected for each individual pin. (However, the TRCGRA register cannot be used for timer mode since the register is used when using any pin for PWM mode.)
Table 18.11 lists the PWM Mode Specifications, Figure 18.13 shows a Block Diagram of PWM Mode, Table 18.12 lists the Functions of TRCGRh Register in PWM Mode, and Figures 18.14 and 18.15 show Operating Examples in PWM Mode.

Table 18.11 PWM Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO20M, fOCO-F, or external signal (rising edge) input to the TRCCLK pin
Count operation	Increment
PWM waveform	PWM period: 1/fk × (m + 1) Active level width: 1/fk × (m - n) Inactive width: 1/fk × (n + 1) fk: Frequency of count source m: Value set in TRCGRA register n: Value set in TRCGRj register 
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with the TRCGRA register). 0 (count stops) is written to the TSTART bit in the TRCMR register. The PWM output pin retains the output level before the count stops, The TRC register retains a value before the count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register). The count stops at a compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match) • TRC register overflow
TRCIOA pin function	Programmable I/O port
TRCIOB, TRCIOC, and TRCIOD pins function	Programmable I/O port or PWM output (selectable for each individual pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• One to three pins selectable as PWM pins One or more of pins TRCIOB, TRCIOC, and TRCIOD • Active level selectable for each individual pin • Initial level selectable for each individual pin • Buffer operation (Refer to **18.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **18.3.4 Forced Cutoff of Pulse Output**.) • A/D trigger generation

j = B, C, or D
h = A, B, C, or D

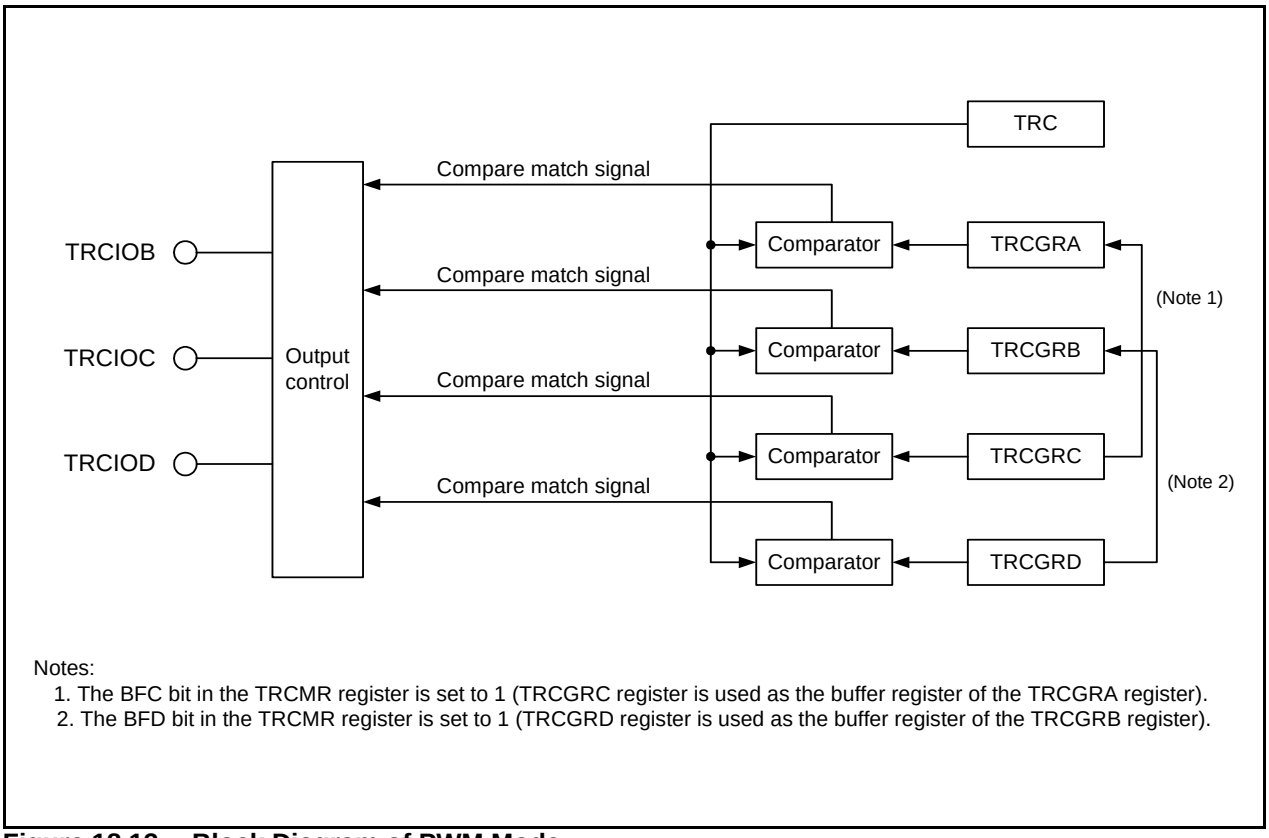


Figure 18.13 Block Diagram of PWM Mode

18.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM mode.	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Initial output selected as non-active level 1: Initial output selected as active level	R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO20M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.6 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

18.6.2 Timer RC Control Register 2 (TRCCR2) in PWM Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

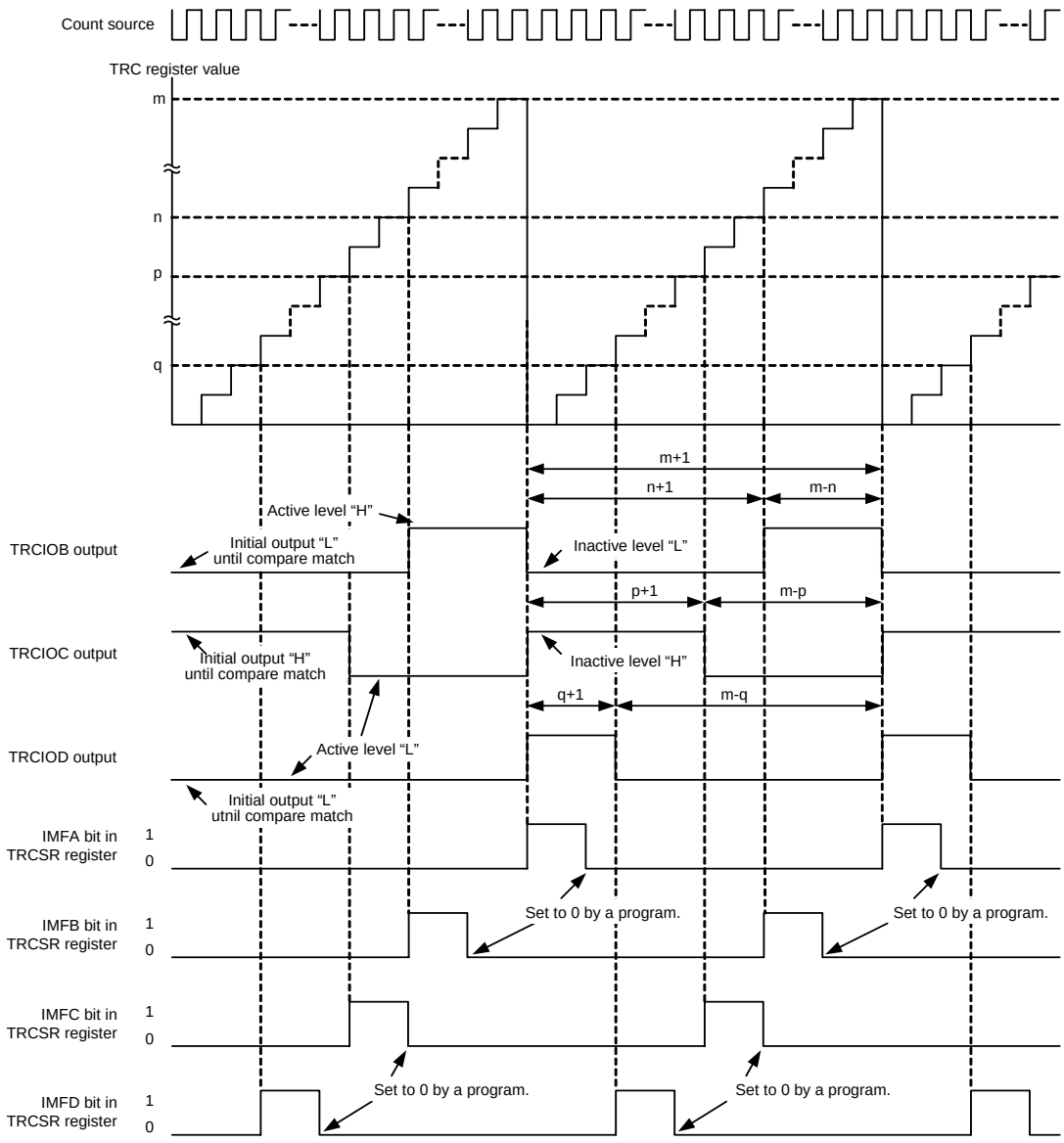
Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

Table 18.12 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	–	General register. Set the PWM period.	–
TRCGRB	–	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BFC = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Set the next PWM period. (Refer to **18.3.2 Buffer Operation**.)	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **18.3.2 Buffer Operation**.)	TRCIOB

h = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. The output level does not change even if a compare match occurs when the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

18.6.3 Operating Example



The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer registers).
- Bits EB, EC, and ED in the TRCOER register are set to 0 (TRCIOB, TRCIOC, and TRCIOD pin output enabled).
- Bits TOB and TOC in the TRCCR1 register are set to 0 (inactive level) and the TOD bit is set to 1 (active level).
- The POLB bit in the TRCCR2 register is set to 1 (high active), bits POLC and POLD are set to 0 (low active).

Figure 18.14 Operating Example in PWM Mode

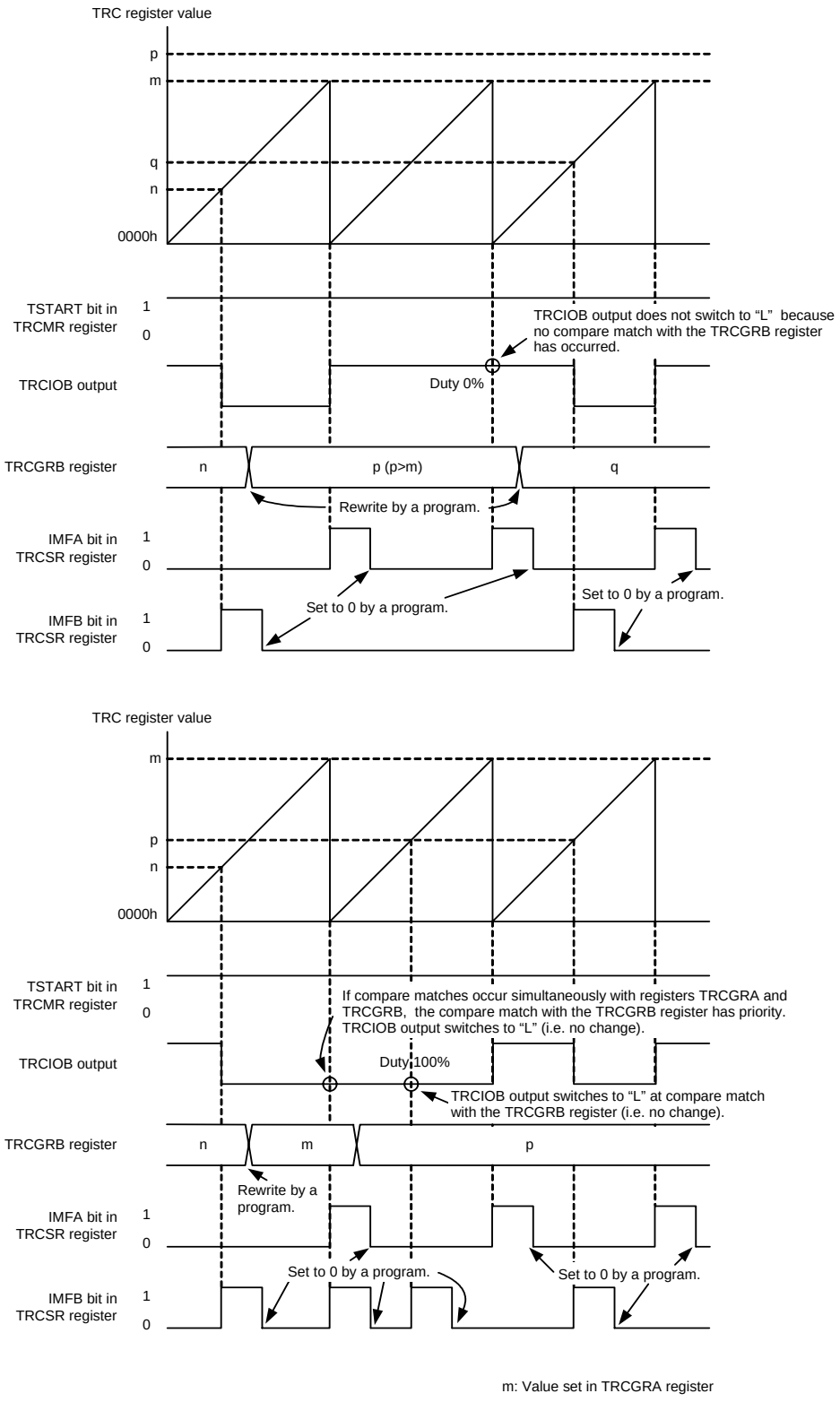
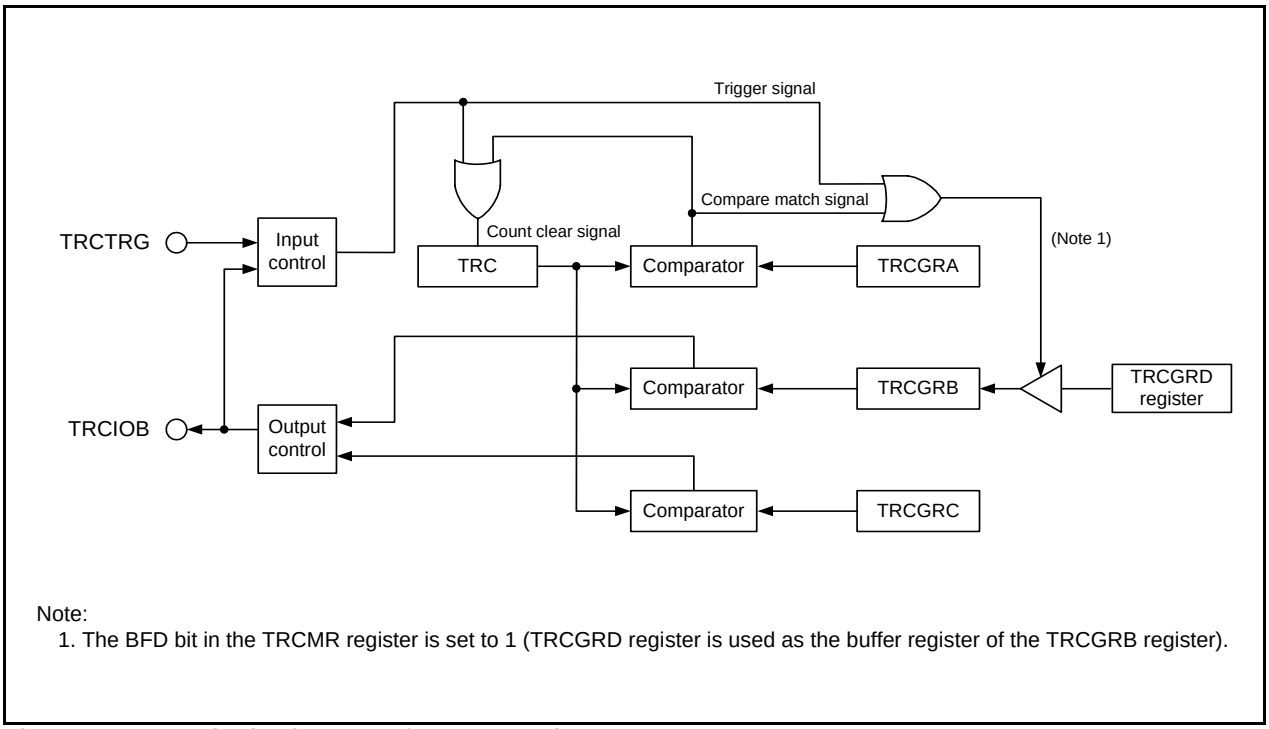


Figure 18.15 Operating Example in PWM Mode (Duty 0% and Duty 100%)

18.7 PWM2 Mode

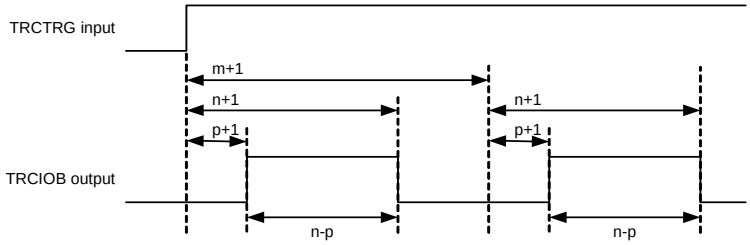
This mode outputs a single PWM waveform. After a given wait time has elapsed following the trigger, the pin output switches to active level. Then, after a given duration, the output switches back to inactive level. Furthermore, the counter stops at the same time the output returns to inactive level, making it possible to use PWM2 mode to output a programmable wait one-shot waveform.
Since timer RC uses multiple general registers in PWM2 mode, other modes cannot be used in conjunction with it. Figure 18.16 shows a Block Diagram of PWM2 Mode, Table 18.13 lists the PWM2 Mode Specifications, Table 18.14 lists the Functions of TRCGRj Register in PWM2 Mode, and Figures 18.17 to 18.19 show Operating Examples in PWM2 Mode.



Note:
1. The BFD bit in the TRCMR register is set to 1 (TRCGRD register is used as the buffer register of the TRCGRB register).

Figure 18.16 Block Diagram of PWM2 Mode

Table 18.13 PWM2 Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO20M, fOCO-F, or external signal input to TRCCLK pin (rising edge)
Count operation	TRC register increment
PWM waveform	PWM period: 1/fk × (m + 1) (no TRCTRG input) Active level width: 1/fk × (n - p) Wait time from count start or trigger: 1/fk × (p + 1) fk: Frequency of count source m: Value set in TRCGRA register n: Value set in TRCGRB register p: Value set in TRCGRC register  (TRCTRG: Rising edge, active level is high)
Count start conditions	• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger disabled) or the CSEL bit in the TRCCR2 register is set to 0 (count continues). 1 (count starts) is written to the TSTART bit in the TRCMR register. • Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger enabled) and the TSTART bit in the TRCMR register is set to 1 (count starts). A trigger is input to the TRCTRG pin.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRCMR register while the CSEL bit in the TRCCR2 register is set to 0 or 1. The TRCIOB pin outputs the initial level in accordance with the value of the TOB bit in the TRCCR1 register. The TRC register retains the value before the count stops. • The count stops at a compare match with TRCGRA while the CSEL bit in the TRCCR2 register is set to 1 The TRCIOB pin outputs the initial level. The TRC register retains the value before the count stops when the CCLR bit in the TRCCR1 register is set to 0. The TRC register is set to 0000h when the CCLR bit in the TRCCR1 register is set to 1.
Interrupt request generation timing	• Compare match (the contents of the TRC register and the TRCGRj register match.) • TRC register overflow
TRCIOA/TRCTRG pins function	Programmable I/O port or TRCTRG input
TRCIOB pin function	PWM output
TRCIOC/TRCIOD pins function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• External trigger and active edge selection The edge or edges of the signal input to the TRCTRG pin can be used as the PWM output trigger: rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **18.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **18.3.4 Forced Cutoff of Pulse Output**.) • Digital filter (Refer to **18.3.3 Digital Filter**.) • A/D trigger generation

j = A, B, C, or D

18.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM2 mode.	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Active level is high (Initial output at low High-level output at compare match with the TRCGRC register Low-level output at compare match with the TRCGRB register) 1: Active level is low (Initial output at high Low-level output at compare match with the TRCGRC register High-level output at compare match with the TRCGRB register)	R/W
b2	TOC	TRCIOC output level select bit (1)	Disabled in PWM2 mode.	R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4	R/W
b5	TCK1		0 0 0: f1	R/W
b6	TCK2		0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO20M 1 1 1: fOCO-F (3)	R/W
b7	CCLR	TRC counter clear select bit	0: Clear disabled (free-running operation) 1: Clear by compare match with the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.6 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

18.7.2 Timer RC Control Register 2 (TRCCR2) in PWM2 Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as low active 1: TRCIOB output level selected as high active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as low active 1: TRCIOC output level selected as high active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as low active 1: TRCIOD output level selected as high active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Trigger input from the TRCTRG pin disabled 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

18.7.3 Timer RC Digital Filter Function Select Register (TRCDF) in PWM2 Mode

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)	0: Function is not used 1: Function is used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Digital filter function clock select bit (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK0 to TCK2 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

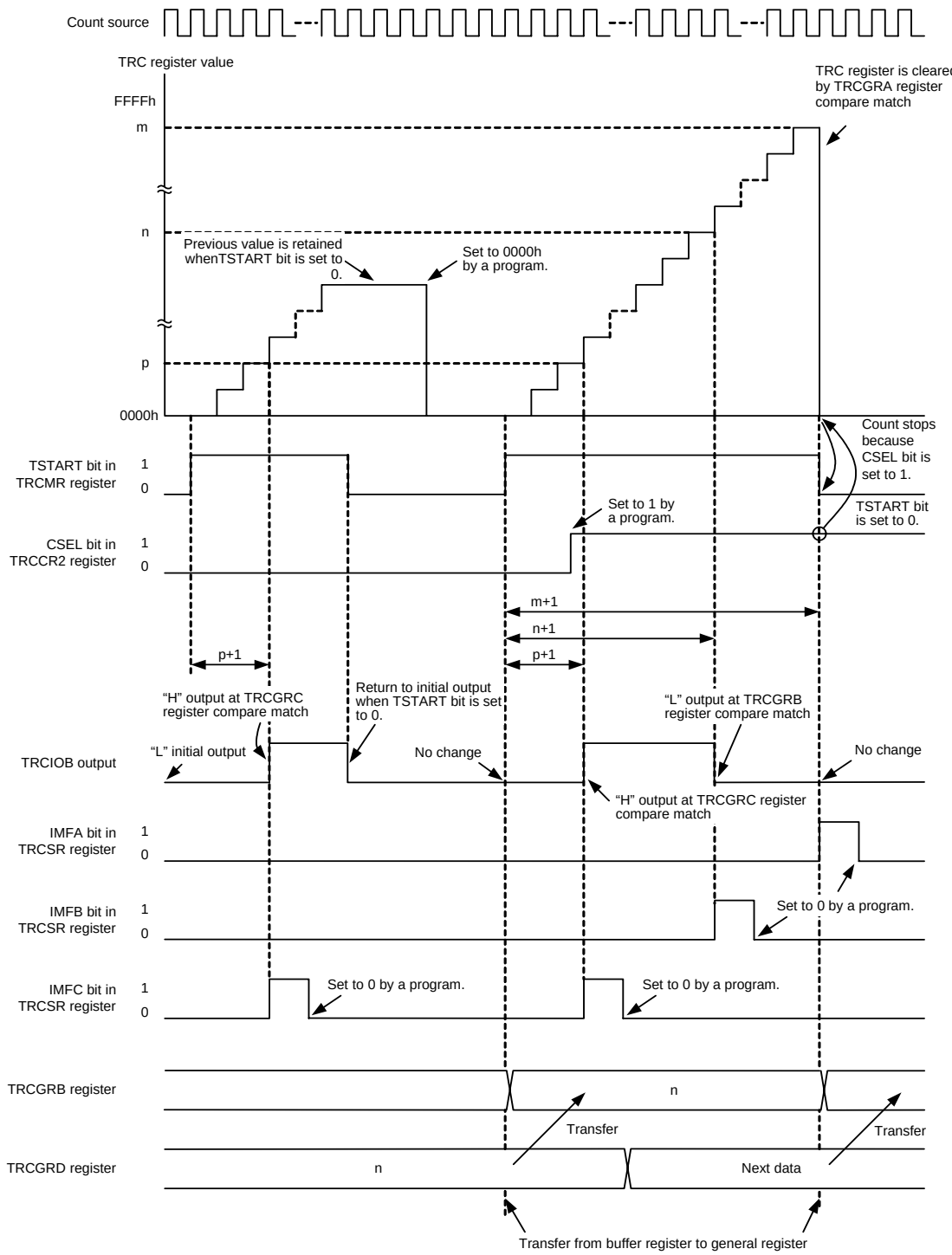
Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

Table 18.14 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	–	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	–	General register. Set the PWM output change point.	
TRCGRC (1)	BFC = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BFD = 0	(Not used in PWM2 mode.)	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **18.3.2 Buffer Operation**.)	TRCIOB pin

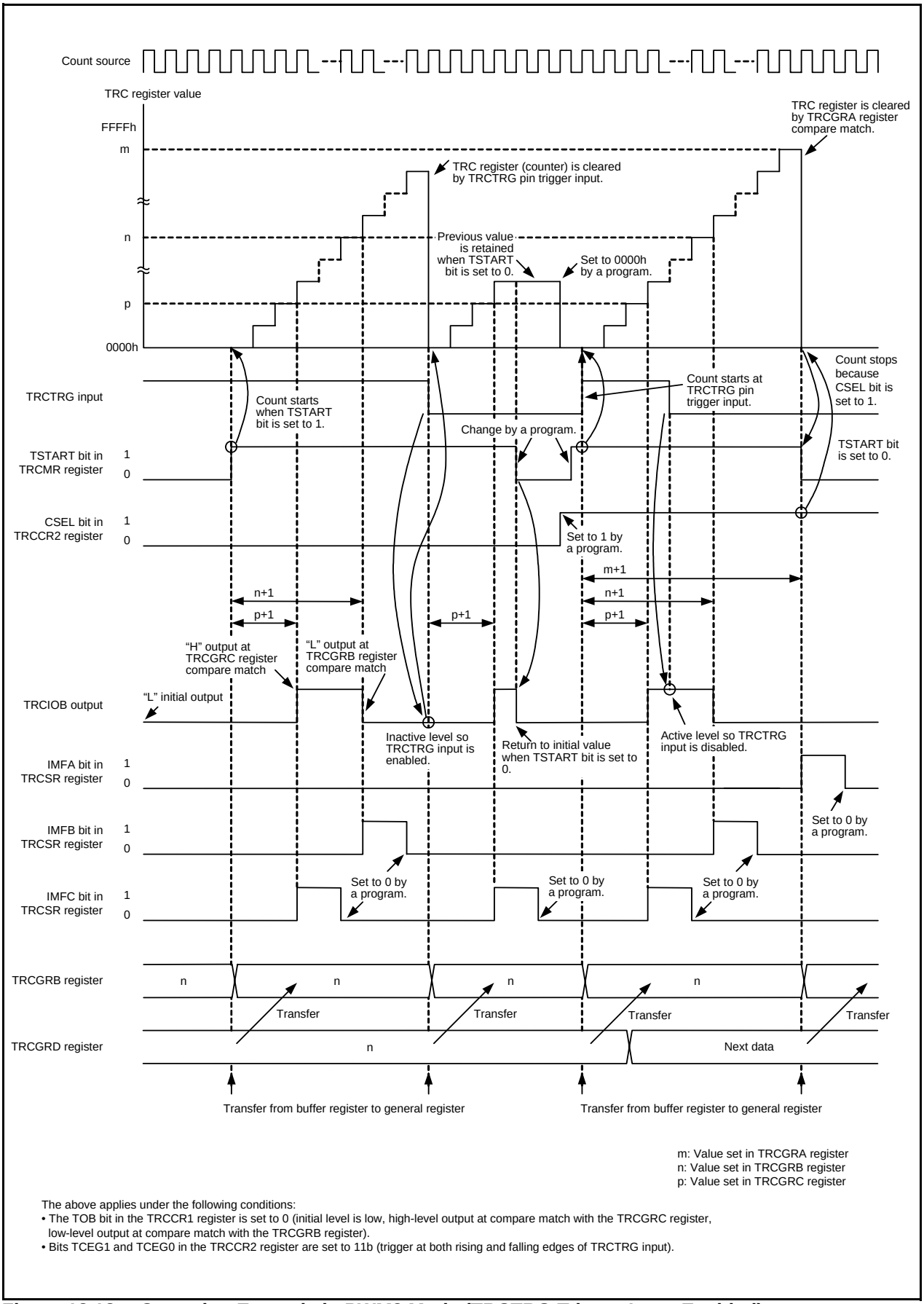
j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. Do not set registers TRCGRB and TRCGRC to the same value.

18.7.4 Operating Example


Count source
TRC register value
FFFFh
m
n
p
0000h
TRC register is cleared by TRCGRA register compare match
Previous value is retained whenTSTART bit is set to 0.
Set to 0000h by a program.
Count stops because CSEL bit is set to 1.
TSTART bit is set to 0.
TSTART bit in TRCMR register
CSEL bit in TRCCR2 register
Set to 1 by a program.
m+1
n+1
p+1
p+1
"H" output at TRCGRC register compare match
Return to initial output when TSTART bit is set to 0.
"L" output at TRCGRB register compare match
TRCIOB output
"L" initial output
No change
No change
"H" output at TRCGRC register compare match
IMFA bit in TRCSR register
IMFB bit in TRCSR register
Set to 0 by a program.
IMFC bit in TRCSR register
Set to 0 by a program.
Set to 0 by a program.
TRCGRB register
n
Transfer
Transfer
TRCGRD register
n
Next data
Transfer from buffer register to general register
m: Value set in TRCGRA register
n: Value set in TRCGRB register
p: Value set in TRCGRC register

The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is low, high-level output at compare match with the TRCGRC register, low-level output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 18.17 Operating Example in PWM2 Mode (TRCTRG Trigger Input Disabled)


Count source
TRC register value
FFFFh
m
n
p
0000h
TRC register is cleared by TRCGRA register compare match.
TRC register (counter) is cleared by TRCTRG pin trigger input.
Previous value is retained when TSTART bit is set to 0.
Set to 0000h by a program.
TRCTRG input
Count starts when TSTART bit is set to 1.
Count starts at TRCTRG pin trigger input.
Count stops because CSEL bit is set to 1.
Change by a program.
TSTART bit in TRCMR register
TSTART bit is set to 0.
CSEL bit in TRCCR2 register
Set to 1 by a program.
n+1
p+1
m+1
"H" output at TRCGRC register compare match
"L" output at TRCGRB register compare match
"L" initial output
TRCIOB output
Inactive level so TRCTRG input is enabled.
Return to initial value when TSTART bit is set to 0.
Active level so TRCTRG input is disabled.
IMFA bit in TRCSR register
IMFB bit in TRCSR register
IMFC bit in TRCSR register
Set to 0 by a program.
TRCGRB register
TRCGRD register
Transfer
Next data
Transfer from buffer register to general register
Transfer from buffer register to general register
m: Value set in TRCGRA register
n: Value set in TRCGRB register
p: Value set in TRCGRC register

The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is low, high-level output at compare match with the TRCGRC register, low-level output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 11b (trigger at both rising and falling edges of TRCTRG input).

Figure 18.18 Operating Example in PWM2 Mode (TRCTRG Trigger Input Enabled)

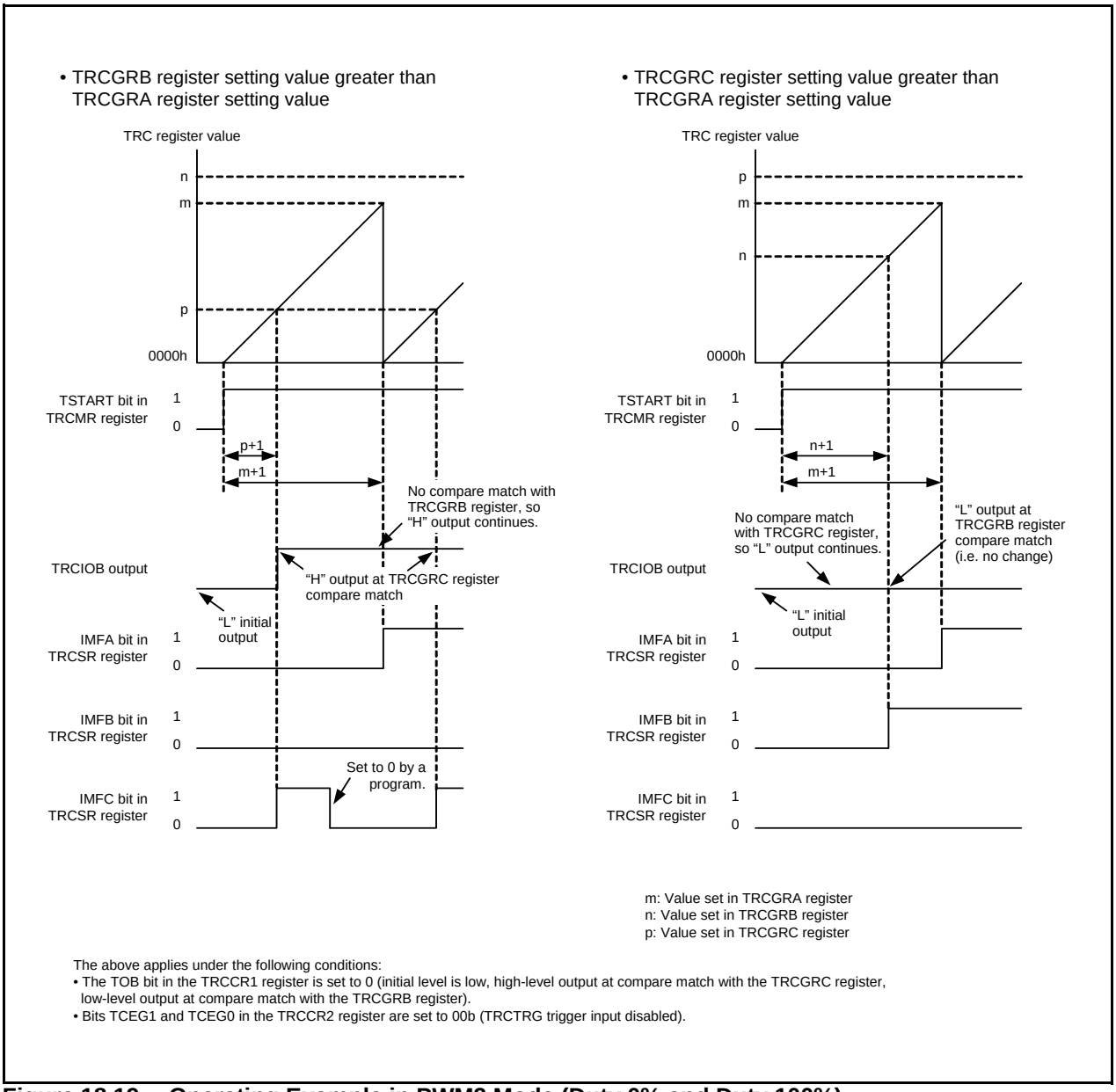

• TRCGRB register setting value greater than TRCGRA register setting value
TRC register value
n
m
p
0000h
TSTART bit in TRCMR register
1
0
p+1
m+1
No compare match with TRCGRB register, so "H" output continues.
TRCIOB output
"H" output at TRCGRC register compare match
"L" initial output
IMFA bit in TRCSR register
IMFB bit in TRCSR register
Set to 0 by a program.
IMFC bit in TRCSR register
• TRCGRC register setting value greater than TRCGRA register setting value
TRC register value
p
m
n
0000h
TSTART bit in TRCMR register
n+1
m+1
No compare match with TRCGRC register, so "L" output continues.
"L" output at TRCGRB register compare match (i.e. no change)
TRCIOB output
"L" initial output
IMFA bit in TRCSR register
IMFB bit in TRCSR register
IMFC bit in TRCSR register
m: Value set in TRCGRA register
n: Value set in TRCGRB register
p: Value set in TRCGRC register
The above applies under the following conditions:
• The TOB bit in the TRCCR1 register is set to 0 (initial level is low, high-level output at compare match with the TRCGRC register, low-level output at compare match with the TRCGRB register).
• Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 18.19 Operating Example in PWM2 Mode (Duty 0% and Duty 100%)

18.8 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 18.15 lists the Registers Associated with Timer RC Interrupt and Figure 18.20 shows a Block Diagram of Timer RC Interrupt.

Table 18.15 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR	TRCIER	TRCIC

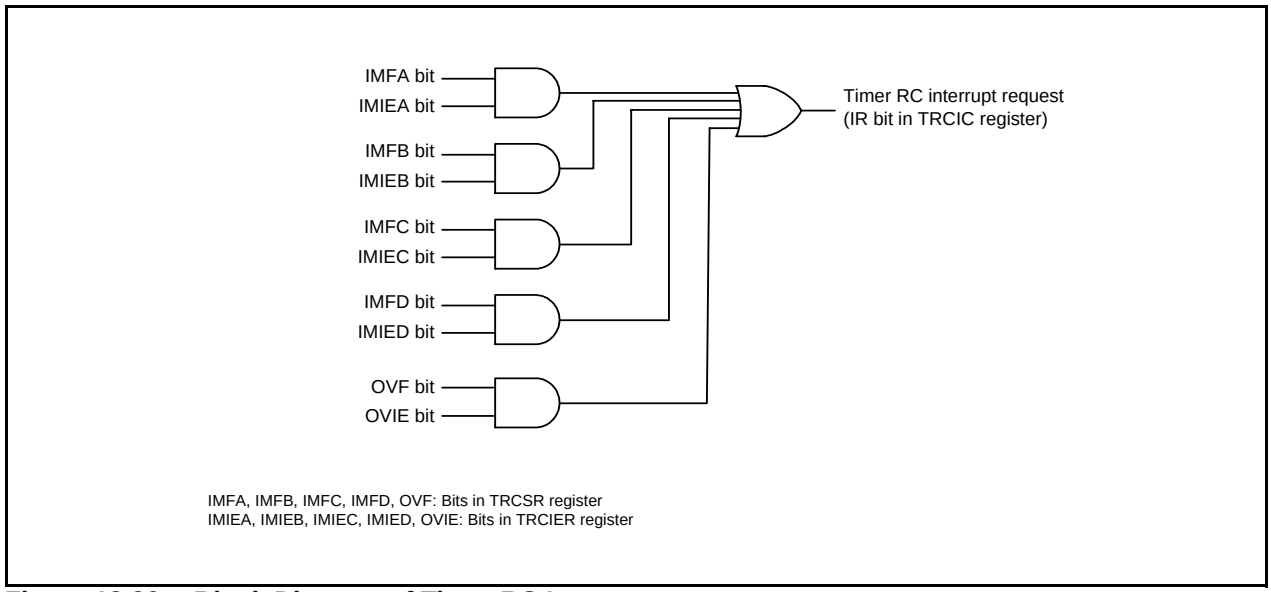


Figure 18.20 Block Diagram of Timer RC Interrupt

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **18.2.5 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **18.2.4 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **12.3 Interrupt Control**, for details of the TRCIC register and **12.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

18.9 Notes on Timer RC

18.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRC register cleared by compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC     ;Write
                    JMP.B   L1              ;JMP.B instruction
                L1: MOV.W   TRC,DATA        ;Read
```

18.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR     ;Write
                    JMP.B   L1              ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA      ;Read
```

18.9.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

18.9.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO20M to another clock, allow two or more cycles of f1 to elapse after changing the clock setting before stopping fOCO20M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for two or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO20M, allow a minimum of one cycle of fOCO-F + fOCO20M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO20M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

18.9.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 18.1 Timer RC Operating Clocks**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 18.5 Block Diagram of Digital Filter**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

18.9.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

19. Timer RH

19.1 Introduction

Timer RH has a 3-bit counter, 4-bit counter, and 8-bit counter.
Timer RH supports the following two modes:

- Real-time clock mode
  A one-second signal is generated from fC-TRH and seconds, minutes, hours, a day of the week, a date, a month, and a year (supporting leap years from 2000 to 2099) are counted.
- Output compare mode
  A count source is counted and compare matches are detected.

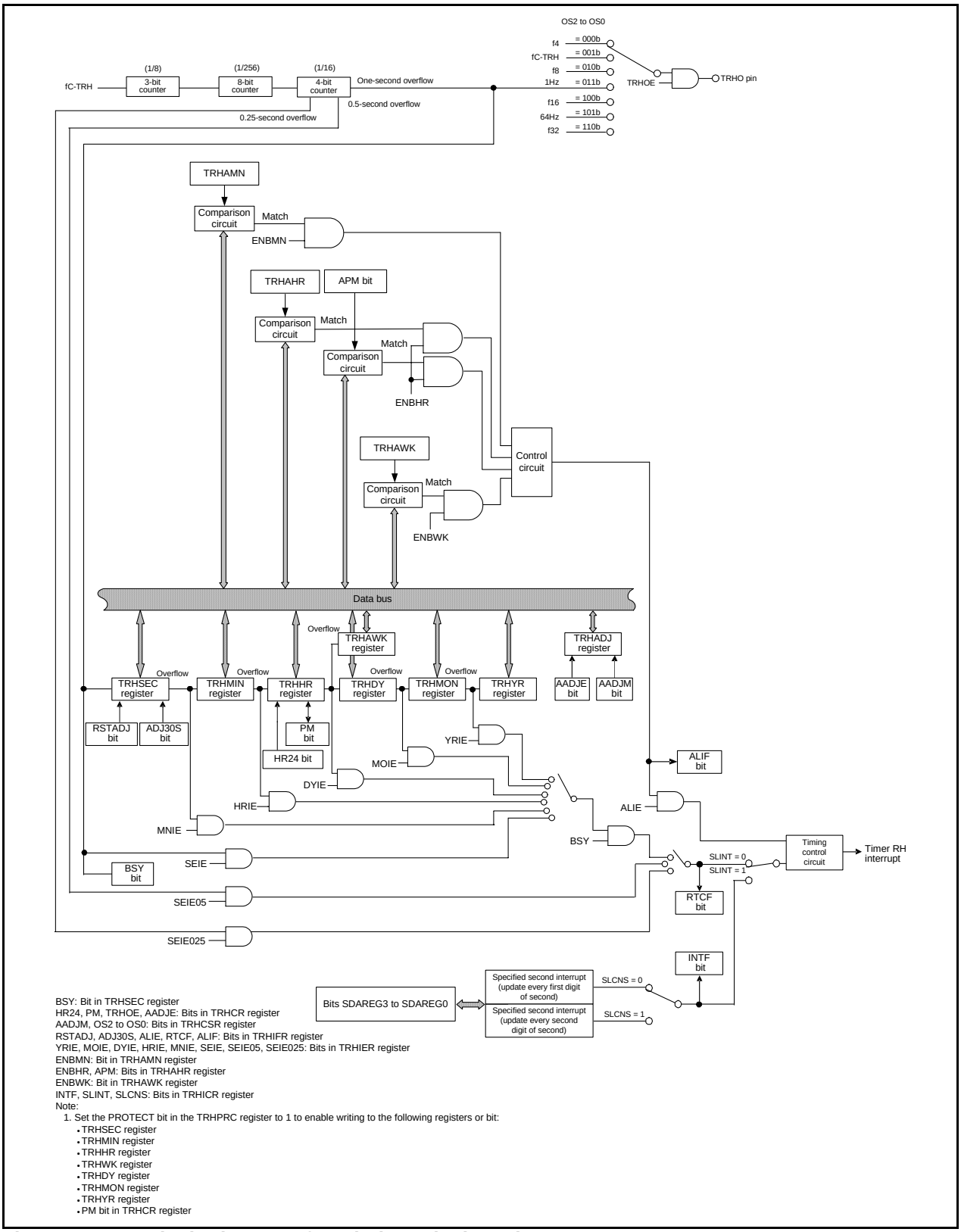
The count source for timer RH is the operating clock that regulates the timing of timer operations.
Table 19.1 lists the Timer RH Pin Configuration.

Table 19.1 Timer RH Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRHO	P0_7	Output	Function differs according to the mode. Refer to descriptions of individual modes for details.

19.2 Real-Time Clock Mode

In real-time clock mode, a one-second signal is generated from fC-TRH using a 3-bit counter, 4-bit counter, or 8-bit counter, and used to count seconds, minutes, hours, a day of the week, a date, a month, and a year. Matches with specified minutes, hours, a day of the week are also detected. Figure 19.1 shows a Block Diagram of Real-Time Clock Mode and Table 19.2 lists the Real-Time Clock Mode Specifications.



BSY: Bit in TRHSEC register
HR24, PM, TRHOE, AADJE: Bits in TRHCR register
AADJM, OS2 to OS0: Bits in TRHCSR register
RSTADJ, ADJ30S, ALIE, RTCF, ALIF: Bits in TRHIFR register
YRIE, MOIE, DYIE, HRIE, MNIE, SEIE, SEIE05, SEIE025: Bits in TRHIER register
ENBMN: Bit in TRHAMN register
ENBHR, APM: Bits in TRHAHR register
ENBWK: Bit in TRHAWK register
INTF, SLINT, SLCNS: Bits in TRHICR register
Note:
1. Set the PROTECT bit in the TRHPRC register to 1 to enable writing to the following registers or bit:
- TRHSEC register
- TRHMIN register
- TRHHR register
- TRHWK register
- TRHDY register
- TRHMON register
- TRHYR register
- PM bit in TRHCR register

Figure 19.1 Block Diagram of Real-Time Clock Mode

Table 19.2 Real-Time Clock Mode Specifications

Item	Specification
Count source	fC-TRH (32.768 kHz)
Count operation	Increment
Count start condition	1 (count starts) is written to the RUN bit in the TRHCR register.
Count stop condition	0 (count stops) is written to the RUN bit in the TRHCR register.
Interrupt request generation timing	Periodic interrupt Select one of the following: • 0.25-second period • 0.5-second period • Update of second data • Update of minute data • Update of hour data • Update of day data • Update of month data • Update of year data Alarm interrupt When time data and alarm data match Update of the specified second set by the TRHICR register
TRHO pin function	Programmable I/O port or output of f4, f8, f16, f32, 1 Hz, 64 Hz, or fC-TRH
Read from timer	When reading timer RH data registers (1), the count values can be read. The values read from the timer RH data registers (1) except TRHWK are represented by the BCD code.
Write to timer	When the PROTECT bit in the TRHPRC register is set to 1 (write enabled) and the RUN bit in the TRHCR register is set to 0 (count stops), the value can be written to timer RH data registers (1) and the PM bit in the TRHCR register. The values written to the timer RH data registers (1) except TRHWK are represented by the BCD code.
Selectable functions	• 12-hour mode/24-hour mode switch function • Alarm function Either of following is detected: - Minutes, hours, or the day of the week - Any combination of these • Second adjustment function • Time error correction function Automatic correction function or correction by software • Clock output

Note:
1. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR registers

19.2.1 Module Standby Control Register 1 (MSTCR1)

Address 0010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRJ2	MSTTRJ1	MSTTRJ0	MSTTRH	MSTTRB1	MSTTRB0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRB0	Timer RB0 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB1	Timer RB1 standby bit	0: Active 1: Standby (2)	R/W
b2	MSTTRH	Timer RH standby bit	0: Active 1: Standby (3)	R/W
b3	MSTTRJ0	Timer RJ0 standby bit	0: Active 1: Standby (4)	R/W
b4	MSTTRJ1	Timer RJ1 standby bit	0: Active 1: Standby (5)	R/W
b5	MSTTRJ2	Timer RJ2 standby bit	0: Active 1: Standby (6)	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. When the MSTTRB0 bit is set to 1 (standby), any access to the timer RB0 associated registers (addresses 0108h to 010Eh) is disabled.
2. When the MSTTRB1 bit is set to 1 (standby), any access to the timer RB1 associated registers (addresses 0098h to 009Eh) is disabled.
3. When the MSTTRH bit is set to 1 (standby), any access to the timer RH associated registers (addresses 0110h to 011Fh) is disabled.
4. When the MSTTRJ0 bit is set to 1 (standby), any access to the timer RJ0 associated registers (addresses 0080h to 0086h) is disabled.
5. When the MSTTRJ1 bit is set to 1 (standby), any access to the timer RJ1 associated registers (addresses 0088h to 008Eh) is disabled.
6. When the MSTTRJ2 bit is set to 1 (standby), any access to the timer RJ2 associated registers (addresses 0090h to 0096h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

19.2.2 Timer RH Second Data Register (TRHSEC) in Real-Time Clock Mode

Address 0110h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	SC00	First digit of second count bit	Count 0 to 9 every second. When the digit increments, 1 is added to the second digit of second.	0 to 9 (BCD code)	R/W
b1	SC01				R/W
b2	SC02				R/W
b3	SC03				R/W
b4	SC10	Second digit of second count bit	When counting 0 to 5, 60 seconds are counted.	0 to 5 (BCD code)	R/W
b5	SC11				R/W
b6	SC12				R/W
b7	BSY	Timer RH busy flag	This bit is set to 1 while timer RH data registers (1) or the PM in the TRHCR register is updated.		R

Note:
1. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR

Set the PROTECT bit in the TRHPRC register to 1 (write enabled) before rewriting this register.

Bits SC03 to SC00 (First Digit of Second Count Bit)
Bits SC12 to SC10 (Second Digit of Second Count Bit)

Set values between 00 to 59 by the BCD code.
Write to these bits when the RUN bit in the TRHCR register is set to 0 (count stops).
Read these bits when the BSY bit is set to 0 (not while data is updated).

BSY Bit (Timer RH Busy Flag)

This bit is set to 1 while data is updated. Read the following registers or bit when this bit set to is 0 (not while data is updated).
- Timer RH data registers (1)
- The PM bit in the TRHCR register

Write to the following registers or bits when the BSY bit is set to 0 (not while data is not updated).
- Timer RH data registers (1)
- Timer RH alarm registers (2)
- Bits PM and HR24 in the TRHCR register
- Registers and bits associated with correction (3)

Notes:
1. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR
2. Timer RH alarm registers: TRHAMN, TRHAHR, and TRHAWK
3. Registers and bits associated with correction: TRHADJ, AADJM in TRHCSR, and AADJE in TRHCR

19.2.3 Timer RH Minute Data Register (TRHMIN) in Real-Time Clock Mode

Address 0111h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MN7	MN12	MN11	MN10	MN03	MN02	MN01	MN00
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	MN00	First digit of minute count bit	Count 0 to 9 every minute. When the digit increments, 1 is added to the second digit of minute.	0 to 9 (BCD code)	R/W
b1	MN01				R/W
b2	MN02				R/W
b3	MN03				R/W
b4	MN10	Second digit of minute count bit	When counting 0 to 5, 60 minutes are counted.	0 to 5 (BCD code)	R/W
b5	MN11				R/W
b6	MN12				R/W
b7	MN7	Set to 0 in real-time clock mode.			R/W

Set the PROTECT bit in the TRHPRC register to 1 (write enabled) before rewriting this register.

Bits MN03 to MN00 (First Digit of Minute Count Bit)
Bits MN12 to MN10 (Second Digit of Minute Count Bit)

Set values between 00 to 59 by the BCD code.
When the digit increments from the TRHSEC register, 1 is added.
Write to these bits when the RUN bit in the TRHCR register is set to 0 (count stops).
Read these bits when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

19.2.4 Timer RH Hour Data Register (TRHHR) in Real-Time Clock Mode

Address 0112h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	HR11	HR10	HR03	HR02	HR01	HR00
After Reset	0	0	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	HR00	First digit of hour count bit	Count 0 to 9 every hour. When the digit increments, 1 is added to the second digit of hour.	0 to 9 (BCD code)	R/W
b1	HR01				R/W
b2	HR02				R/W
b3	HR03				R/W
b4	HR10	Second digit of hour count bit	Count 0 to 1 when the HR24 bit in the TRHCR register is set to 0 (12-hour mode). Count 0 to 2 when the HR24 bit is set to 1 (24-hour mode).	0 to 2 (BCD code)	R/W
b5	HR11				R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
b7	—				

Set the PROTECT bit in the TRHPRC register to 1 (write enabled) before rewriting this register.

Bits HR03 to HR00 (First Digit of Hour Count Bit)
Bits HR11 to HR10 (Second Digit of Hour Count Bit)

Set values between 00 to 11 by the BCD code when the HR24 bit in the TRHCR register is set to 0 (12-hour mode). Set values between 00 to 23 by the BCD code when the HR24 bit is set to 1 (24-hour mode).
When the digit increments from the TRHMIN register, 1 is added.
Write to these bits when the RUN bit in the TRHCR register is set to 0 (count stops).
Read these bits when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

19.2.5 Timer RH Day-of-the-Week Data Register (TRHWK) in Real-Time Clock Mode

Address 0113h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	WK2	WK1	WK0
After Reset	0	0	0	0	0	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WK0	Day-of-the-week count bit	b2 b1 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Do not set.	R/W
b1	WK1			R/W
b2	WK2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Set the PROTECT bit in the TRHPRC register to 1 (write enabled) before rewriting this register.

Bits WK2 to WK0 (Day-of-Week Count Bit)

A week is counted by counting from 000b (Sunday) to 110b (Saturday) repeatedly. Do not set to 111b.
When the digit increments from the TRHHR register, 1 is added.
Write to these bits when the RUN bit in the TRHCR register is 0 (count stops).
Read these bits when the BSY bit in the TRHSEC register is 0 (not while data is updated).

19.2.6 Timer RH Date Data Register (TRHDY) in Real-Time Clock Mode

Address 0114h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	DY11	DY10	DY03	DY02	DY01	DY00
After Reset	0	0	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	DY00	First digit of date count bit	Count 0 to 9 every day. When the digit increments, 1 is added to the second digit of date.	0 to 9 (BCD code)	R/W
b1	DY01				R/W
b2	DY02				R/W
b3	DY03				R/W
b4	DY10	Second digit of date count bit	Count 0 to 3.	0 to 3 (BCD code)	R/W
b5	DY11				R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
b7	—				

Set the PROTECT bit in the TRHPRC register to 1 (write enabled) before rewriting this register.

Bits DY03 to DY00 (First Digit of Date Count Bit)
Bits DY11 to DY10 (Second Digit of Date Count Bit)

Set values between 01 and 31 by the BCD code.
When the digit increments from the TRHHR register, 1 is added.
The number of days (28 to 31) in each month including February in a leap year are counted from 2000 to 2099.
Write to these bits when the RUN bit in the TRHCTR register is set to 0 (count stops).
Read these bits when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

19.2.7 Timer RH Month Data Register (TRHMON) in Real-Time Clock Mode

Address 0115h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MO10	MO03	MO02	MO01	MO00
After Reset	0	0	0	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	MO00	First digit of month count bit	Count 0 to 9 every hour. When the digit increments, 1 is added to the second digit of month.	0 to 9 (BCD code)	R/W
b1	MO01				R/W
b2	MO02				R/W
b3	MO03				R/W
b4	MO10	Second digit of month count bit	Count 0 to 1.	0 to 1 (BCD code)	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
b6	—				
b7	—				

Set the PROTECT bit in the TRHPRC register to 1 (write enabled) before rewriting this register.

Bits MO03 to MO00 (First Digit of Month Count Bit)
MO10 Bit (Second Digit of Month Count Bit)

Set values between 01 and 12 by the BCD code.
When the digit increments from the TRHDY register, 1 is added.
Write to these bits when the RUN bit in the TRHCR register is set to 0 (count stops).
Read these bits when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

19.2.8 Timer RH Year Data Register (TRHYR) in Real-Time Clock Mode

Address 0116h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	YR13	YR12	YR11	YR10	YR03	YR02	YR01	YR00
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	YR00	First digit of year count bit	Count 0 to 9 every hour. When the digit increments, 1 is added to the second digit of year.	0 to 9 (BCD code)	R/W
b1	YR01				R/W
b2	YR02				R/W
b3	YR03				R/W
b4	YR10	Second digit of year count bit	Count 0 to 9.	0 to 9 (BCD code)	R/W
b5	YR11				R/W
b6	YR12				R/W
b7	YR13				R/W

Set the PROTECT bit in the TRHPRC register to 1 (write enabled) before rewriting this register.

Bits YR03 to YR00 (First Digit of Year Count Bit)
Bits YR13 to YR10 (Second Digit of Year Count Bit)

Set values between 00 and 99 by the BCD code. Fourth digit and third digit of the year are fixed to 20.
When the digit increments from the TRHMON register, 1 is added.
Write to these bits when the RUN bit in the TRHCR register is set to 0 (count stops).
Read these bits when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

19.2.9 Timer RH Control Register (TRHCR) in Real-Time Clock Mode

Address 0117h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RUN	HR24	PM	RTCRST	CCLR	LFLAG	TRHOE	AADJE
After Reset	X	X	X	0	0	X	0	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	X	X	1	X	0

Bit	Symbol	Bit Name	Function	R/W
b0	AADJE	Timer RH automatic correction function enable bit	0: Automatic correction function disabled (correction function by software enabled) 1: Automatic correction function enabled (correction function by software disabled)	R/W
b1	TRHOE	Timer RH output enable bit	0: TRHO output disabled 1: TRHO output enabled	R/W
b2	LFLAG	Leap year flag(1)	0: Common year 1: Leap year	R
b3	CCLR	Set to 0 in real-time clock mode.		R/W
b4	RTCRST	Timer RH reset bit (2)	When this bit is set to 1, the target registers and bits are initialized to the reset values and the timer RH control circuit is initialized.	R/W
b5	PM	a.m./p.m. bit	0: a.m. 1: p.m.	R/W
b6	HR24	Operating mode select bit	0: 12-hour mode 1: 24-hour mode	R/W
b7	RUN	Timer RH operation start bit	0: Count stops 1: Count starts	R/W

Notes:
1. When the RTCRST bit is set to 1, the TRHYR register is reset to 00h.
   As year 2000 is a leap year, the initial value of the LFLAG bit is 1.
2. Set the RTCRST bit to 0 after setting it to 1.

AADJE Bit

Rewrite this bit when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

TRHOE Bit (Timer RH Output Enable Bit)

Rewrite this bit when the RUN bit is set to 0 (count stops).

LFLAG Bit (Leap Year Flag)

This bit is set to 1 (leap year) when the values of the TRHYR register are 00 or the multiples of four. When this bit is set to 1, the number of days in February becomes 29.

RTCRST Bit (Timer RH Reset Bit)

When the RTCRST bit set to 1, the registers and bits listed in Table 19.3 are initialized to the reset values and the timer RH control circuit is initialized. Always set the RTCRST bit to 0 after setting it to 1.

Table 19.3 Registers and Bits (1) Initialized by RTCRST Bit

Register	Bit to be Initialized	Bit to Retain Setting Value
Timer RH data register (2)	Bit 0 to bit 7	—
Timer RH alarm register (3)	Bit 0 to bit 7	—
TRHCR	AADJE, LFLAG, PM, HR24, RUN	TRHOE, CCLR, RTCRST
TRHCSR	Bit 7	Bit 0 to bit 6
TRHADJ	Bit 0 to bit 7	—
TRHIFR	Bit 0 to bit 2	Bit 3 to bit 7
TRHIER	Bit 0 to bit 7	—
TRHPRC	Bit 0 to bit 7	—
TRHICR	Bit 0 to bit 7	—

Notes:
1. For the reset values, refer to each register's values reset by the RTCRST bit.
2. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR
3. Timer RH alarm registers: TRHAMN, TRHAHR, and TRHAWK

PM Bit (a.m./p.m. Bit)

Write to this bit when the RUN bit in the TRHCR register is 0 (count stops). Set the PROTECT bit in the TRHPRC register to 1 (write enabled) before rewriting this bit.
Read this bit when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).
This bit is enabled when the HR24 bit is set to 0 (12-hour mode).
This bit changes as follows while counting.

- Changes to 0 when this bit is 1 (p.m.) and the clock increments from 11:59:59 to 00:00:00.
- Changes to 1 when this bit is 0 (a.m.) and the clock increments from 11:59:59 to 00:00:00.

Figure 19.2 shows the Definition of Time Representation.

< When count starts from 0 a.m. of Saturday on January 1, 2000 >

Noon

HR24 bit = 1 (24-hour mode)	TRHHR register	0	1	···	10	11	12	13	···	22	23	0	1	2	···	21	22	23	0	1	2			
	PM bit	0																						
HR24 bit = 0 (12-hour mode)	TRHHR register	0	1	···	10	11	0	1	···	10	11	0	1	2	···	9	11	11	0	1	2			
	PM bit	0 (a.m.)					1 (p.m.)					0 (a.m.)			···	1 (p.m.)			0 (a.m.)					
TRHWK register		110 (Sat.)										000 (Sun.)			···	001 (Mon.)			010 (Tue.)					
TRHDY register		Day 1										Day 2			···	Day 31			Day 1					
TRHMON register		January																	February					
TRHYR register		Year 2000																						
LFLAG bit		1																						

HR24 bit = 1 (24-hour mode)	TRHHR register	3	4	5	···	21	22	23	0	1	2	···	21	22	23	0	1	2	···					
	PM bit	0																						
HR24 bit = 0 (12-hour mode)	TRHHR register	3	4	5	···	21	10	11	0	1	2	···	9	10	11	0	1	2	···					
	PM bit	0 (a.m.)			···	1 (p.m.)			0 (a.m.)			···	1 (p.m.)			0 (a.m.)			···					
TRHWK register		010 (Tue.)			···	010 (Tue.)			011 (Wed.)			···	000 (Sun.)			001 (Mon.)			···					
TRHDY register		Day 1			···	Day 29			Day 1			···	Day 31			Day 1			···					
TRHMON register		February							March			···	December			January			···					
TRHYR register		Year 2000														Year 2001			···					
LFLAG bit		1														0			···					

LFLAG, PM, HR24: Bits in TRHCR register

Figure 19.2 Definition of Time Representation

HR24 Bit (Operating Mode Select Bit)

When this bit is set to 0, the TRHHR register counts 0 to 11. When this bit is set to 1, the register counts 0 to 23. Write to this bit when the RUN bit is set to 0 (counter stops).

19.2.10 Timer RH Count Source Select Register (TRHCSR) in Real-Time Clock Mode

Address 0118h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	AADJM	OS2	OS1	OS0	CS3	CS2	CS1	CS0
After Reset	X	0	0	0	1	0	0	0
After Reset by RTCRST Bit in TRHCR Register	0	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	CS0	Count source select bit	Set to 1000b (fC-TRH) in real-time clock mode (CS3 bit = 1).	R/W
b1	CS1			R/W
b2	CS2			R/W
b3	CS3			R/W
b4	OS0	Timer RH output select bit	b6 b5 b4 0 0 0: f4 0 0 1: fC-TRH 0 1 0: f8 0 1 1: 1 Hz (1, 3) 1 0 0: f16 1 0 1: 64 Hz (2, 3) 1 1 0: f32 1 1 1: Do not set.	R/W
b5	OS1			R/W
b6	OS2			R/W
b7	AADJM	Automatic correction mode select bit	0: Correct every minute 1: Correct every 10 seconds	R/W

Notes:
1. When fC-TRH = 32.768 kHz
   When fC-TRH ≠ 32.768 kHz, the output frequency may vary from 1 Hz.
2. When fC-TRH = 32.768 kHz
   When fC-TRH ≠ 32.768 kHz, the output frequency may vary from 64 Hz.
3. When the second adjustment or clock error correction is used, the output frequency may vary depending on the timing.

Bits CS3 to CS0 (Count Source Select Bit)

Rewrite these bits when the RUN bit in the TRHCR register is set to 0 (count stops).

Bits OS2 to OS0 (Timer RH Output Select Bit)

Rewrite these bits when the RUN bit in the TRHCR register is set to 0 (count stops).
These bits are enabled when the TRHOE bit in the TRHCR register is set to 1 (TRHO output enabled).

AADJM Bit (Automatic Correction Mode Select Bit)

This bit is enabled when the AADJE bit in the TRHCR register is set to 1 (automatic correction function enabled).
Rewrite this bit when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

19.2.11 Timer RH Clock Error Correction Register (TRHADJ) in Real-Time Clock Mode

Address 0119h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PLUS	MINUS	ADJ5	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADJ0	Correction value set bit	Setting range: 00h to 3Fh (00 to 63)	R/W
b1	ADJ1			R/W
b2	ADJ2			R/W
b3	ADJ3			R/W
b4	ADJ4			R/W
b5	ADJ5			R/W
b6	MINUS	Correction counter bit	b7 b6 0 0: Not corrected 0 1: Corrected to the minus side 1 0: Corrected to the plus side 1 1: Do not set.	R/W
b7	PLUS			R/W

Rewrite this register when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

Bits MINUS and PLUS (Correction Counter Bit)

The one-second counter is changed depending on the values of bits ADJ0 to ADJ5.
When the PLUS bit is set to 0 and the MINUS bit is set to 1, the internal counter is corrected to the minus side. The clock can be set back when it gains time.
When the PLUS bit is set to 1 and the MINUS bit is set to 0, the internal counter is corrected to the plus side. The clock can be set ahead when it loses time.

19.2.12 Timer RH Interrupt Flag Register (TRHIFR) in Real-Time Clock Mode

Address 011Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	RSTADJ	ADJ30S	ALIE	RTCF	ALIF
After Reset	0	0	0	0	0	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ALIF	Alarm interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	RTCF	RTC periodic interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b2	ALIE	Alarm interrupt enable bit	0: Alarm interrupt disabled 1: Alarm interrupt enabled	R/W
b3	ADJ30S	30 seconds adjust bit	When 1 is written to this bit, the values of the TRHSEC register are as follows: When the TRHSEC register values ≤ 29: TRHSEC ← 00 When the TRHSEC register values ≥ 30: TRHSEC ← 00, TRHSEC ← TRHMIN + 1 When read, the content is 0.	W
b4	RSTADJ	Second counter reset adjust bit	When setting this bit is set to 1, the values of the TRHSEC register are set to 00, and the internal counter is initialized. When read, the content is 0.	W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

ALIF Bit (Alarm Interrupt Flag)

[Condition for setting to 0]
Write 0 after reading this bit. When writing 0 to this bit if the read value is 1, this bit is set to 0.
[Condition for setting to 1]
The contents of timer RH alarm registers (1) match the contents of timer RH data registers (2) (refer to **19.2.20 Alarm Function**).
When writing 0 to this bit if the read value is 0, this bit remains unchanged (if this bit changes from 0 to 1 after reading this bit, this bit remains 1 even if writing 0). Writing 1 has no effect.
To confirm the match, set an ENB bit in the timer RH alarm registers (1) to 1.

Notes:
1. Timer RH alarm registers: TRHAMN, TRHAHR, and TRHAWK
2. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR

RTCF Bit (RTC Periodic Interrupt Flag)

[Condition for setting to 0]
Write 0 after reading this bit. When writing 0 to this bit if the read value is 1, this bit is set to 0.
[Condition for setting to 1]
An interrupt source enabled in the TRHIER register is generated.
When writing 0 to this bit if the read value is 0, this bit remains unchanged (if this bit changes from 0 to 1 after reading this bit, this bit remains 1 even if writing 0). Writing 1 has no effect.

19.2.13 Timer RH Interrupt Enable Register (TRHIER) in Real-Time Clock Mode

Address 011Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	YRIE	MOIE	DYIE	HRIE	MNIE	SEIE	SEIE05	SEIE025
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SEIE025	Periodic interrupt triggered every 0.25 seconds enable bit	0: Periodic interrupt triggered every 0.25 seconds disabled 1: Periodic interrupt triggered every 0.25 seconds enabled	R/W
b1	SEIE05	Periodic interrupt triggered every 0.5 seconds enable bit	0: Periodic interrupt triggered every 0.5 seconds disabled 1: Periodic interrupt triggered every 0.5 seconds enabled	R/W
b2	SEIE	Periodic interrupt triggered every second enable bit	0: Periodic interrupt triggered every second disabled 1: Periodic interrupt triggered every second enabled	R/W
b3	MNIE	Periodic interrupt triggered every minute enable bit	0: Periodic interrupt triggered every minute disabled 1: Periodic interrupt triggered every minute enabled	R/W
b4	HRIE	Periodic interrupt triggered every hour enable bit	0: Periodic interrupt triggered every hour disabled 1: Periodic interrupt triggered every hour enabled	R/W
b5	DYIE	Periodic interrupt triggered every day enable bit	0: Periodic interrupt triggered every day disabled 1: Periodic interrupt triggered every day enabled	R/W
b6	MOIE	Periodic interrupt triggered every month enable bit	0: Periodic interrupt triggered every month disabled 1: Periodic interrupt triggered every month enabled	R/W
b7	YRIE	Periodic interrupt triggered every year enable bit	0: Periodic interrupt triggered every year disabled 1: Periodic interrupt triggered every year enabled	R/W

Write to this register when the RUN bit in the TRHCR register is set to 0 (count stops).

An interrupt request can be generated every 0.25 seconds, 0.5 seconds, one second, minute, hour, day, month, or year. To generate an interrupt request, set one of the following bits to 1 (interrupt enabled): SEIE025, SEIE05, SEIE, MNIE, HRIE, DYIE, MOIE, and YRIE (be sure to set only one bit to 1). Table 19.4 lists RTC Periodic Interrupt Sources.

Table 19.4 RTC Periodic Interrupt Sources

Source	Interrupt Source	Interrupt Enable Bit
Periodic interrupt triggered every year	The TRHYR register is updated (one-year period)	YRIE
Periodic interrupt triggered every month	The TRHMON register is updated (one-month period)	MOIE
Periodic interrupt triggered every day	The TRHDY register is updated (one-day period).	DYIE
Periodic interrupt triggered every hour	The TRHHR register is updated (one-hour period).	HRIE
Periodic interrupt triggered every minute	The TRHMIN register is updated (one-minute period).	MNIE
Periodic interrupt triggered every second	The TRHSEC register is updated (one-second period).	SEIE
Periodic interrupt triggered every 0.5 seconds	0.5-second period	SEIE05
Periodic interrupt triggered every 0.25 seconds	0.25-second period	SEIE025

When the interrupt is enabled by the above bits, the following occurs when the periodic interrupt is generated:

- The RTCF bit in the TRHIFR register is set to 1 (periodic interrupt requested).
- The IR bit in the TRHIC register is set to 1 (interrupt requested).

19.2.14 Timer RH Alarm Minute Register (TRHAMN) in Real-Time Clock Mode

Address 011Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ENBMN	AMN6	AMN5	AMN4	AMN3	AMN2	AMN1	AMN0
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	AMN0	First digit of minute alarm data bit	Store alarm data	0 to 9 (BCD code)	R/W
b1	AMN1				R/W
b2	AMN2				R/W
b3	AMN3				R/W
b4	AMN4	Second digit of minute alarm data bit	Store alarm data	0 to 5 (BCD code)	R/W
b5	AMN5				R/W
b6	AMN6				R/W
b7	ENBMN	Minute alarm enable bit	0: Minute alarm disabled (not compared with the TRHMIN register) 1: Minute alarm enabled (compared with the TRHMIN register)		R/W

Write to this register when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

Bits AMN3 to AMN0 (First Digit of Minute Alarm Data Bit)
Bits AMN6 to AMN4 (Second Digit of Minute Alarm Data Bit)

Set values between 00 and 59 by the BCD code.

19.2.15 Timer RH Alarm Hour Register (TRHAHR) in Real-Time Clock Mode

Address 011Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ENBHR	APM	AHR5	AHR4	AHR3	AHR2	AHR1	AHR0
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	AHR0	First digit of hour alarm data bit	Store alarm data	0 to 9 (BCD code)	R/W
b1	AHR1				R/W
b2	AHR2				R/W
b3	AHR3				R/W
b4	AHR4	Second digit of hour alarm data bit	Store alarm data	0 to 2 (BCD code)	R/W
b5	AHR5				R/W
b6	APM	a.m./p.m. alarm data bit	0: a.m. 1: p.m.		R/W
b7	ENBHR	Hour alarm enable bit	0: Hour alarm disabled (not compared with the TRHHR register) 1: Hour alarm enabled (compared with the TRHHR register)		R/W

Write to this register when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

Bits AHR3 to AHR0 (First Digit of Hour Alarm Data Bit)
Bits AHR5 to AHR4 (Second Digit of Hour Alarm Data Bit)

When the HR24 bit in the TRHCR register is set to 0 (12-hour mode), set values between 00 and 11 by the BCD code. When the HR24 bit is set to 1 (24-hour mode), set values between 00 and 23 by the BCD code.

APM Bit (a.m./p.m. Alarm Data Bit)

This bit is disabled when the HR24 bit in the TRHCR register is set to 1 (24-hour mode).

19.2.16 Timer RH Alarm Day-of-Week Data Register (TRHAWK) in Real-Time Clock Mode

Address 011Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ENBWK	—	—	—	—	AWK2	AWK1	AWK0
After Reset	X	0	0	0	0	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W	Bit
b0	AWK0	Day-of-week alarm data bit	b2 b1 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Do not set.		R/W
b1	AWK1				R/W
b2	AWK2				R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
b4	—				
b5	—				
b6	—				
b7	ENBWK	Day-of-week alarm enable bit	0: Day-of-week alarm disabled (not compared with the TRHWK register) 1: Day-of-week alarm enabled (compared with the TRHWK register)		—

Write to this register when the BSY bit in the TRHSEC register is set to 0 (not while data is updated).

Bits AWK2 to AWK0 (Day-of-Week Alarm Data Bit)

Set 000b (Sunday) to 110b (Saturday).

19.2.17 Timer RH Protect Register (TRHPRC) in Real-Time Clock Mode

Address 011Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PROTECT	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0
After Reset by RTCRST Bit in TRHCR Register	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	PROTECT	Protect bit	Write to time data registers enabled/disabled 0: Write disabled 1: Write enabled	R/W

PROTECT Bit (Protect Bit)

The following registers and bit can be changed when this bit is set to 1 (write enabled):
Timer RH data registers (1) and the PM bit in the TRHCR register
When writing 1 to this bit by a program, this bit stays 1. Change the registers protected by this bit as follows:
(1) Write 1 to this bit.
(2) Write a value to the register protected by this bit.
(3) Write 0 (write disabled) to this bit.

Note:
1. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR

19.2.18 Timer RH Second Interrupt Control Register (TRHICR) in Real-Time Clock

Address 018Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INTF	—	SLINT	SLCNS	SDAREG3	SDAREG2	SDAREG1	SDAREG0
After Reset	X	0	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	SDAREG0	Specified second interrupt value set bit	b3 b2 b1 b0 < SLCNS = 0 > < SLCNS = 1 > 0 0 0 0: Do not set. 0 0 0 1: 1 second 10 seconds 0 0 1 0: 2 seconds 20 seconds 0 0 1 1: 3 seconds 30 seconds 0 1 0 0: 4 seconds 40 seconds 0 1 0 1: 5 seconds 50 seconds 0 1 1 0: 6 seconds 60 seconds 0 1 1 1: 7 seconds 70 seconds 1 0 0 0: 8 seconds 80 seconds 1 0 0 1: 9 seconds 90 seconds 1 0 1 0: 10 seconds 100 seconds 1 0 1 1: 11 seconds 110 seconds 1 1 0 0: 12 seconds 120 seconds 1 1 0 1: 13 seconds 130 seconds 1 1 1 0: 14 seconds 140 seconds 1 1 1 1: 15 seconds 150 seconds	R/W
b1	SDAREG1			R/W
b2	SDAREG2			R/W
b3	SDAREG3			R/W
b4	SLCNS	Count source select bit	0: Update of the first digit of second 1: Update of the second digit of second	R/W
b5	SLINT	Interrupt select bit (1)	0: RTC periodic interrupt 1: Specified second interrupt	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	INTF	Specified second interrupt flag (2)	0: Interrupt requested 1: No interrupt requested	R/W

Notes:
1. When not using a specified second interrupt after setting the INTF flag to 0, set the SLINT bit to 0.
2. The INTF flag is not automatically set to 0 even if an interrupt is accepted. Write 0 to this flag.
3. When the TRHICR register is written, bits SDAREG0 to SDAREG3 are reloaded to the counter.

Use this register while the RTC periodic interrupt is disabled (the TRHIER register is 00h).

Bits SDAREG3 to SDAREG0 (Specified Second Interrupt Value Set Bit)

Set the time to generate an interrupt request. Select either update of the first digit or the second digit of second in the TRHSEC register as the count source by the SLCNS bit.
When writing to the TRHICR register while the RUN bit in the TRHCR register is 1, the count starts with the contents of bits SDAREG3 to SDAREG0 and SLICNS. When writing to the TRHICR register while the RUN bit is 0, the count starts when the RUN bit is set to 1.

INTF Bit (Specified Second Interrupt Flag)

[Condition for setting to 0]
Write 0 after reading this bit. Note a maximum of 0.04 ms is required before the INTF bit is set to 0. When writing 0 to this bit is the read value is 1, this bit is set to 0.
[Condition for setting to 1]
When the value set in bits SDAREG3 to SDAREG0 is decremented and changes to 0.
When writing 0 to this bit if the read value is 0, this bit remains unchanged (if this bit changes from 0 to 1 after reading this bit, this bit remains 1 even if writing 0). Writing 1 has no effect.

When using a specified second interrupt, confirm the state of the INTF bit.
When the first digit of second (or the second digit of second) is updated while the RUN bit in the TRHCR register is 1 (count starts), the INTF bit may be set to 1 because count operation is performed. Once the INTF bit is set to 1, this bit remains as 1 until it is set to 0 or initialized by the RTCRST bit in the TRHCR register.
The INTF bit is set to 1 within about 0.04 ms after the BSY bit is changed from 1 (while data is updated) to 0 (not while data is updated). Adjust the timing when setting the INTF bit to 0 while the RUN bit is 1.

19.2.19 Operating Example

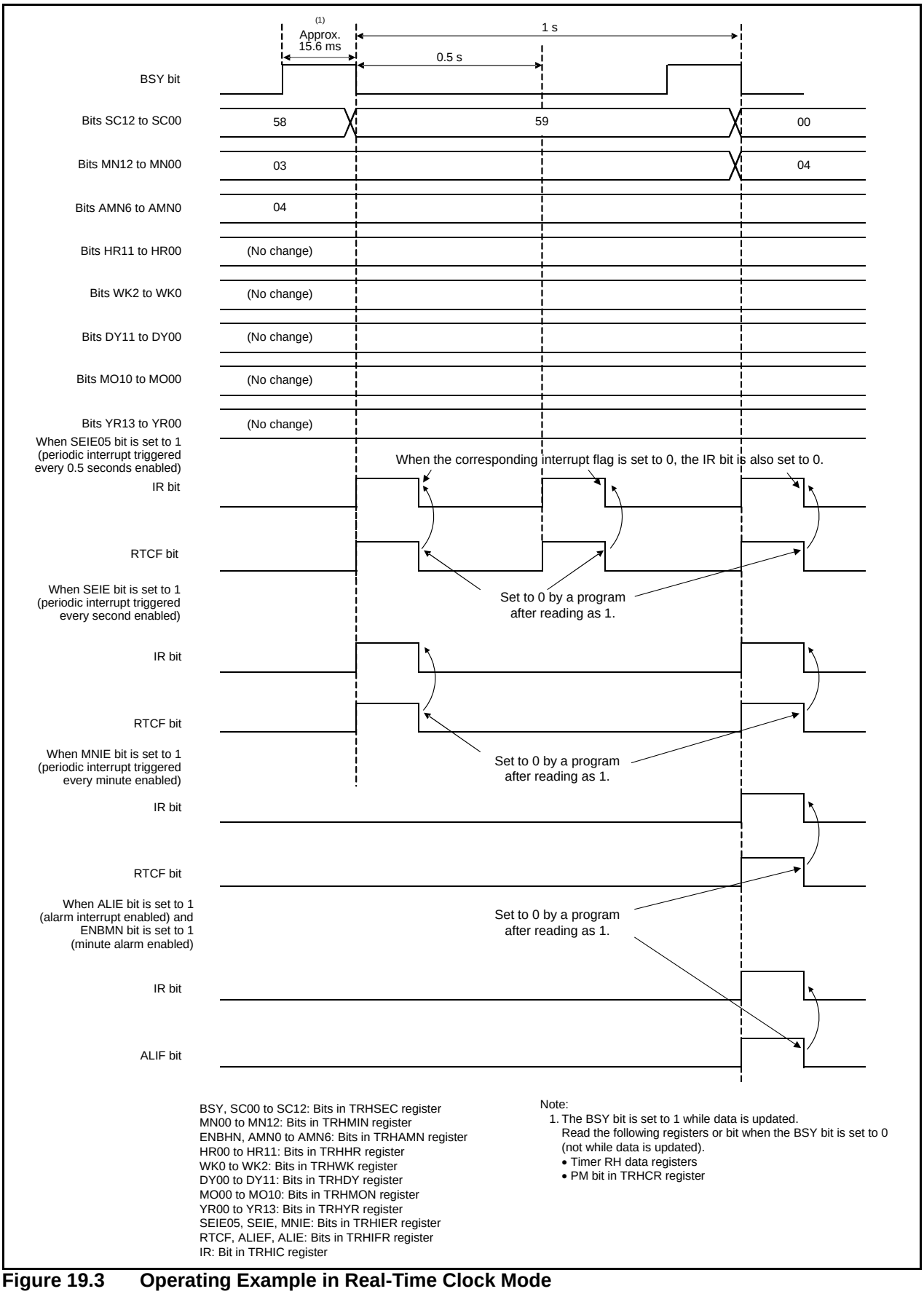

(1)
Approx.
15.6 ms
1 s
0.5 s
BSY bit
Bits SC12 to SC00
58
59
00
Bits MN12 to MN00
03
04
Bits AMN6 to AMN0
04
Bits HR11 to HR00
(No change)
Bits WK2 to WK0
(No change)
Bits DY11 to DY00
(No change)
Bits MO10 to MO00
(No change)
Bits YR13 to YR00
(No change)
When SEIE05 bit is set to 1
(periodic interrupt triggered
every 0.5 seconds enabled)
When the corresponding interrupt flag is set to 0, the IR bit is also set to 0.
IR bit
RTCF bit
When SEIE bit is set to 1
(periodic interrupt triggered
every second enabled)
Set to 0 by a program
after reading as 1.
IR bit
RTCF bit
When MNIE bit is set to 1
(periodic interrupt triggered
every minute enabled)
Set to 0 by a program
after reading as 1.
IR bit
RTCF bit
When ALIE bit is set to 1
(alarm interrupt enabled) and
ENBMN bit is set to 1
(minute alarm enabled)
Set to 0 by a program
after reading as 1.
IR bit
ALIF bit
BSY, SC00 to SC12: Bits in TRHSEC register
MN00 to MN12: Bits in TRHMIN register
ENBHN, AMN0 to AMN6: Bits in TRHAMN register
HR00 to HR11: Bits in TRHHR register
WK0 to WK2: Bits in TRHWK register
DY00 to DY11: Bits in TRHDY register
MO00 to MO10: Bits in TRHMON register
YR00 to YR13: Bits in TRHYR register
SEIE05, SEIE, MNIE: Bits in TRHIER register
RTCF, ALIEF, ALIE: Bits in TRHIFR register
IR: Bit in TRHIC register
Note:
1. The BSY bit is set to 1 while data is updated.
Read the following registers or bit when the BSY bit is set to 0
(not while data is updated).
• Timer RH data registers
• PM bit in TRHCR register

Figure 19.3 Operating Example in Real-Time Clock Mode

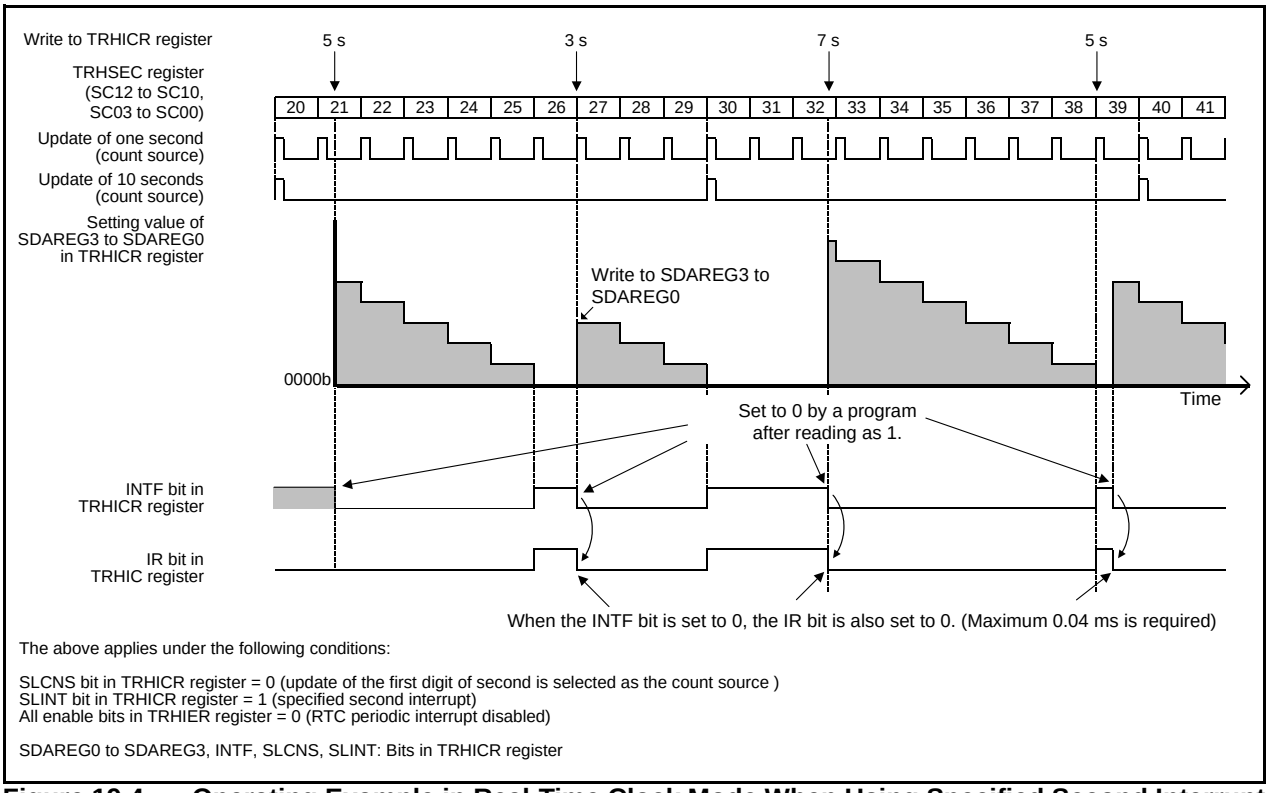

Write to TRHICR register
5 s
3 s
7 s
5 s
TRHSEC register
(SC12 to SC10,
SC03 to SC00)
20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41
Update of one second
(count source)
Update of 10 seconds
(count source)
Setting value of
SDAREG3 to SDAREG0
in TRHICR register
Write to SDAREG3 to
SDAREG0
0000b
Time
Set to 0 by a program
after reading as 1.
INTF bit in
TRHICR register
IR bit in
TRHIC register
When the INTF bit is set to 0, the IR bit is also set to 0. (Maximum 0.04 ms is required)
The above applies under the following conditions:
SLCNS bit in TRHICR register = 0 (update of the first digit of second is selected as the count source)
SLINT bit in TRHICR register = 1 (specified second interrupt)
All enable bits in TRHIER register = 0 (RTC periodic interrupt disabled)
SDAREG0 to SDAREG3, INTF, SLCNS, SLINT: Bits in TRHICR register

Figure 19.4 Operating Example in Real-Time Clock Mode When Using Specified Second Interrupt

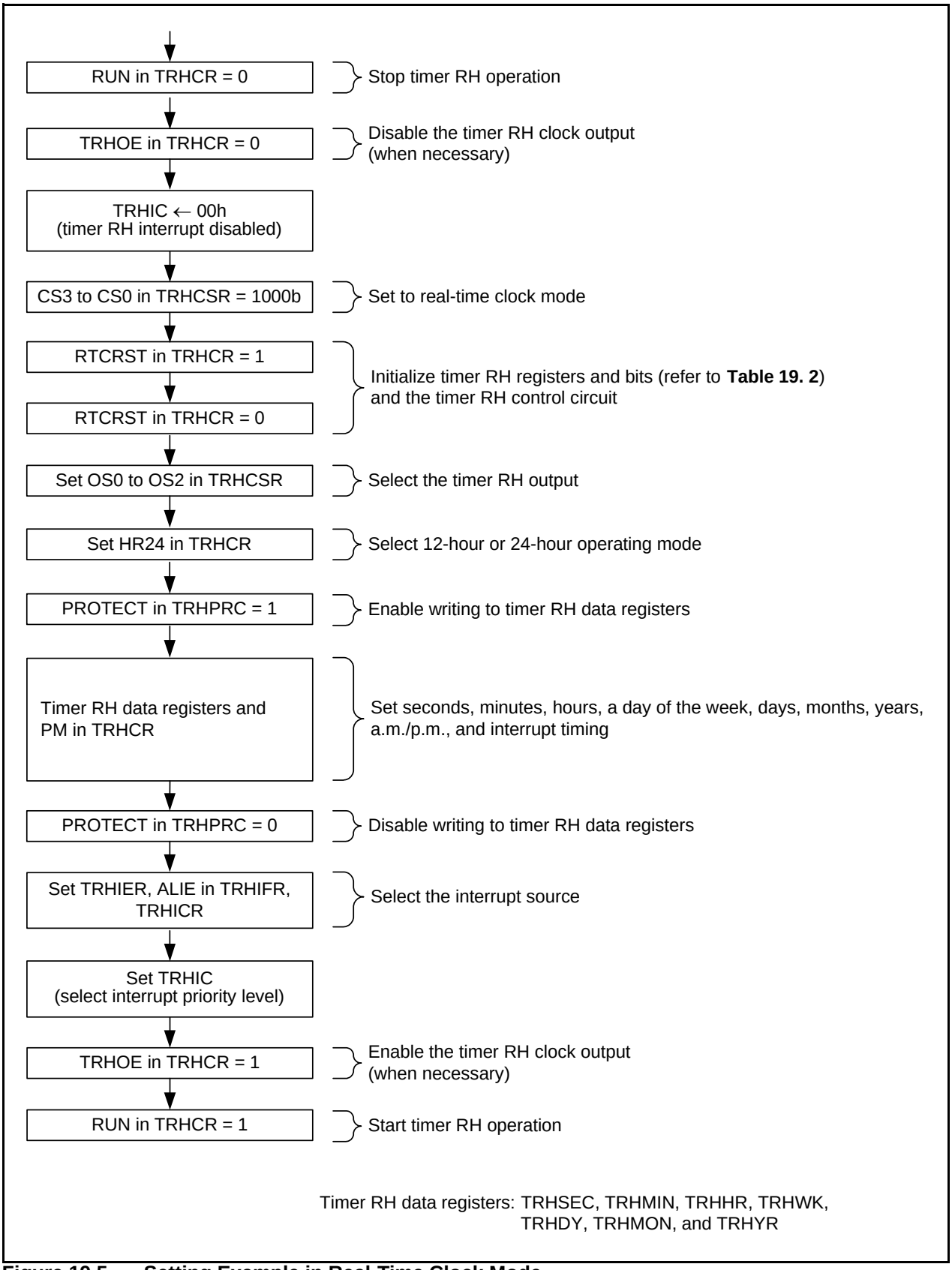

RUN in TRHCR = 0
Stop timer RH operation
TRHOE in TRHCR = 0
Disable the timer RH clock output (when necessary)
TRHIC ← 00h (timer RH interrupt disabled)
CS3 to CS0 in TRHCSR = 1000b
Set to real-time clock mode
RTCRST in TRHCR = 1
RTCRST in TRHCR = 0
Initialize timer RH registers and bits (refer to Table 19. 2) and the timer RH control circuit
Set OS0 to OS2 in TRHCSR
Select the timer RH output
Set HR24 in TRHCR
Select 12-hour or 24-hour operating mode
PROTECT in TRHPRC = 1
Enable writing to timer RH data registers
Timer RH data registers and PM in TRHCR
Set seconds, minutes, hours, a day of the week, days, months, years, a.m./p.m., and interrupt timing
PROTECT in TRHPRC = 0
Disable writing to timer RH data registers
Set TRHIER, ALIE in TRHIFR, TRHICR
Select the interrupt source
Set TRHIC (select interrupt priority level)
TRHOE in TRHCR = 1
Enable the timer RH clock output (when necessary)
RUN in TRHCR = 1
Start timer RH operation
Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR

Figure 19.5 Setting Example in Real-Time Clock Mode

19.2.20 Alarm Function

Time data (1) and alarm data (2) are compared, and a compare match is detected.
An alarm can be generated by minutes, hours, or day of the week, or any combination of these. Set an ENB bit in the corresponding alarm register to 1. Hour is a.m. or p.m.
When the comparison result matches, the following occurs:

- The ALIF bit in the TRHIFR register is set to 1 (alarm interrupt requested).
- When the ALIE bit in the TRHIFR register is 1 (alarm interrupt enabled), the IR bit in the TRHIC register is set to 1 (alarm interrupt requested).

Notes:

1. Bits for time data are as follows:
   Bits MN12 to MN10 and MN03 to MN00 in the TRHMIN register
   Bits HR11 to HR10 and HR03 to HR00 in the TRHHR register
   The PM bit in the TRHCR register
   Bits WK2 to WK0 in the TRHWK register
2. Bits for alarm data are as follows:
   Bits AMN6 to AMN4 and AMN3 to AMN0 in the TRHAMN register
   Bits AHR5 to AHR4 and AHR3 to AHR0 in the TRHAHR register
   The APM bit in the TRHAHR register
   Bits AWK2 to AWK0 in the TRHAWK register

Figure 19.6 shows the Alarm Time Setting Procedure.

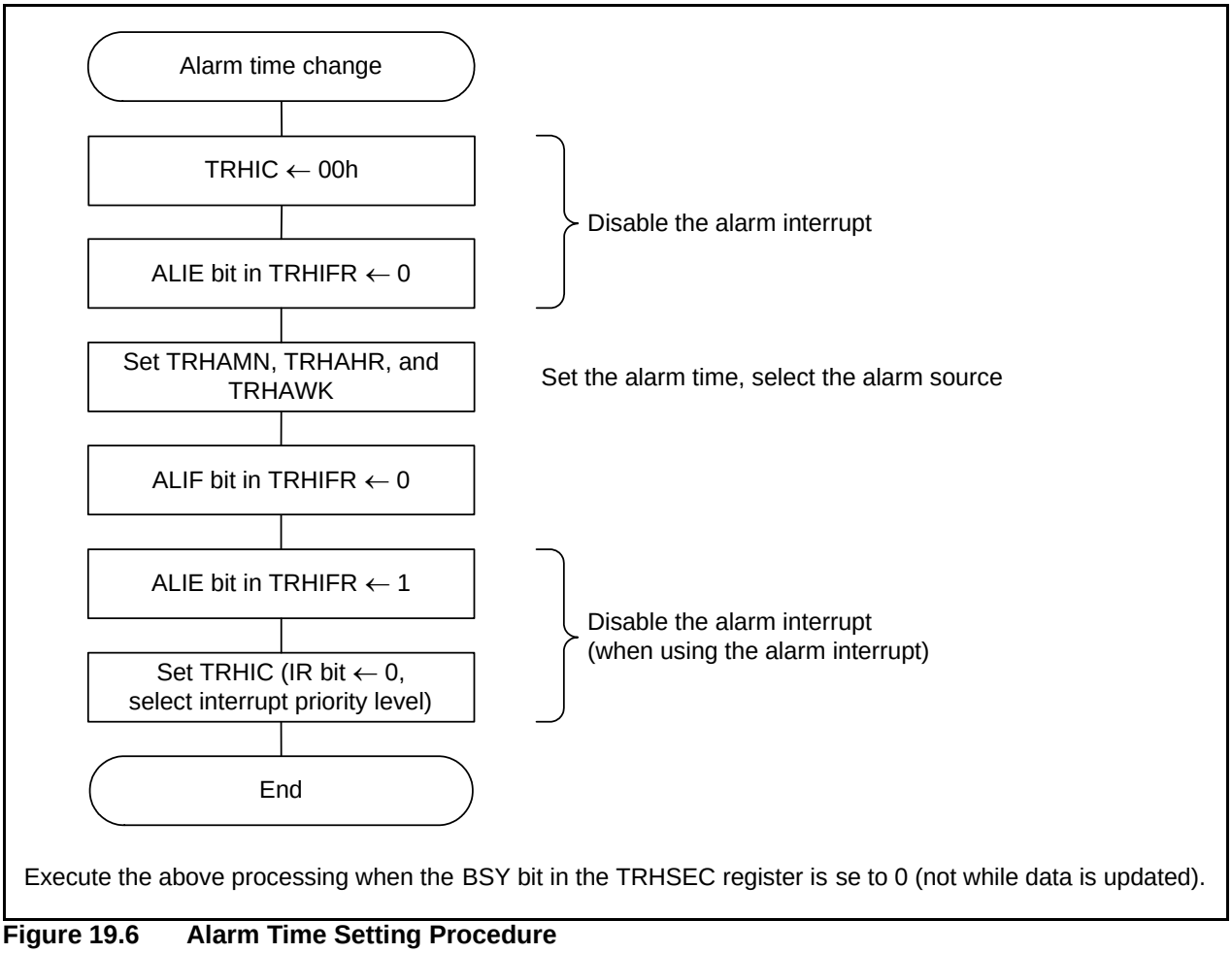
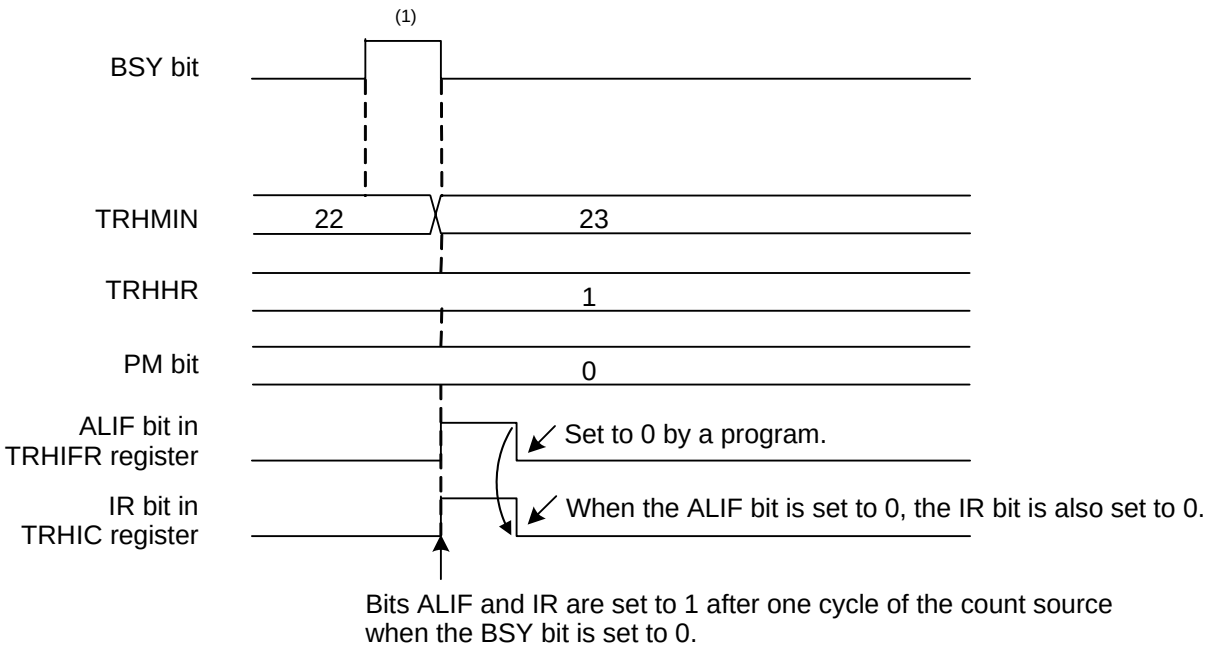

Alarm time change
TRHIC ← 00h
ALIE bit in TRHIFR ← 0
Disable the alarm interrupt
Set TRHAMN, TRHAHR, and TRHAWK
Set the alarm time, select the alarm source
ALIF bit in TRHIFR ← 0
ALIE bit in TRHIFR ← 1
Set TRHIC (IR bit ← 0, select interrupt priority level)
Disable the alarm interrupt (when using the alarm interrupt)
End
Execute the above processing when the BSY bit in the TRHSEC register is se to 0 (not while data is updated).

Figure 19.6 Alarm Time Setting Procedure


(1)
BSY bit
TRHMIN
22
23
TRHHR
1
PM bit
0
ALIF bit in TRHIFR register
Set to 0 by a program.
IR bit in TRHIC register
When the ALIF bit is set to 0, the IR bit is also set to 0.
Bits ALIF and IR are set to 1 after one cycle of the count source when the BSY bit is set to 0.

The above applies under the following conditions:
- HR24 bit in TRHCR register = 0 (12-hour mode)
- ENBMN bit in TRHAMN register = 1 (minute alarm enabled), bits AMN6 to AMN4 = 2, and bits AMN3 to AMN0 = 3 (23 minutes)
- ENBHR bit in TRHAHR register = 1 (hour alarm enabled), APM bit = 0 (a.m.), bits AHR5 to AHR4 = 0, and bits AHR3 to AHR0 = 1 (1 o'clock)
- ENBWK bit in TRHAWK register = 0 (day-of-week alarm disabled)
- ALIE bit in TRHIFR register = 1 (alarm interrupt enabled)

BSY: Bit in TRHSEC register
TRHMIN: Bits MN12 to MN10 and MN03 to MN00 in TRHMIN register
TRHHR: Bits HR11 to HR10 and HR03 to HR00 in TRHHR register
PM: Bit in TRHCR register

Note:
1. The BSY bit is set to 1 while data is updated.
   Read the following registers or bit when the BSY bit is set to 0 (not while data is updated).
   - Timer RH data registers
   - PM bit in TRHCR register

Figure 19.7 Alarm Function

19.2.21 Second Adjustment Function

Two functions are available as the second adjustment function: reset adjustment and 30 seconds adjustment.

19.2.21.1 Reset Adjustment Function

The reset adjustment function initializes the TRHSEC register and the internal counters (3-bit, 4-bit, and 8-bit counters). When 1 is written to the RSTADJ bit in the TRHIFR register while the BSY bit in the TRHSEC register is 0 (not while data is updated), the TRHSEC register is set to 00h and the internal counter is initialized and the count restarts after about 0.1 ms. When 1 is written to the RSTADJ bit while the BSY bit is 1 (while data is updated), the TRHSEC register is set to 00h and the internal counter is initialized and the count restarts when the data is updated.
The other timer RH data registers are not affected. After the RSTADJ bit is set to 1, wait for about 0.2 ms or more to write to the TRHSEC register.

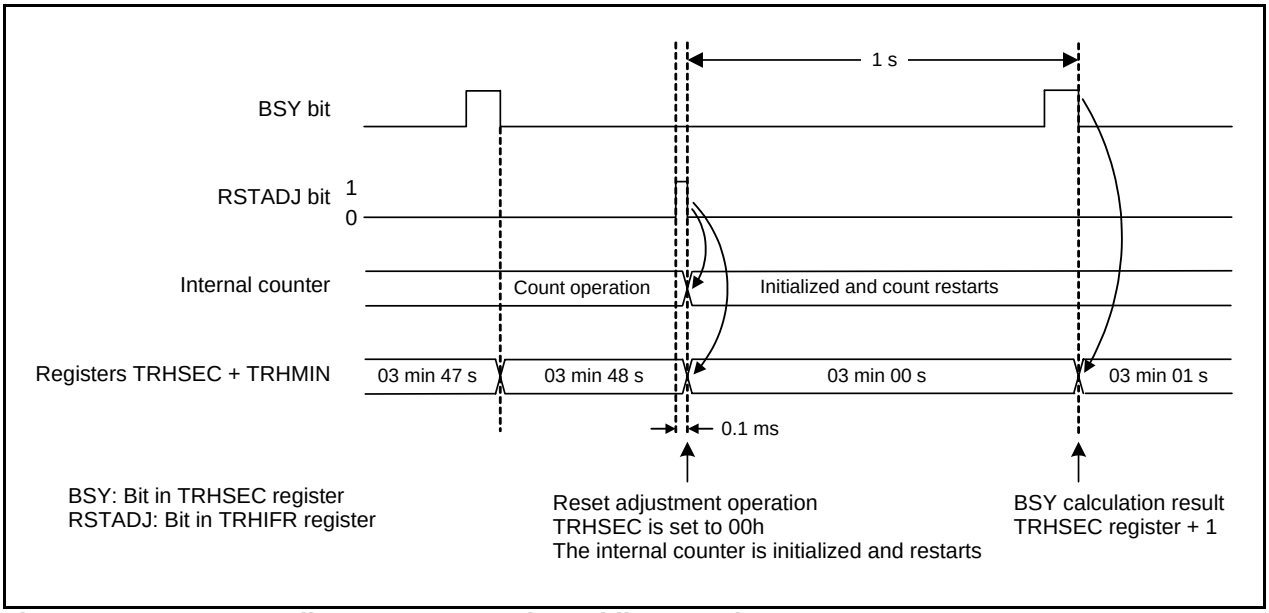


Figure 19.8 Reset Adjustment Generation While BSY Bit = 0

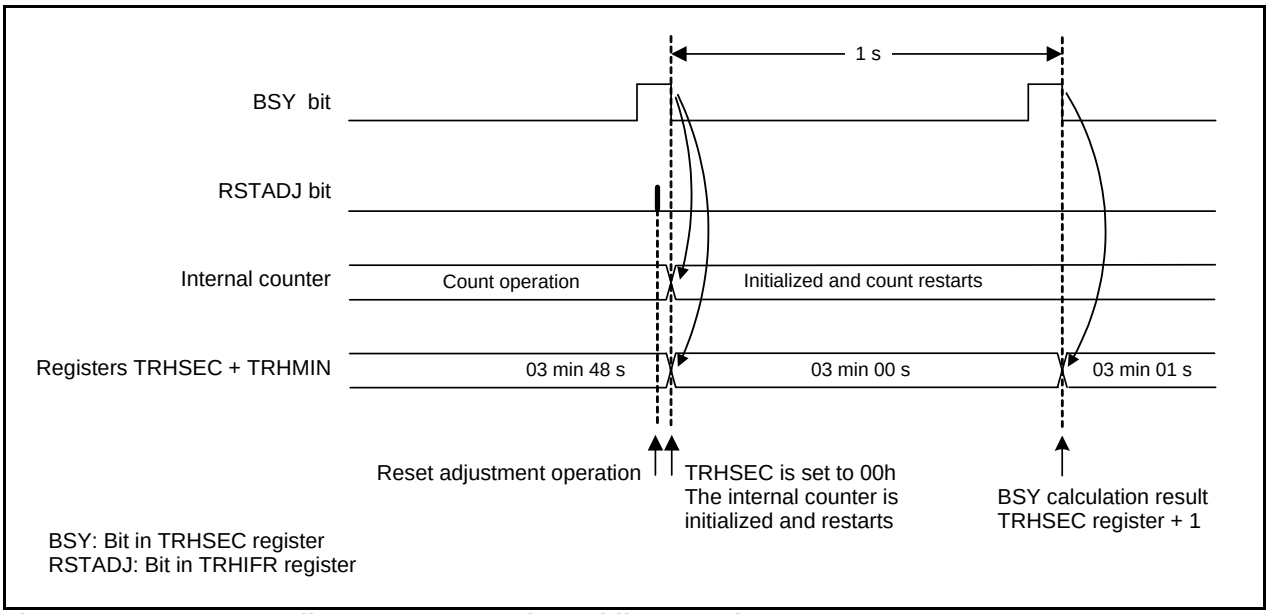


Figure 19.9 Reset Adjustment Generation While BSY Bit = 1

19.2.21.2 30 Seconds Adjustment Function

The 30 seconds adjustment function rounds 29 seconds or less to 00 and 30 seconds or more to 00.
When 1 is written to the 30SADJ bit in the TRHIFR register while the BSY bit is 0 (not while data is updated), the TRHSEC register is adjusted by 30 seconds when the data is updated. When 1 is written to the 30SADJ bit while the BSY bit is 1 (while data is updated), the TRHSEC register is adjusted by 30 seconds when the data is updated next time. The other timer RH data register are not affected during 30 seconds adjustment.

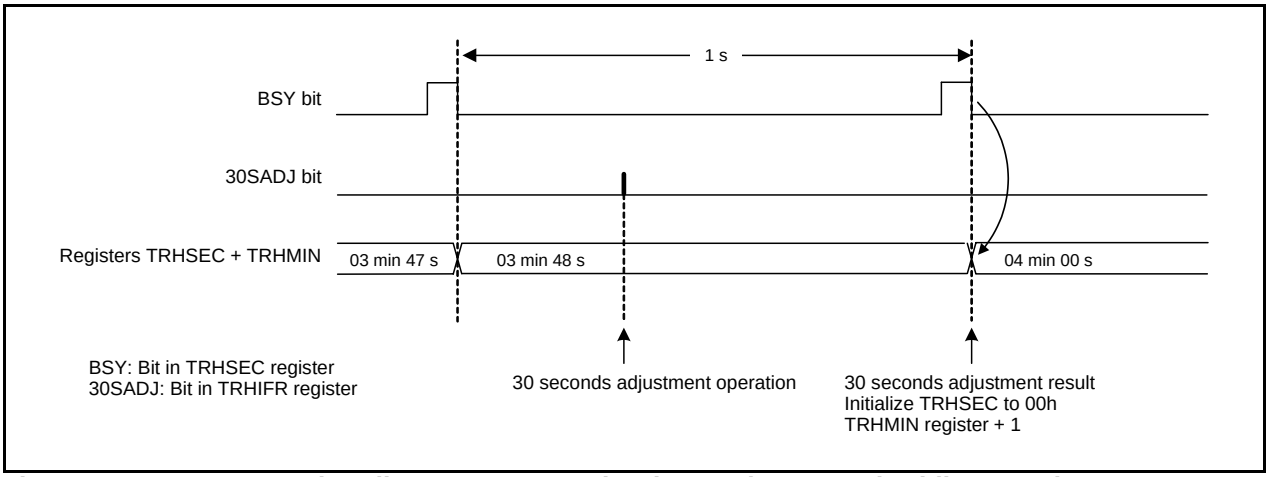


Figure 19.10 30 Seconds Adjustment Generation (Second Data ≥ 30) While BSY Bit = 0

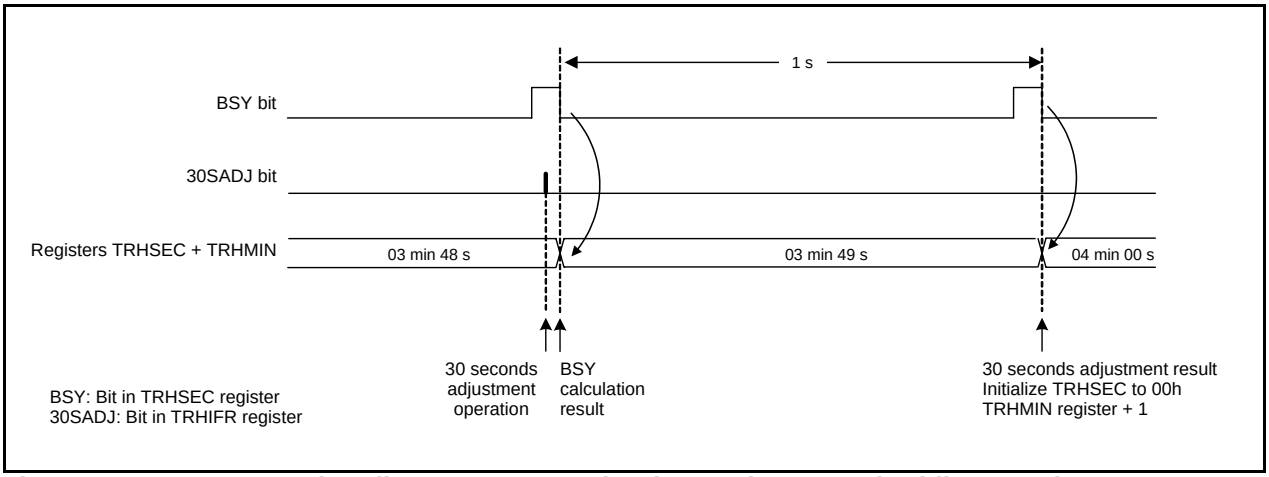


Figure 19.11 30 Seconds Adjustment Generation (Second Data ≥ 30) While BSY Bit = 1

19.2.22 Clock Error Correction Function

This function corrects a frequency error of fC-TRH. As shown in the basic operation in Figure 19.12, the internal counter of the one-second generation circuit counts 32.768 kHz 32768 times. When fC-TRH is larger or smaller than 32.768 kHz, it can be corrected by increasing or decreasing the number of count.
Select automatic correction or correction by software by the AADJE bit in the TRHCR register.

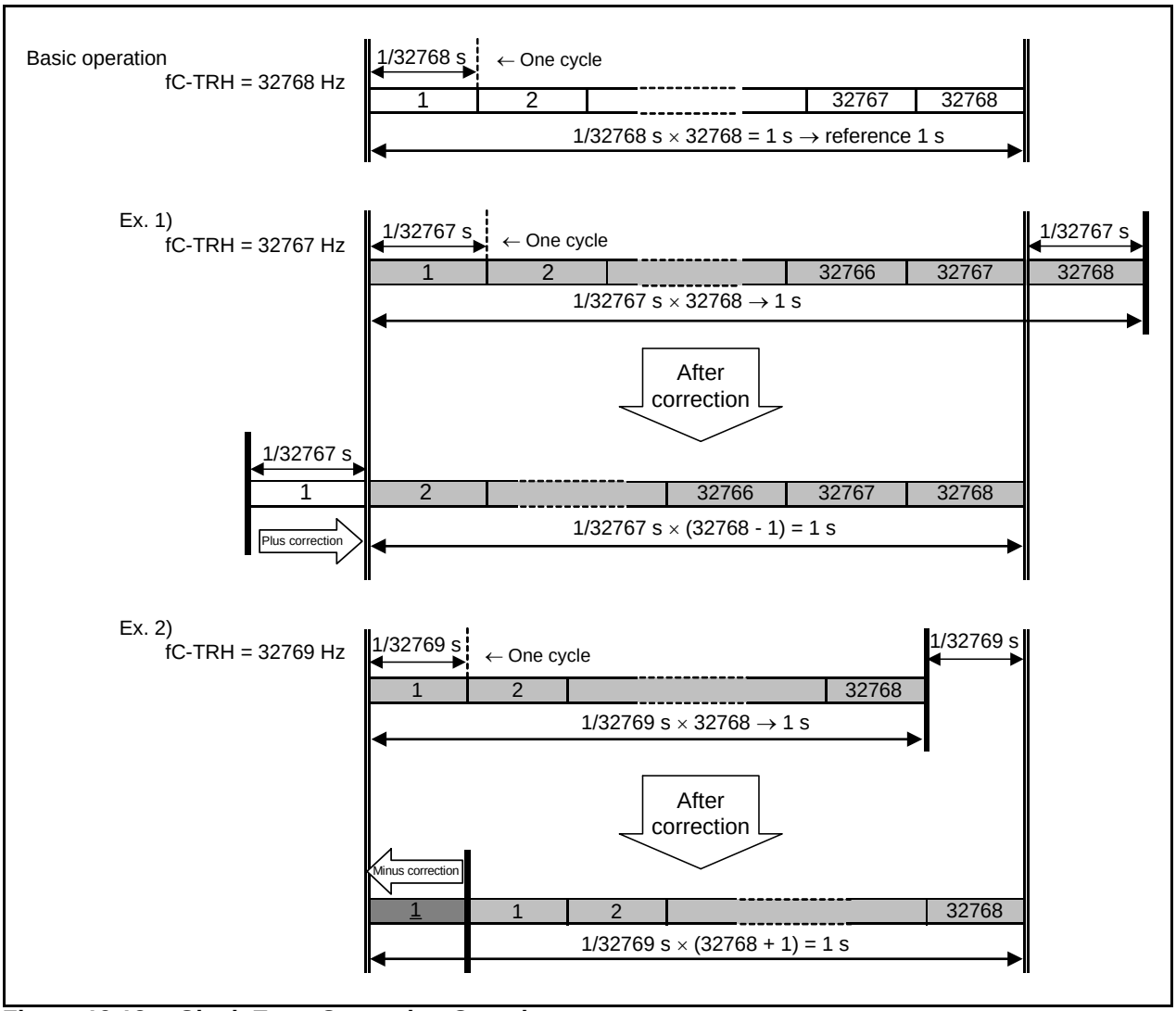


Figure 19.12 Clock Error Correction Overview

19.2.22.1 Automatic Correction Function

When the AADJE bit in the TRHCR register is set to 1, an automatic correction function is enabled.
Select a correction timing by the AADJM bit in the TRHCSR register. Set a correction value and correction content (add/subtract) to the TRHADJ register. The correction value is automatically added or subtracted at the selected correction timing. However, during automatic correction, do no rewrite the registers and bits associated correction while the BSY bit is 1 (about 15. 6 ms) and after 2 ms when the BSY bit is changed from 1 to 0.

Registers and bits associated with correction: TRHADJ, AADJM in TRHCSR, and AADJE in TRHCR

Examples are as follows:

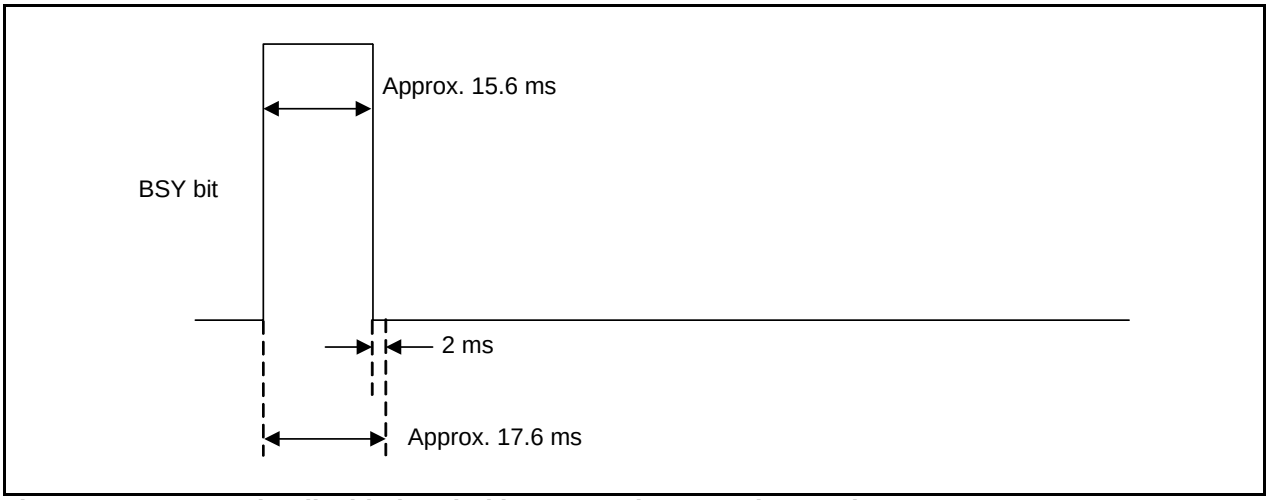


Figure 19.13 Rewrite disabled period in automatic correction mode

Ex. 1) fC-TRH = 32767 Hz
1. Example of Correction Procedure
One cycle to make one second is 32767 Hz (= 1/32767 s). Thus, counting 32768 times makes the second longer than the reference one second, causing the clock to lose time.
The clock needs to be set forward to correct this error. It can be corrected to the reference one second (counts: 32767 times) by setting the correction value 1 to the plus side.
Set the correction value 60 to the plus side to perform automatic correction every minute.

Register setting
- The AADJM bit in the TRHCSR register: 0 (corrected every minute)
- Bits PLUS and MINUS in the TRHADJ register: 10b (corrected to the plus side)
- Bits ADJ5 to ADJ0 in the TRHADJ register: 3Ch (60)

Ex. 2) fC-TRH = 32769 Hz
2. Example of Correction Procedure
One cycle to make a one second is 32769 Hz (= 1/32769 s). Thus, counting 32768 times makes the second shorter than the reference one second, causing the clock to gain time.
The clock needs to be set backward to correct this error. It can be corrected to the reference one second (counts: 32769 times) by setting the correction value 1 to the minus side.
Set the correction value 10 to the minus side to perform an automatic correction every 10 seconds.

Register setting
- The AADJM bit in the TRHCSR register: 1 (corrected every 10 seconds)
- Bits PLUS and MINUS in the TRHADJ register: 01b (corrected to the minus side)
- Bits ADJ5 to ADJ0 in the TRHADJ register: 0Ah (10)

19.2.22.2 Correction by Software

When the AADJE bit in the TRHCR register is set to 0, correction by software is enabled. Write a correction value and correction content (add/subtract) to the TRHADJ register at an arbitrary timing. Correction is performed when the write instruction is executed.
However, after correction by software is set once, wait for about 62.6 ms or more to rewrite the registers and bits associated with correction.

Ex. 1) fC-TRH = 32769 Hz
How to correct
One cycle to make one second is 32769 Hz (= 1/32769 s). Thus, counting 32768 times makes the second shorter than the reference one second, causing the clock to gain time.
The clock needs to be set backward to correct this error. It can be corrected to the reference one second (counts: 32769 times) by setting the correction value to minus 1.
Set the correction value 1 to the minus side every second by software.

Register setting
- Bits PLUS and MINUS in the TRHADJ register: 01b (corrected to the minus side)
- Bits ADJ5 to ADJ0 in the TRHADJ register: 01h (01)
- Write to the TRHADJ register every second.

19.2.22.3 Correction Mode Change Procedure

Change correction mode following the procedure shown below:

(1) When changing from correction by software to automatic correction:
Do not rewrite the registers and bits associated with correction for about 62.6 ms after correction by software is set once. Also, do not rewrite the above registers and bits while the BSY bit is 1 (while data is updated).

Registers and bits associated with correction: TRHADJ, AADJM in TRHCSR, and AADJE in TRHCR

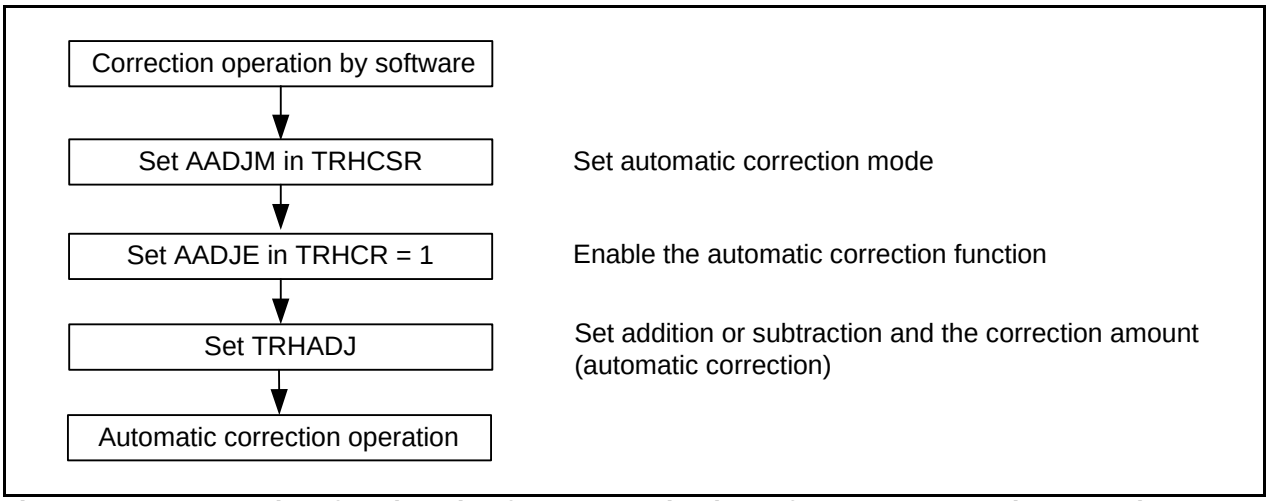

Correction operation by software
Set AADJM in TRHCSR
Set automatic correction mode
Set AADJE in TRHCR = 1
Enable the automatic correction function
Set TRHADJ
Set addition or subtraction and the correction amount (automatic correction)
Automatic correction operation

Figure 19.14 Procedure for Changing from Correction by Software to Automatic Correction

(2) When changing from automatic correction to correction by software:
Do not rewrite the registers and bits associated with correction while the BSY bit is 1 (while data is updated).
Do not rewrite the above registers and bits for 2 ms after the BSY bit is changed from 1 (while data is updated) to 0 (not while data is updated). Refer to Figure 19.13.

Registers and bits associated with correction: TRHADJ, AADJM in TRHCSR, and AADJE in TRHCR

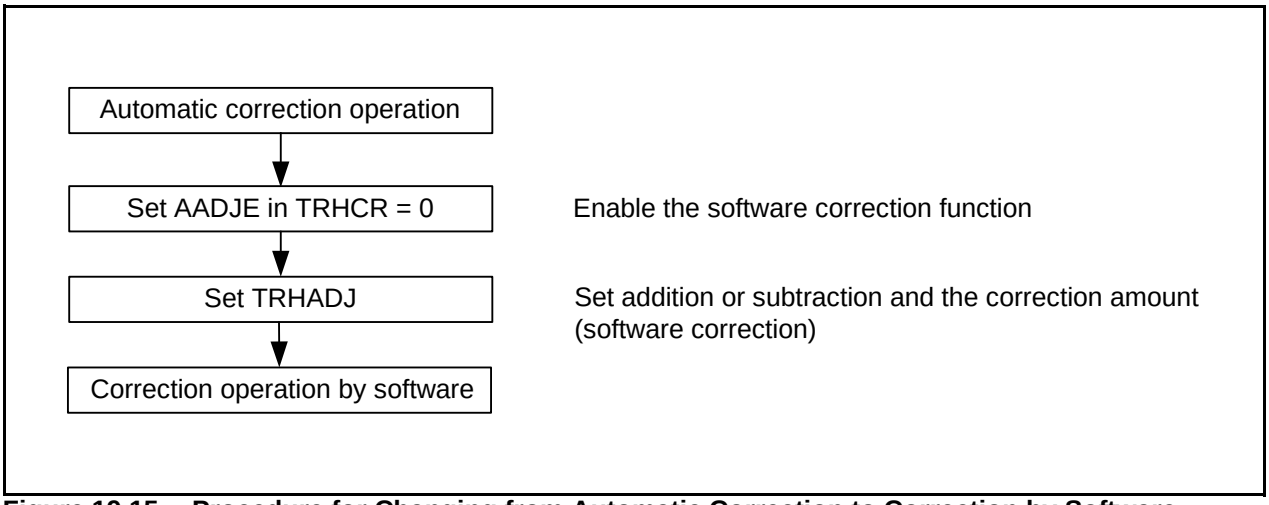

Automatic correction operation
Set AADJE in TRHCR = 0
Enable the software correction function
Set TRHADJ
Set addition or subtraction and the correction amount (software correction)
Correction operation by software

Figure 19.15 Procedure for Changing from Automatic Correction to Correction by Software

19.2.23 Clock Output

When the TRHOE bit in the TRHCR register is set to 1 (TRHO output enabled), a clock is output from the TRHO pin. Select the clock by bits OS2 to OS0 in the TRHCSR register.

19.3 Output Compare Mode

In output compare mode, the count source is counted using the 8-bit counter and a compare value match is detected with the counter. Figure 19.16 shows a Block Diagram of Output Compare Mode and Table 19.5 lists the Output Compare Mode Specifications.

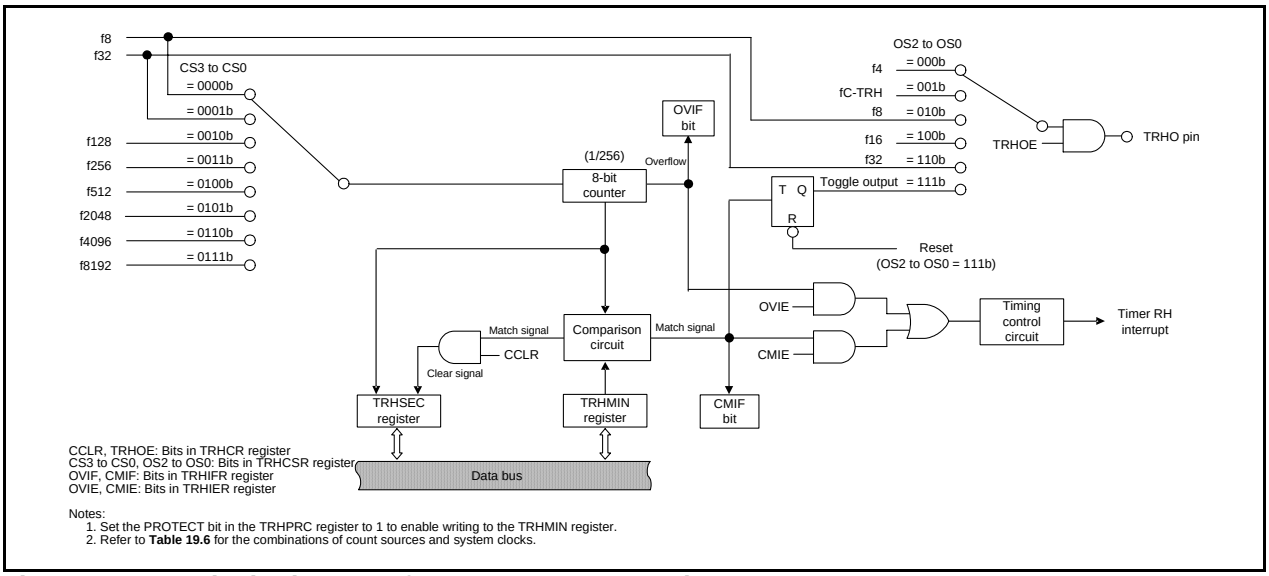


Figure 19.16 Block Diagram of Output Compare Mode

Table 19.5 Output Compare Mode Specifications

Item	Specification
Count sources	f8, f32, f128, f256, f512, f2048, f4096, f8192
Count operations	Increment
Count period	• The CCLR bit in the TRHCR register is set to 0 (free-running operation): 1/fi × 65,536 fi: Frequency of count source • The CCLR bit in the TRHCR register is set to 1 (TRC register is set to 00h by TRHMIN register compare match): 1/fi × (n + 1) n: Value set in TRHMIN register
Count start condition	1 (count starts) is written to the RUN bit in the TRHCR register.
Count stop condition	0 (count stops) is written to the RUN bit in the TRHCR register.
Interrupt request generation timing	• When the contents of the 8-bit counter and the TRHMIN register match. • When the 8-bit counter overflows.
TRHO pin function	Select either one of the following • Programmable I/O port • Output of f4, f8, fC-TRH, f16, f32 • Toggle output at every compare match
Read from timer	When the TRHSEC register is read, the 8-bit counter value can be read. When the TRHMIN register is read, the compare value can be read.
Write to timer	Writing to the TRHSEC register is disabled. When the PROTECT bit in the TRHPRC register is set to 1 (write enabled) and the RUN bit in the TRHCR register is set to 0 (count stops), writing to the TRHMIN register is enabled.
Selectable functions	• Toggle output function (TRHO output polarity is inverted) • Timing for setting the TRHSEC register to 00h When the CCLR bit in the TRHCR register is set to 0, overflow. When the CCLR bit in the TRHCR register is set to 1, compare match with the TRHMIN register. • When 111b is written to bits OS2 to OS0 in the TRHCSR register, the output level is initialized to 0.

19.3.1 Timer RH Counter Data Register (TRHSEC) in Output Compare Mode

Address 0110h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Function	R/W
b7 to b0	8-bit counter data can be read. Even if timer RH stops counting, the count value is retained. When the CCLR bit in the TRHCR register is set to 0, even if a compare match occurs, the count continues. When the CCLR bit is set to 1, the TRHSEC register is set to 00h.	R

19.3.2 Timer RH Compare Data Register (TRHMIN) in Output Compare Mode

Address 0111h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MN7	MN6	MN5	MN4	MN3	MN2	MN1	MN0
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MN0	Compare data bit 0	8-bit compare data is stored. Write the compare value.	R/W
b1	MN1	Compare data bit 1		R/W
b2	MN2	Compare data bit 2		R/W
b3	MN3	Compare data bit 3		R/W
b4	MN4	Compare data bit 4		R/W
b5	MN5	Compare data bit 5		R/W
b6	MN6	Compare data bit 6		R/W
b7	MN7	Compare data bit 7		R/W

Do not write 00h to the TRHMIN register when the CCLR bit in the TRHCR register is set to 1.

19.3.3 Timer RH Control Register (TRHCR) in Output Compare Mode

Address 0117h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RUN	HR24	PM	RTCRST	CCLR	LFLAG	TRHOE	AADJE
After Reset	X	X	X	0	0	X	0	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	X	X	1	X	0

Bit	Symbol	Bit Name	Function	R/W
b0	AADJE	Set to 0 in output compare mode.		R/W
b1	TRHOE	Timer RH output enable bit	0: Output disabled 1: Output enabled	R/W
b2	LFLAG	Set to 0 in output compare mode.		R
b3	CCLR	Counter clear enable bit	0: TRHSEC register initialization by compare match disabled 1: TRHSEC register initialization by compare match enabled	R/W
b4	RTCRST	Timer RH reset bit (1)	0: Normal operation 1: Timer RH reset	R/W
b5	PM	Set to 0 in output compare mode.		R/W
b6	HR24			R/W
b7	RUN	Timer RH operation start bit	0: Count stops 1: Count starts	R/W

Note:
1. Set the RTCRST bit to 0 after setting it to 1.

TRHOE Bit (Timer RH Output Enable Bit)

Rewrite this bit when the RUN bit is set to 0 (count stops).

CCLR Bit (Count Clear Enable Bit)

Rewrite this bit when the RUN bit is set to 0 (count stops).
Set this bit to select whether to reset the TRHSEC register at the compare match between registers TRHSEC and TRHMIN. This bit is enabled only when the CS3 bit in the TRHCSR register is set to 0.

RTCRST Bit (Timer RH Reset Bit)

When this bit is set to 1, the registers and bits listed in Table 19.3 are initialized to the values after reset, and the timer RH control circuit is initialized.

19.3.4 Timer RH Count Source Select Register (TRHCSR) in Output Compare Mode

Address 0118h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	AADJM	OS2	OS1	OS0	CS3	CS2	CS1	CS0
After Reset	X	0	0	0	1	0	0	0
After Reset by RTCRST Bit in TRHCR Register	0	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	CS0	Count source select bit (1)	In output compare mode (CS3 bit = 0), set to the following: b3 b2 b1 b0 0 0 0 0: f8 0 0 0 1: f32 0 0 1 0: f128 0 0 1 1: f256 0 1 0 0: f512 0 1 0 1: f2048 0 1 1 0: f4096 0 1 1 1: f8192 1 X X X: Do not set.	R/W
b1	CS1			R/W
b2	CS2			R/W
b3	CS3			R/W
b4	OS0	Timer RH output select bit	b6 b5 b4 0 0 0: f4 0 0 1: fC-TRH 0 1 0: f8 0 1 1: Do not set. 1 0 0: f16 1 0 1: Do not set. 1 1 0: f32 1 1 1: Toggle output at the compare match When writing 111b to bits OS2 to OS0, the internal output level is initialized to “L”.	R/W
b5	OS1			R/W
b6	OS2			R/W
b7	AADJM	Set to 0 in output compare mode.		R/W

X: 0 or 1

Note:

1. When f8 is used as the count source, do not use f4, f8, or f16 as the system clock.
   When f32 is used as the count source, do not use f16 as the system clock.
   Refer to Table 19.6 for details.

Bits CS3 to CS0 (Count Source Select Bit)

Rewrite these bits when the RUN bit in the TRHCR register is set to 0 (count stops).

Bits OS2 to OS0 (Timer RH Output Select Bit)

Rewrite these bits when the RUN bit in the TRHCR register is set to 0 (count stops).
These bits are enabled when the TRHOE bit in the TRHCR register is set to 1 (TRHO output enabled).

Table 19.6 Combinations of Count Sources and System Clocks

System Clocks / Count Sources	f1	f2	f4	f8	f16
f8	Enabled	Enabled	Disabled	Disabled	Disabled
f32	Enabled	Enabled	Enabled	Enabled	Disabled
f128	Enabled	Enabled	Enabled	Enabled	Enabled
f256	Enabled	Enabled	Enabled	Enabled	Enabled
f512	Enabled	Enabled	Enabled	Enabled	Enabled
f2048	Enabled	Enabled	Enabled	Enabled	Enabled
f4096	Enabled	Enabled	Enabled	Enabled	Enabled
f8192	Enabled	Enabled	Enabled	Enabled	Enabled

19.3.5 Timer RH Interrupt Flag Register (TRHIFR) in Output Compare Mode

Address 011Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	RSTADJ	ADJ30S	ALIE	OVIF	CMIF
After Reset	0	0	0	0	0	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMIF	Compare match interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	OVIF	Overflow interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b2	ALIE	Set to 0 in output compare mode.		R/W
b3	ADJ30S			W
b4	RSTADJ			W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

CMIF Bit (Compare Match Interrupt Flag)

[Condition for setting to 0]
Write 0 after reading this bit. When writing 0 to this bit if the read value is 1, this bit is set to 0.
[Condition for setting to 1]
The contents of registers TRHSEC and TRHMIN match.
When writing 0 to this bit if the read value is 0, this bit remains unchanged (if this bit changes from 0 to 1 after reading this bit, this bit remains 1 even if writing 0). Writing 1 has no effect.

OVIF Flag (Overflow Interrupt Flag)

[Condition for setting to 0]
Write 0 after reading this bit. When writing 0 to this bit if the read value is 1, this bit is set to 0.
[Condition for setting to 1]
The 8-bit counter overflows.
When writing 0 to this bit if the read value is 0, this bit remains unchanged (if this bit changes from 0 to 1 after reading this bit, this bit remains 1 even if writing 0). Writing 1 has no effect.

19.3.6 Timer RH Interrupt Enable Register (TRHIER) in Output Compare Mode

Address 011Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	YRIE	MOIE	DYIE	HRIE	MNIE	SEIE	OVIE	CMIE
After Reset	X	X	X	X	X	X	X	X
After Reset by RTCRST Bit in TRHCR Register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMIE	Compare match interrupt enable bit	0: Compare match interrupt disabled 1: Compare match interrupt enabled	R/W
b1	OVIE	Overflow interrupt enable bit	0: Overflow interrupt disabled 1: Overflow interrupt enabled	R/W
b2	SEIE	Set to 0 in output compare mode.		R/W
b3	MNIE			R/W
b4	HRIE			R/W
b5	DYIE			R/W
b6	MOIE			R/W
b7	YRIE			R/W

Write to this register when the RUN bit in the TRHCR register is 0 (count stops).

19.3.7 Timer RH Protect Register (TRHPRC) in Output Compare Mode

Address 011Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PROTECT	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0
After Reset by RTCRST Bit in TRHCR Register	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	PROTECT	Protect bit	Write to TRHMIN register enabled/disabled 0: Write disabled 1: Write enabled	R/W

PROTECT Bit (Protect Bit)

TRHMIN register can be changed when this bit is set to 1 (write enabled):
When writing 1 to this bit by a program, this bit stays 1. Change the registers protected by this bit as follows:
(1) Write 1 to this bit.
(2) Write a value to the register protected by this bit.
(3) Write 0 (write disabled) to this bit.

19.3.8 Operating Example

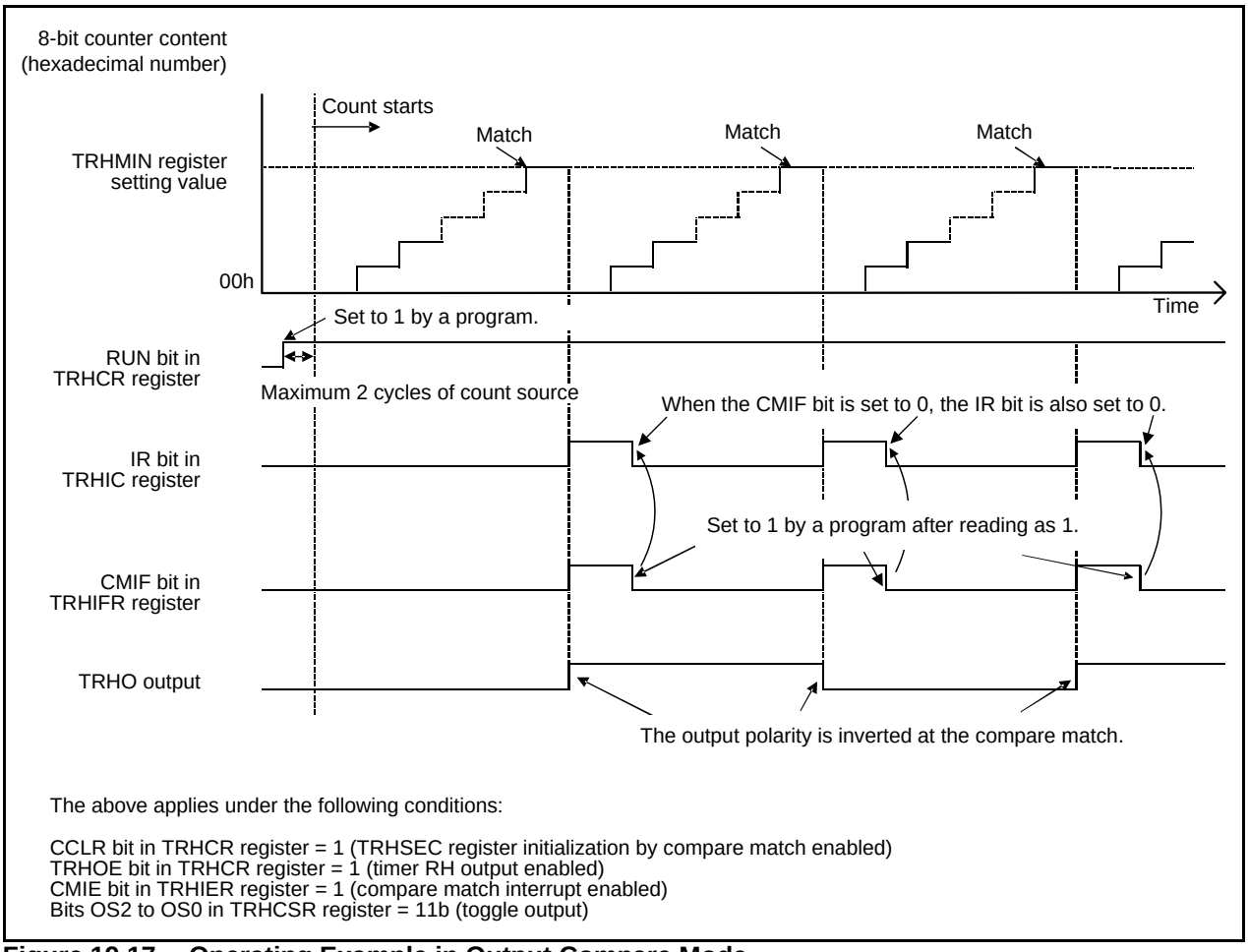

8-bit counter content
(hexadecimal number)
Count starts
Match
Match
Match
TRHMIN register
setting value
00h
Time
Set to 1 by a program.
RUN bit in
TRHCR register
Maximum 2 cycles of count source
When the CMIF bit is set to 0, the IR bit is also set to 0.
IR bit in
TRHIC register
Set to 1 by a program after reading as 1.
CMIF bit in
TRHIFR register
TRHO output
The output polarity is inverted at the compare match.
The above applies under the following conditions:
CCLR bit in TRHCR register = 1 (TRHSEC register initialization by compare match enabled)
TRHOE bit in TRHCR register = 1 (timer RH output enabled)
CMIE bit in TRHIER register = 1 (compare match interrupt enabled)
Bits OS2 to OS0 in TRHCSR register = 11b (toggle output)

Figure 19.17 Operating Example in Output Compare Mode

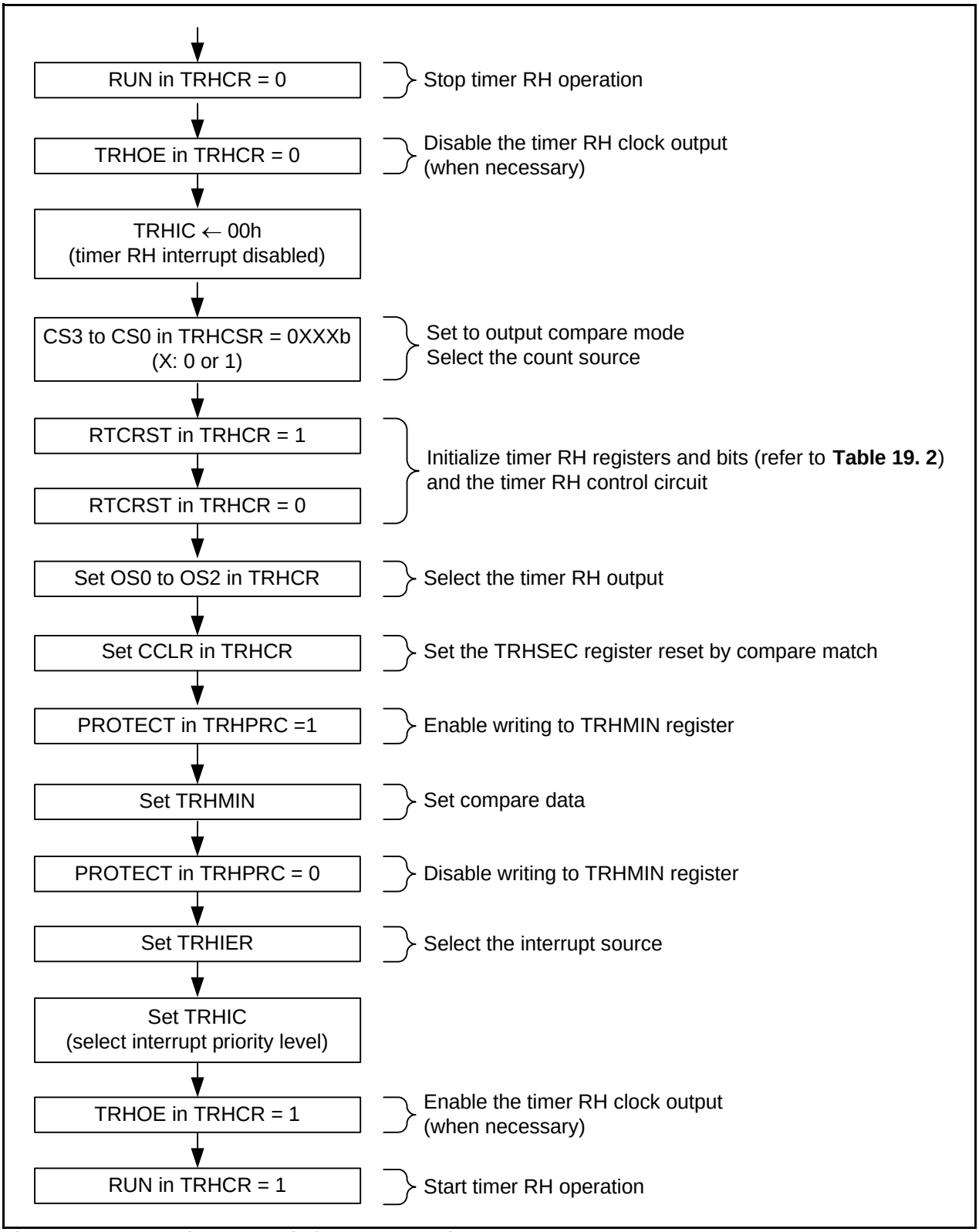

RUN in TRHCR = 0
Stop timer RH operation
TRHOE in TRHCR = 0
Disable the timer RH clock output (when necessary)
TRHIC ← 00h (timer RH interrupt disabled)
CS3 to CS0 in TRHCSR = 0XXXb (X: 0 or 1)
Set to output compare mode
Select the count source
RTCRST in TRHCR = 1
RTCRST in TRHCR = 0
Initialize timer RH registers and bits (refer to Table 19. 2) and the timer RH control circuit
Set OS0 to OS2 in TRHCR
Select the timer RH output
Set CCLR in TRHCR
Set the TRHSEC register reset by compare match
PROTECT in TRHPRC =1
Enable writing to TRHMIN register
Set TRHMIN
Set compare data
PROTECT in TRHPRC = 0
Disable writing to TRHMIN register
Set TRHIER
Select the interrupt source
Set TRHIC (select interrupt priority level)
TRHOE in TRHCR = 1
Enable the timer RH clock output (when necessary)
RUN in TRHCR = 1
Start timer RH operation

Figure 19.18 Setting Example in Output Mode

19.4 Notes on Timer RH

19.4.1 Reset

A reset input does not reset the timer RH registers that store data of seconds, minutes, hours, days of the week, dates, months, years, 12-hour/24-hour operating mode, a.m./p.m., alarms, interrupts, error correction. This requires the initial setting of all registers after power on.

19.4.2 Starting and Stopping Count

Timer RH uses the RUN bit in the TRHCR register to instruct the count to start or stop.
When the RUN bit is set to 1 (count starts), timer RH starts counting. It takes the time for up to two cycles of the count source until the 15-bit counter starts counting. During this time, do not access registers associated with timer RH (1).
Similarly, when the RUN bit is set to 0 (count stops), timer RH stops counting. It takes the time for up to two cycles of the count source until the 15-bit counter stops counting. During this time, do not access registers associated with timer RH (1).

Note:
1. Registers associated with timer RH: MSTCR1, TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, TRHYR, TRHCR, TRHCSR, TRHADJ, TRHIFR, TRHIER, TRHAMIN, TRHAHR, TRHWK, TRHPRC, and TRHICR

19.4.3 Register Setting

Write to the following registers or bits when the RUN bit in the TRHCR register is set to 0 (count stops).
- Timer TRH data registers (1)
- The TRHIER register
- Bits TRHOE, HR24, PM, and CCLR in the TRHCR register
- Bits CS0 to CS3 and OS0 to OS2 in the TRHCSR register

Set the TRHIER register after setting other registers and bits mentioned above (immediately before timer RH count starts).
Figure 19.5 shows a Setting Example in Real-Time Clock Mode.

Note:
1. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR

19.4.4 Time Reading Procedure in Real-Time Clock Mode

In real-time clock mode, read timer RH data registers (1) and bits HR24 and PM in the TRHCR register when the BSY bit in the TRHSEC is set to 0 (not while data is updated).
When reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.
In order to prevent this, use the reading procedure shown below:

- Using an interrupt
  Read necessary contents of timer RH data registers (1) and bits HR24 and PM in the TRHCR register in the timer RH interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TRHIC register with a program and read necessary contents of timer RH data registers (1) and bits HR24 and PM in the TRHCR register after the IR bit is set to 1 (timer RH interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after it is set to 1 (approximately 15.6 ms while the BSY bit is 1).
(3) Read necessary contents of timer RH data registers (1) and bits HR24 and PM in the TRHCR register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of timer RH data registers (1) and bits HR24 and PM in the TRHCR register
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match the previous contents.

Also, when reading several registers, read them as continuously as possible.

Note:
1. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR

20. Timer RJ

Note

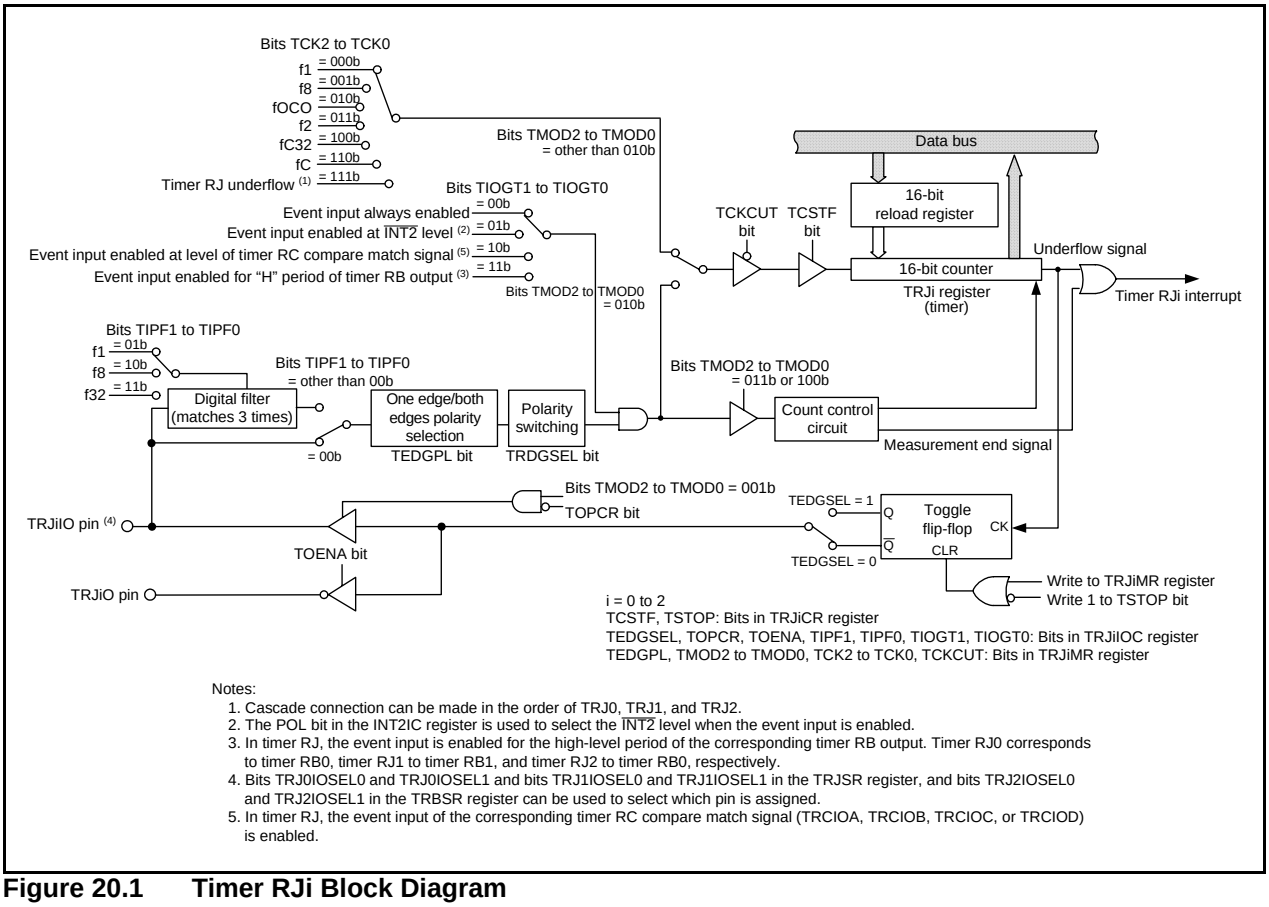
The description offered in this chapter is based on the R8C/LA8A Group.
For other groups, refer to 1.1.2 Differences between Groups.

20.1 Introduction

Timer RJ has three timers (RJ0, RJ1, and RJ2).
Timer RJ0, timer RJ1, and timer RJ2 are 16-bit timers.
Timer RJ has three 16-bit timers (timer RJ0, timer RJ1, and timer RJ2).
Timer RJi (i = 0 to 2) has two input and output pins.
The timers each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing the TRJi register (refer to **Tables 20.2 to 20.6** for details of the specifications of each mode).
The count source for timer RJ is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 20.1 shows the Timer RJi Block Diagram. Table 20.1 lists the Timer RJi Pin Configuration.

Timer RJi supports the following five operating modes:

- Timer mode: The timer counts an internal count source.
- Pulse output mode: The timer counts an internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.


Bits TCK2 to TCK0
f1 = 000b
f8 = 001b
fOCO = 010b
f2 = 011b
fC32 = 100b
fC = 110b
Timer RJ underflow (1) = 111b
Bits TMOD2 to TMOD0 = other than 010b
Bits TIOGT1 to TIOGT0
Event input always enabled = 00b
Event input enabled at INT2 level (2) = 01b
Event input enabled at level of timer RC compare match signal (5) = 10b
Event input enabled for "H" period of timer RB output (3) = 11b
Bits TMOD2 to TMOD0 = 010b
Data bus
TCKCUT bit
TCSTF bit
16-bit reload register
16-bit counter
TRJi register (timer)
Underflow signal
Timer RJi interrupt
Bits TIPF1 to TIPF0
f1 = 01b
f8 = 10b
f32 = 11b
Bits TIPF1 to TIPF0 = other than 00b
Digital filter (matches 3 times)
One edge/both edges polarity selection
= 00b
TEDGPL bit
Polarity switching
TRDGSEL bit
Bits TMOD2 to TMOD0 = 011b or 100b
Count control circuit
Measurement end signal
Bits TMOD2 to TMOD0 = 001b
TOPCR bit
TEDGSEL = 1
TEDGSEL = 0
Toggle flip-flop
Q
Q
CK
CLR
TRJiIO pin (4)
TOENA bit
TRJiO pin
Write to TRJiMR register
Write 1 to TSTOP bit
i = 0 to 2
TCSTF, TSTOP: Bits in TRJiCR register
TEDGSEL, TOPCR, TOENA, TIPF1, TIPF0, TIOGT1, TIOGT0: Bits in TRJiIOC register
TEDGPL, TMOD2 to TMOD0, TCK2 to TCK0, TCKCUT: Bits in TRJiMR register

Notes:
1. Cascade connection can be made in the order of TRJ0, TRJ1, and TRJ2.
2. The POL bit in the INT2IC register is used to select the INT2 level when the event input is enabled.
3. In timer RJ, the event input is enabled for the high-level period of the corresponding timer RB output. Timer RJ0 corresponds to timer RB0, timer RJ1 to timer RB1, and timer RJ2 to timer RB0, respectively.
4. Bits TRJ0IOSEL0 and TRJ0IOSEL1 and bits TRJ1IOSEL0 and TRJ1IOSEL1 in the TRJSR register, and bits TRJ2IOSEL0 and TRJ2IOSEL1 in the TRBSR register can be used to select which pin is assigned.
5. In timer RJ, the event input of the corresponding timer RC compare match signal (TRCIOA, TRCIOB, TRCIOC, or TRCIOD) is enabled.

Figure 20.1 Timer RJi Block Diagram

Table 20.1 Timer RJi Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRJ0IO	P6_2, P8_3	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRJ0O	P7_2	Output	
TRJ1IO	P6_1, P8_2	I/O	
TRJ1O	P7_1	Output	
TRJ2IO	P6_0	I/O	
TRJ2O	P7_0	Output	

20.2 Registers

20.2.1 Module Standby Control Register 1 (MSTCR1)

Address 0010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRJ2	MSTTRJ1	MSTTRJ0	MSTTRH	MSTTRB1	MSTTRB0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRB0	Timer RB0 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB1	Timer RB1 standby bit	0: Active 1: Standby (2)	R/W
b2	MSTTRH	Timer RH standby bit	0: Active 1: Standby (3)	R/W
b3	MSTTRJ0	Timer RJ0 standby bit	0: Active 1: Standby (4)	R/W
b4	MSTTRJ1	Timer RJ1 standby bit	0: Active 1: Standby (5)	R/W
b5	MSTTRJ2	Timer RJ2 standby bit	0: Active 1: Standby (6)	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. When the MSTTRB0 bit is set to 1 (standby), any access to the timer RB0 associated registers (addresses 0108h to 010Eh) is disabled.
2. When the MSTTRB1 bit is set to 1 (standby), any access to the timer RB1 associated registers (addresses 0098h to 009Eh) is disabled.
3. When the MSTTRH bit is set to 1 (standby), any access to the timer RH associated registers (addresses 0110h to 011Fh) is disabled.
4. When the MSTTRJ0 bit is set to 1 (standby), any access to the timer RJ0 associated registers (addresses 0080h to 0086h) is disabled.
5. When the MSTTRJ1 bit is set to 1 (standby), any access to the timer RJ1 associated registers (addresses 0088h to 008Eh) is disabled.
6. When the MSTTRJ2 bit is set to 1 (standby), any access to the timer RJ2 associated registers (addresses 0090h to 0096h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

20.2.2 Timer RJi Control Register (TRJiCR) (i = 0 to 2)

Address 0080h (TRJ0CR), 0088h (TRJ1CR), 0090h (TRJ2CR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RJi count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RJi count status flag (1)	0: Count stops 1: During count operation	R
b2	TSTOP	Timer RJi count forcible stop bit (2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TEDGF	Active edge judgment flag (3, 4)	0: Active edge not received 1: Active edge received (end of measurement period)	R/W
b5	TUNDF	Timer RJi underflow flag (3, 4)	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Refer to **20.8 Notes on Timer RJ** for notes regarding bits TSTART and TCSTF.
2. When 1 is written to the TSTOP bit, bits TSTART and TCSTF and the TRJi register are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. Set to 0 in timer mode, pulse output mode, and event counter mode.

In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRJiCR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.

20.2.3 Timer RJi I/O Control Register (TRJiIOC) (i = 0 to 2)

Address 0081h (TRJ0IOC), 0089h (TRJ1IOC), 0091h (TRJ2IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJiIO polarity switch bit	Function varies according to the operating mode.	R/W
b1	TOPCR	TRJiIO output control bit		R/W
b2	TOENA	TRJiO output enable bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJiIO input filter select bit	Function varies according to the operating mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJiIO event input control bit		R/W
b7	TIOGT1			R/W

20.2.4 Timer RJi Mode Register (TRJiMR) (i = 0 to 2)

Address 0082h (TRJ0MR), 008Ah (TRJ1MR), 0092h (TRJ2MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RJi operating mode select bit	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	TEDGPL	TRJiO input polarity select bit	0: One edge 1: Both edges (1)	R/W
b4	TCK0	Timer RJi count source select bit (2)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fOCO 0 1 1: f2 1 0 0: fC32 1 0 1: Do not set. 1 1 0: fC 1 1 1: Timer RJ0 underflow (TRJ1MR register) Timer RJ1 underflow (TRJ2MR register)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RJi count source cut off bit	0: Count source provided 1: Count source cut off	R/W

Notes:
1. When setting the TEDGPL bit to 1 (both edges), set the TEDGSEL bit in the TRJiIOC register to 0 (count on rising edge). The setting of both edges can be used only in event counter mode.
2. Do not set bits TCK2 to TCK0 in the TRJ0MR register to 111b.

When both the TSTART and TCSTF bits in the TRJiCR register are set to 0 (count stops), rewrite the TRJiMR register.

20.2.5 Timer RJi Event Pin Select Register (TRJiISR) (i = 0 to 2)

Address 0083h (TRJ0ISR), 008Bh (TRJ1ISR), 0093h (TRJ2ISR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	RCCPSEL2	RCCPSEL1	RCCPSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCCPSEL0	Timer RC compare input event select bit (1)	b1 b0 0 0: TRCIOD output used 0 1: TRCIOC output used 1 0: TRCIOB output used 1 1: TRCIOA output used	R/W
b1	RCCPSEL1			R/W
b2	RCCPSEL2	Timer RC compare event invert bit	0: Low-level period of the compare match signal is counted 1: High-level period of the compare match signal is counted	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. Bits RCCPSEL0 and RCCPSEL1 in the TRJiISR register are used to select the compare output from timer RC.

20.2.6 Timer RJi Register (TRJi) (i = 0 to 2)

Address 0084h to 0085h (TRJ0), 008Ch to 008Dh (TRJ1), 0094h to 0095h (TRJ2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	b15	b14	b13	b12	b11	b10	b9	b8	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b15 to b0	Timer mode	Counts an internal count source.	0000h to FFFFh	R/W
	Pulse output mode		0000h to FFFFh	R/W
	Event counter mode	Counts an external count source.	0000h to FFFFh	R/W
	Pulse width measurement mode	Measures the pulse width of input pulses from external (counts an internal count source).	0001h to FFFFh (3)	R/W
	Pulse period measurement mode	Measures the pulse period of input pulses from external (counts an internal count source).	0001h to FFFFh (3)	R/W

Notes:
1. When 1 is written to the TSTOP bit in the TRJiCR register, the TRJi register is set to FFFFh.
2. Access the TRJi register in 16-bit units. Do not access this register in 8-bit units.
3. Do not set 0000h in pulse width measurement mode and pulse period measurement mode.

20.2.7 Timer RJ Pin Select Register (TRJSR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRJ1IOSEL1	TRJ1IOSEL0	—	—	TRJ0IOSEL1	TRJ0IOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJ0IOSEL0	TRJ0IO pin select bit	b1 b0 0 0: TRJ0IO pin not used 0 1: P6_2 assigned 1 0: P8_3 assigned 1 1: Do not set.	R/W
b1	TRJ0IOSEL1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	TRJ1IOSEL0	TRJ1IO pin select bit	b5 b4 0 0: TRJ1IO pin not used 0 1: P6_1 assigned 1 0: P8_2 assigned 1 1: Do not set.	R/W
b5	TRJ1IOSEL1			R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

To use the I/O pins for timer RJi, set the TRJSR register.
Set this register before setting the timer RJi associated registers. Also, do not change the setting value of this register during timer RJi operation.

20.2.8 Timer RB Pin Select Register (TRBSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRB1OSEL1	TRB1OSEL0	TRB0OSEL1	TRB0OSEL0	—	—	TRJ2IOSEL1	TRJ2IOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJ2IOSEL0	TRJ2IO pin select bit	b1 b0 0 0: TRJ2IO pin not used 0 1: P6_0 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b1	TRJ2IOSEL1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	TRB0OSEL0	TRB0O pin select bit	b5 b4 0 0: P8_7 assigned 0 1: P7_6 assigned 1 0: P6_6 assigned 1 1: Do not set.	R/W
b5	TRB0OSEL1			R/W
b6	TRB1OSEL0	TRB1O pin select bit	b7 b6 0 0: P7_5 assigned 0 1: P6_5 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b7	TRB1OSEL1			R/W

To use the output pins for timer RJi, set the TRBSR register.
Set this register before setting the timer RJi associated registers. Also, do not change the setting value of this register during timer RJi operation.

20.3 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 20.2**).

Table 20.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC, timer RJ0 underflow for timer RJ1, timer RJ1 underflow for timer RJ2 (1)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(m+1) m: Value set in TRJi register
Count start condition	1 (count starts) is written to the TSTART bit in the TRJiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRJiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJiCR register.
Interrupt request generation timing	When timer RJi underflows [timer RJi interrupt].
TRJiIO pin function	Programmable I/O port
TRJiO pin function	Programmable I/O port
Read from timer	The count value can be read out by reading the TRJi register.
Write to timer	• When the TRJi register is written while the count is stopped, values written to both the reload register and counter. • When the TRJi register is written during count operation, values are written to the reload register and counter (refer to **20.3.2 Timer Write Control during Count Operation**).

Note:
1. Underflow cannot be selected for timer RJ0.

i = 0 to 2

20.3.1 Timer RJi I/O Control Register (TRJiIOC) (i = 0 to 2) in Timer Mode

Address 0081h (TRJ0IOC), 0089h (TRJ1IOC), 0091h (TRJ2IOC)

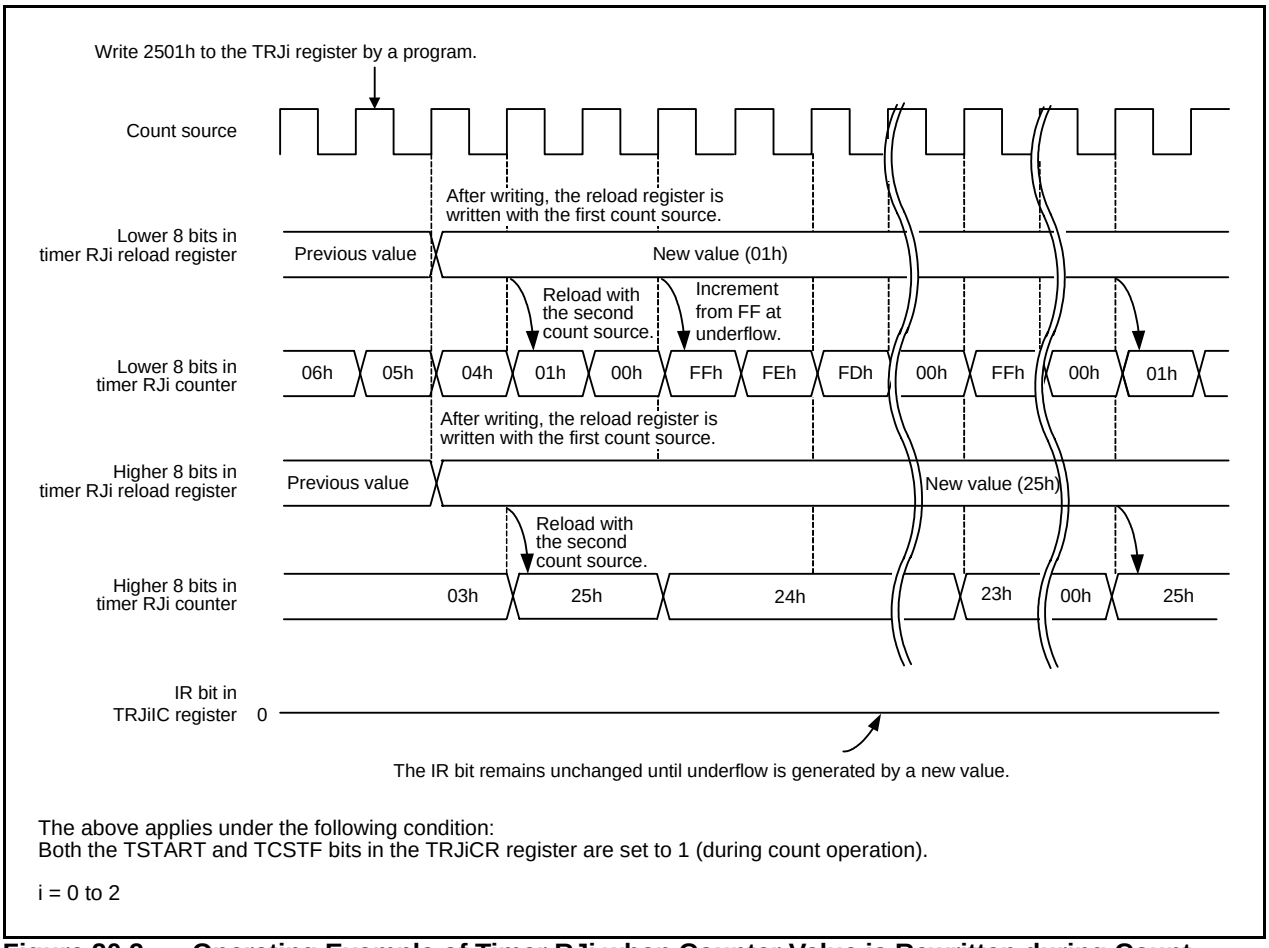
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJiIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRJiIO output control bit		R/W
b2	TOENA	TRJiO output enable bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJiIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJiIO event input control bit		R/W
b7	TIOGT1			R/W

20.3.2 Timer Write Control during Count Operation

Timer RJi has a reload register and a counter. When writing to the timer, values are written to both the reload register and counter.

Figure 20.2 shows an Operating Example of Timer RJi when Counter Value is Rewritten during Count Operation.



The above applies under the following condition:
Both the TSTART and TCSTF bits in the TRJiCR register are set to 1 (during count operation).

i = 0 to 2

Figure 20.2 Operating Example of Timer RJi when Counter Value is Rewritten during Count Operation

20.4 Pulse Output Mode

In pulse output mode, an internally generated count source is counted, and a pulse with inverted polarity is output from the TRJiIO pin each time the timer underflows (refer to **Table 20.3**).

Table 20.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC, timer RJ0 underflow for timer RJ1, timer RJ1 underflow for timer RJ2 (1)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(m+1) m: Value set in TRJi register
Count start condition	1 (count starts) is written to the TSTART bit in the TRJiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRJiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJiCR register.
Interrupt request generation timing	When timer RJi underflows [timer RJi interrupt].
TRJiIO pin function	Pulse output or programmable output port
TRJiO pin function	Programmable I/O port or inverted output of TRJiIO output
Read from timer	The count value can be read out by reading the TRJi register.
Write to timer	• When the TRJi register is written while the count is stopped, values are written to both the reload register and counter. • When the TRJi register is written during count operation, values are written to the reload register and counter (refer to **20.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRJiIO output polarity switch function The level when the pulse output starts is selected by the TEDGSEL bit in the TRJiIOC register. (2) • TRJiO output function Pulses inverted from the TRJiIO output polarity can be output from the TRJiO pin (selected by the TOENA bit in the TRJiIOC register). • Pulse output stop function Output from the TRJiIO pin is stopped by the TOPCR bit in the TRJiIOC register. • TRJiIO pin select function Use of the TRJiIO pin is selected by bits TRJiIOSEL0 and TRJiIOSEL1 in the TRJSR register.

Notes:
1. Underflow cannot be selected for timer RJ0.
2. By writing to the TRJiMR register, the output pulse is set to the level when the pulse output starts.

i = 0 to 2

20.4.1 Timer RJi I/O Control Register (TRJiIOC) (i = 0 to 2) in Pulse Output Mode

Address 0081h (TRJ0IOC), 0089h (TRJ1IOC), 0091h (TRJ2IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJiIO polarity switch bit	0: TRJiIO output starts at high 1: TRJiIO output starts at low	R/W
b1	TOPCR	TRJiIO output control bit	0: TRJiIO output 1: I/O port	R/W
b2	TOENA	TRJiO output enable bit	0: TRJiO output disabled 1: TRJiO output enabled (inverted TRJiIO output is output from each port)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJiIO input filter select bit	Set to 0 in pulse output mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJiIO event input control bit		R/W
b7	TIOGT1			R/W

20.5 Event Counter Mode

In event counter mode, external signal inputs to the TRJiIO pin are counted (refer to **Table 20.4**).

Table 20.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal input to the TRJiIO pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Division ratio	1/(m+1) m: Value set in TRJi register
Count start condition	1 (count starts) is written to the TSTART bit in the TRJiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRJiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJiCR register.
Interrupt request generation timing	When timer RJi underflows [timer RJi interrupt].
TRJiIO pin function	Count source input
TRJiO pin function	Programmable I/O port or pulse output (1)
Read from timer	The count value can be read out by reading the TRJi register.
Write to timer	• When the TRJi register is written while the count is stopped, values are written to both the reload register and counter. • When the TRJi register is written during count operation, values are written to the reload register and counter (refer to **20.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRJiIO input polarity switch function The active edge of the count source is selected by the TEDGSEL bit in the TRJiIOC register. • Count source input pin select function Use of the TRJiIO pin is selected by bits TRJiIOSEL0 and TRJiIOSEL1 in the TRJSR register. • Pulse output function Pulses of inverted polarity can be output from the TRJiO pin each time the timer underflows (selected by the TOENA bit in the TRJiIOC register). (1) • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRJiIOC register. • Event input control function The enabled period for the event input to the TRJiIO pin is selected by bits TIOGT0 and TIOGT1 in the TRJiIOC register.

Note:
1. By writing to the TRJiMR register, the output pulse is set to the level when the pulse output starts.

i = 0 to 2

20.5.1 Timer RJi I/O Control Register (TRJiIOC) (i = 0 to 2) in Event Counter Mode

Address 0081h (TRJ0IOC), 0089h (TRJ1IOC), 0091h (TRJ2IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJiIO polarity switch bit (1)	0: Count at the rising edge of TRJiIO input and TRJiO output starts at low 1: Count at the falling edge of TRJiIO input and TRJiO output starts at high	R/W
b1	TOPCR	TRJiIO output control bit	Set to 0 in event counter mode.	R/W
b2	TOENA	TRJiO output enable bit	0: TRJiO output disabled 1: TRJiO output enabled	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJiIO input filter select bit (2)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJiIO event input control bit	b7 b6 0 0: Event input always enabled 0 1: Event input enabled at $\overline{\text{INT2}}$ level (3) 1 0: Event input enabled at level of timer RC compare match signal (5) 1 1: Event input enabled for high-level period of timer RB output (4)	R/W
b7	TIOGT1			R/W

Notes:
1. Do not change the setting value of the TEDGSEL bit during count operation.
2. When the same value from the TRJiIO pin is sampled three times continuously, the input is determined.
3. Set the INT2PL bit in the INTEN register to 0 (one edge).
   When the POL bit in the INT2IC register is set to 0 (falling edge selected), the event input for the $\overline{\text{INT2}}$ high-level period is enabled. When the POL bit is set to 1 (rising edge selected), the event input for the $\overline{\text{INT2}}$ low-level period is enabled.
4. In timer RJ, the event input is enabled for the high-level period of the corresponding timer RB output. Timer RJ0 corresponds to timer RB0, timer RJ1 to timer RB1, and timer RJ2 to timer RB0, respectively.
5. In timer RJ, the event input of the corresponding timer RC compare match signal (TRCIOA, TRCIOB, TRCIOC, or TRCIOD) is enabled. Bits RCCPSEL0 and RCCPSEL1 in the TRJiISR register can be used to select the compare output from timer RC, and the RCCPSEL2 bit can be used to select the level of the timer RC compare match signal.

20.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the TRJiIO pin is measured (refer to **Table 20.5**).

Figure 20.3 shows an Operating Example in Pulse Width Measurement Mode.

Table 20.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, f32, fC, timer RJ0 underflow for timer RJ1, timer RJ1 underflow for timer RJ2 (1)
Count operations	• Decrement • The count is continued only while the measured pulse is high or low level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRJiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRJiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJiCR register.
Interrupt request generation timing	• When timer RJi underflows [timer RJi interrupt]. • Rising or falling of the TRJiIO input (end of measurement period) [timer RJi interrupt]
TRJiIO pin function	Measured pulse input
TRJiO pin function	Programmable I/O port
Read from timer	The count value can be read out by reading the TRJi register.
Write to timer	• When the TRJi register is written while the count is stopped, values are written to both the reload register and counter. • When the TRJi register is written during count operation, values are written to the reload register and counter (refer to **20.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement level setting A high-level or low-level period is selected by the TEDGSEL bit in the TRJiIOC register. • Measured pulse input pin select function Use of the TRJiIO pin is selected by bits TRJiIOSEL0 and TRJiIOSEL1 in the TRJSR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRJiIOC register.

Note:
1. Underflow cannot be selected for timer RJ0.

i = 0 to 2

20.6.1 Timer RJi I/O Control Register (TRJiIOC) (i = 0 to 2) in Pulse Width Measurement Mode

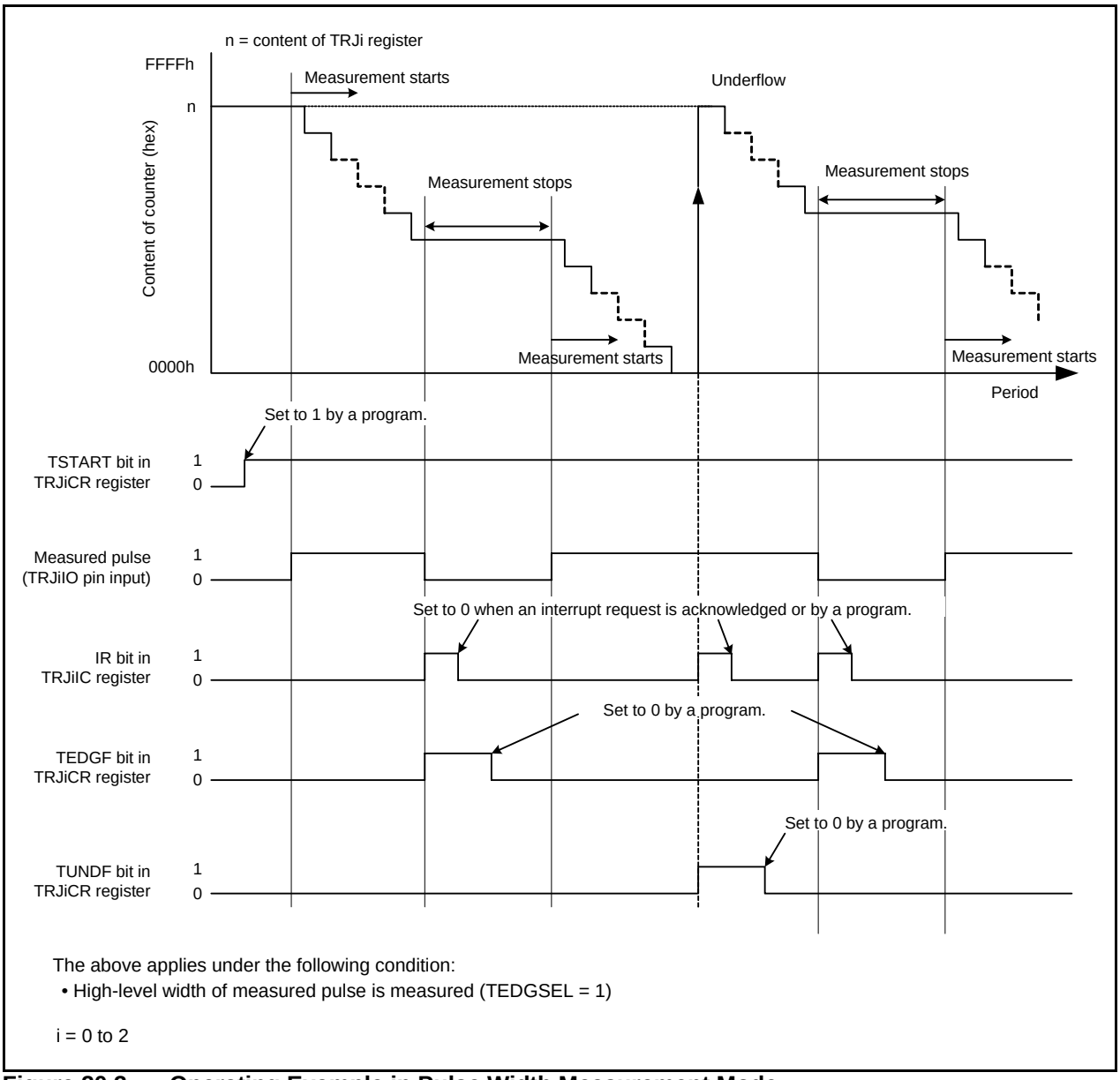
Address 0081h (TRJ0IOC), 0089h (TRJ1IOC), 0091h (TRJ2IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJiIO polarity switch bit	0: Low-level width of TRJiIO input is measured 1: High-level width of TRJiIO input is measured	R/W
b1	TOPCR	TRJiIO output control bit	Set to 0 in pulse width measurement mode.	R/W
b2	TOENA	TRJiO output enable bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJiIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJiIO event input control bit	Set to 0 in pulse width measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRJiIO pin is sampled three times continuously, the input is determined.

20.6.2 Operating Example



The above applies under the following condition:
- High-level width of measured pulse is measured (TEDGSEL = 1)

i = 0 to 2

Figure 20.3 Operating Example in Pulse Width Measurement Mode

20.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the TRJiIO pin is measured (refer to **Table 20.6**).

Figure 20.4 shows an Operating Example in Pulse Period Measurement Mode.

Table 20.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC, timer RJ0 underflow for timer RJ1, timer RJ1 underflow for timer RJ2 (1)
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RJi. Then timer RJi reloads the contents of the reload register at the second underflow and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRJiCR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRJiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJiCR register.
Interrupt request generation timing	• When timer RJi underflows or reloads [timer RJi interrupt]. • Rising or falling of the TRJiIO input (end of measurement period) [timer RJi interrupt]
TRJiIO pin function	Measured pulse input
TRJiO pin function	Programmable I/O port
Read from timer	The count value can be read out by reading the TRJi register.
Write to timer	• When the TRJi register is written while the count is stopped, values are written to both the reload register and counter. • When the TRJi register is written during count operation, values are written to the reload register and counter (refer to **20.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement period selection The measurement period of the input pulse is selected by the TEDGSEL bit in the TRJiIOC register. • Measured pulse input pin select function Use of the TRJiIO pin is selected by bits TRJiIOSEL0 and TRJiIOSEL1 in the TRJSR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRJiIOC register.

Note:
1. Underflow cannot be selected for timer RJ0.

i = 0 to 2

20.7.1 Timer RJi I/O Control Register (TRJiIOC) (i = 0 to 2) in Pulse Period Measurement Mode

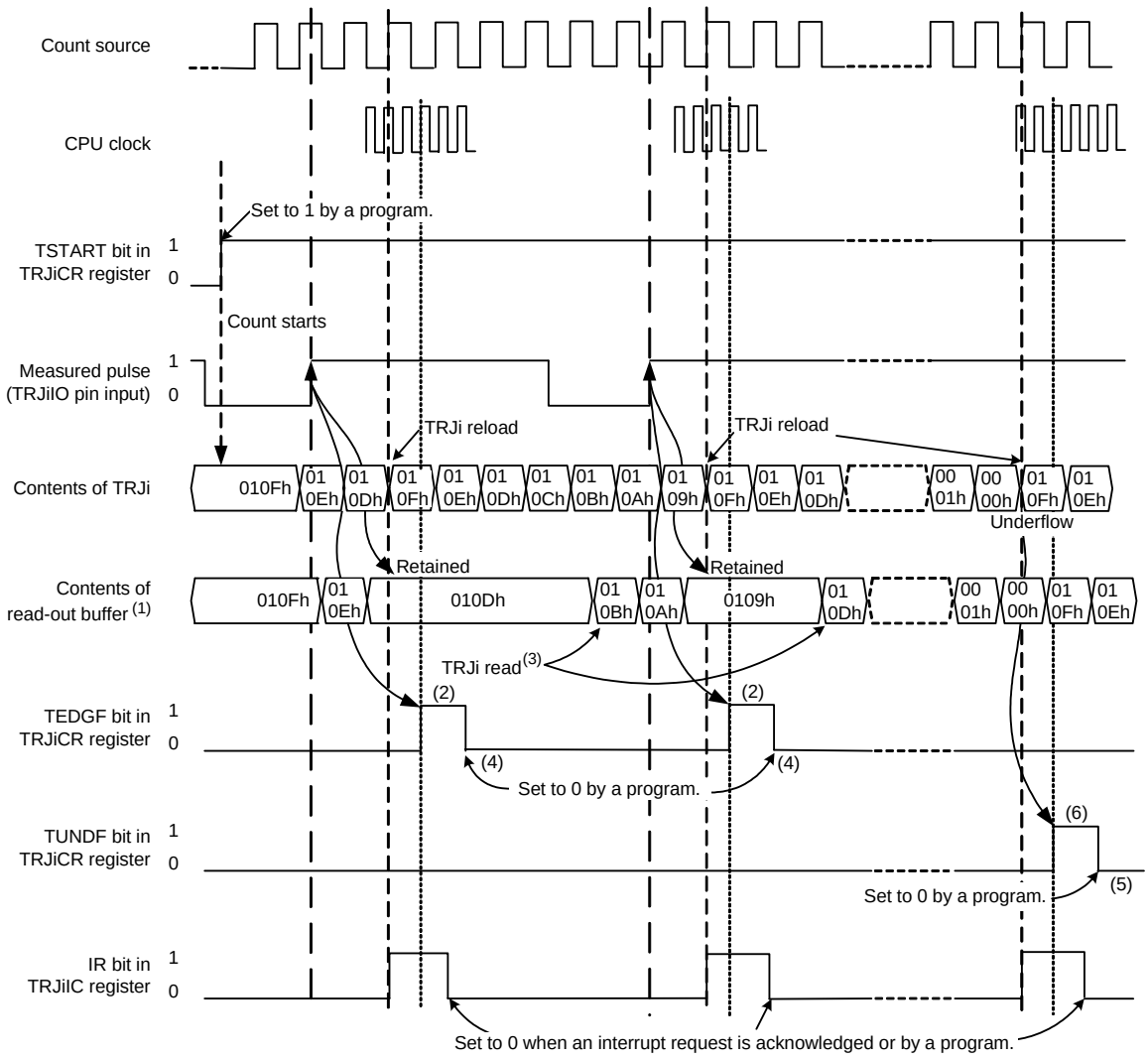
Address 0081h (TRJ0IOC), 0089h (TRJ1IOC), 0091h (TRJ2IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRJiIO polarity switch bit	0: Period from one rising edge to next rising edge of measured pulse is measured 1: Period from one falling edge to next falling edge of measured pulse is measured	R/W
b1	TOPCR	TRJiIO output control bit	Set to 0 in pulse period measurement mode.	R/W
b2	TOENA	TRJiO output enable bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TIPF0	TRJiIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJiIO event input control bit	Set to 0 in pulse period measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRJiIO pin is sampled three times continuously, the input is determined.

20.7.2 Operating Example



The above applies when the initial value in the TRJi register is set to 010Fh and the period from one rising edge to the next rising edge of the measurement pulse is measured (TEDGSEL = 0).

Notes:
1. The content of the read-out buffer can be read by reading the TRJi register in pulse period measurement mode.
2. After the active edge of the measurement pulse is input, a TRJi reload occurs at the second rising edge of the count source. Then the TEDGF bit in the TRJiCR register is set to 1 (active edge received) at the second rising edge of the CPU clock.
3. The TRJi register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge received). The contents of the read-out buffer are retained until the TRJi register is read. If the TRJi register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRJiCR register. At the same time, write 1 to the TUNDF bit.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit in the TRJiCR register. At the same time, write 1 to the TEDGF bit.
6. When timer RJi underflows and reloads at the input of an active edge simultaneously, bits TUNDF and TEDGF are set to 1 at the second rising edge of the system clock after the underflow. If not, the TUNDF bit is set to 1 at the second rising edge of the CPU clock after the underflow.

i = 0 to 2

Figure 20.4 Operating Example in Pulse Period Measurement Mode

20.8 Notes on Timer RJ

- Timer RJi stops counting after a reset. Set the values in the timer before the count starts.
- Read the timer in 16-bit units.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRJiCR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRJiCR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RJi underflow signal generated after the count starts.
- When using pulse period measurement mode, leave two or more periods of the timer RJi register immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit remains 0 (count stops) for zero or one cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RJi (1) other than the TCSTF bit.
  Timer RJi starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for zero or one cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RJi counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RJi (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RJi: TRJiCR, TRJiIOC, TRJiMR, and TRJi

- When the TRJi register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.

21. Serial Interface (UART0)

The serial interface consists of two channels, UART0 and UART2. This chapter describes UART0.

21.1 Introduction

UART0 has a dedicated timer to generate a transfer clock. Clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode) are supported.
Figure 21.1 shows a Block Diagram of UART0. Figure 21.2 shows a Block Diagram of UART0 Transmit/Receive Unit. Table 21.1 lists the Pin Configuration of UART0.

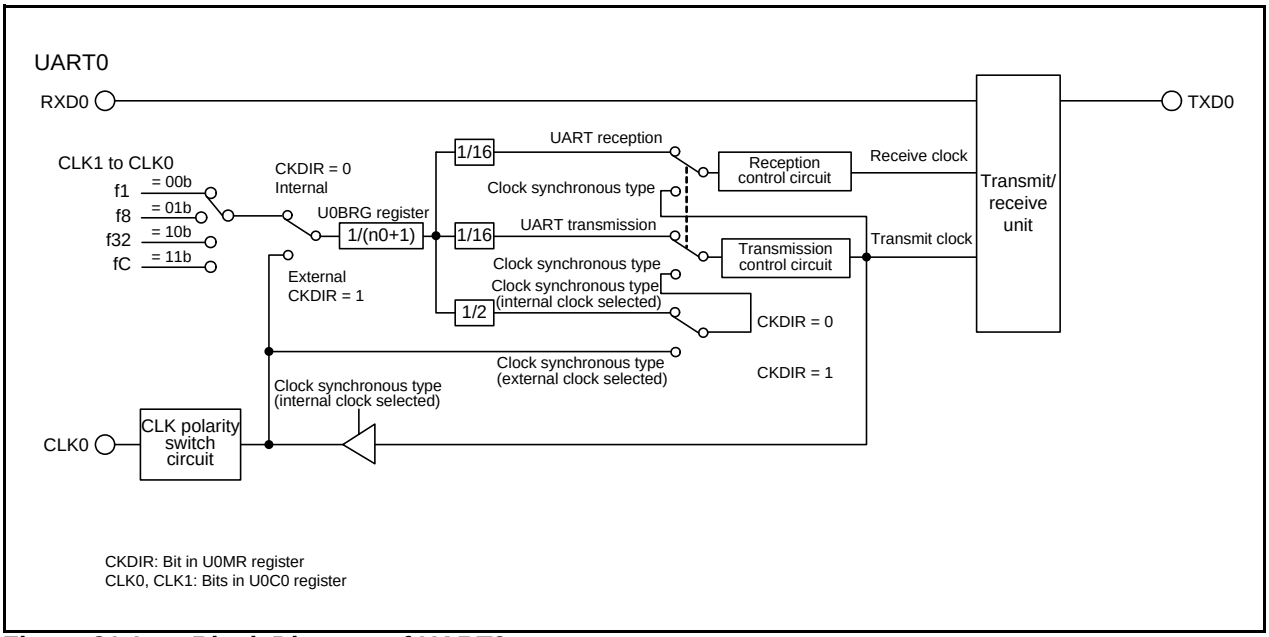


Figure 21.1 Block Diagram of UART0

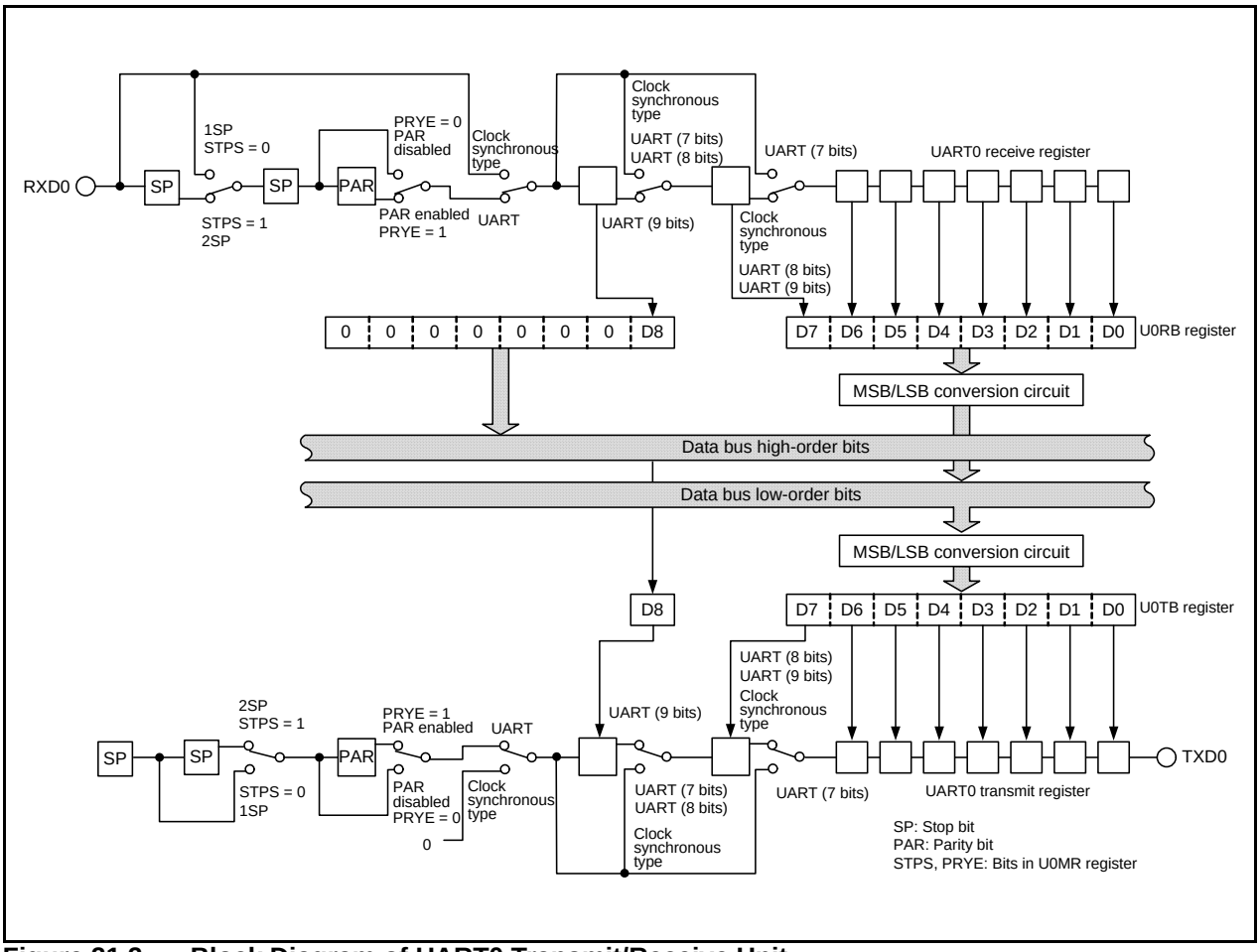


Figure 21.2 Block Diagram of UART0 Transmit/Receive Unit

Table 21.1 Pin Configuration of UART0

Pin Name	Assigned Pin	I/O	Function
TXD0	P8_5	Output	Serial data output
RXD0	P8_6	Input	Serial data input
CLK0	P8_4	I/O	Transfer clock I/O

21.2 Registers

21.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	MSTURT2	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	UART0 standby bit	0: Active 1: Standby (1)	R/W
b2	MSTURT2	UART2 standby bit	0: Active 1: Standby (2)	R/W
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (3)	R/W
b4	MSTLCD	LCD standby bit	0: Active 1: Standby (4)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (5)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	A/D standby bit (6)	0: Active 1: Standby	R/W

Notes:
1. When the MSTURT0 bit is set to 1 (standby), any access to the UART0 associated registers (addresses 00A0h to 00A7h) is disabled.
2. When the MSTURT2 bit is set to 1 (standby), any access to the timer UART2 associated registers (addresses 00A8h to 00BFh) is disabled.
3. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
4. When the MSTLCD bit is set to 1 (standby), any access to the timer LCD associated registers (addresses 0200h to 0237h) is disabled.
5. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
6. When the MSTADC bit is set to 1 (standby), any access to the timer A/D associated registers (addresses 00C0h to 00D9h, 00DCh to 00DFh) is disabled.
   Set the MSTADC bit to 0 (active) when the temperature sensor is used.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

21.2.2 UART0 Transmit/Receive Mode Register (U0MR)

Address 00A0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit (1, 2)	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. When setting bits SMD2 to SMD0 to 000b (serial interface disabled), set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. When bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode), the error flags (bits FER, PER, and SUM) in the U0RB register are disabled. When these bits are read, the values are undefined.

21.2.3 UART0 Bit Rate Register (U0BRG)

Address 00A1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U0BRG divides the count source by n+1.	00h to FFh	W

Write to the U0BRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK0 and CLK1 in the U0C0 register before writing to the U0BRG register.

21.2.4 UART0 Transmit Buffer Register (U0TB)

Address 00A3h to 00A2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data (D8 to D0)	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	—		
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

When the transfer data is 9 bits long, write data to the high-order byte first, then low-order byte of the U0TB register.
Use the MOV instruction to write to this register.

21.2.5 UART0 Transmit/Receive Control Register 0 (U0C0)

Address 00A4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	—	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: fC selected	R/W
b1	CLK1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	NCH	Data output select bit	0: TXD0 pin set as CMOS output 1: TXD0 pin set as N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Note:
1. If the BRG count source is switched, set the U0BRG register again.

21.2.6 UART0 Transmit/Receive Control Register 1 (U0C1)

Address 00A5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	U0RRM	U0IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data in the U0TB register 1: No data in the U0TB register	R
b2	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Reception complete flag (1)	0: No data in the U0RB register 1: Data in the U0RB register	R
b4	U0IRS	UART0 transmit interrupt source select bit	0: Transmit buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U0RRM	UART0 continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. The RI bit is set to 0 when the higher byte of the U0RB register is read.
2. In UART mode, set the U0RRM bit to 0 (continuous receive mode disabled).

21.2.7 UART0 Receive Buffer Register (U0RB)

Address 00A7h to 00A6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	—	—	Receive data (D8)	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Notes:
1. Bits SUM, PER, FER, and OER are set to 0 (no error) when either of the following is set:
   - Bits SMD2 to SMD0 in the U0MR register are set to 000b (serial interface disabled).
   - The RE bit in the U0C1 register is set to 0 (reception disabled).
   The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error).
   Bits PER and FER are also set to 0 when the high-order byte of the U0RB register is read.
   When setting bits SMD2 to SMD0 in the UiMR register to 000b, set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the UiMR register are set to 001b (clock synchronous serial I/O mode). When read, the content is undefined.

Always read the U0RB register in 16-bit units.

21.2.8 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK0SEL1	CLK0SEL0	RXD0SEL1	RXD0SEL0	TXD0SEL1	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	b1 b0 0 0: TXD0 pin not used 0 1: P8_5 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b1	TXD0SEL1			R/W
b2	RXD0SEL0	RXD0 pin select bit	b3 b2 0 0: RXD0 pin not used 0 1: P8_6 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b3	RXD0SEL1			R/W
b4	CLK0SEL0	CLK0 pin select bit	b5 b4 0 0: CLK0 pin not used 0 1: P8_4 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b5	CLK0SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		R/W
b7	—			R/W

The U0SR register selects which pin is assigned as the UART0 input/output. To use the I/O pins for UART0, set this register.

Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value of this register during UART0 operation.

21.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 21.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 21.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 21.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clocks	• The CKDIR bit in the U0MR register is set to 0 (internal clock): fi/(2(n+1)) fi = f1, f8, f32, fC n = Value set in U0BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLK0 pin
Transmit start conditions	• To start transmission, the following requirements must be met: (1) - The TE bit in the U0C1 register is set to 1 (transmission enabled). - The TI bit in the U0C1 register is set to 0 (data in the U0TB register).
Receive start conditions	• To start reception, the following requirements must be met: (1) - The RE bit in the U0C1 register is set to 1 (reception enabled). - The TE bit in the U0C1 register is set to 1 (transmission enabled). - The TI bit in the U0C1 register is set to 0 (data in the U0TB register).
Interrupt request generation timing	• For transmission, one of the following can be selected. - The U0IRS bit is set to 0 (transmit buffer empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit is set to 1 (transmission completed): When data transmission from the UART0 transmit register is completed. • For reception When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U0RB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock. • LSB first, MSB first selection Whether data transmission/reception begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the U0RB register.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the U0C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the U0C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register will be undefined.

Table 21.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode(1)

Register	Bit	Function
U0TB	b0 to b7	Set data transmission.
U0RB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U0BRG	b0 to b7	Set the transfer rate.
U0MR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select an internal clock or external clock.
U0C0	CLK0, CLK1	Select the count source for the U0BRG register.
	TXEPT	Transmit register empty flag
	NCH	Select the output format of the TXD0 pin.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
U0C1	TE	Set to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U0IRS	Select the UART0 transmit interrupt source.
	U0RRM	Set to 1 to use continuous receive mode.

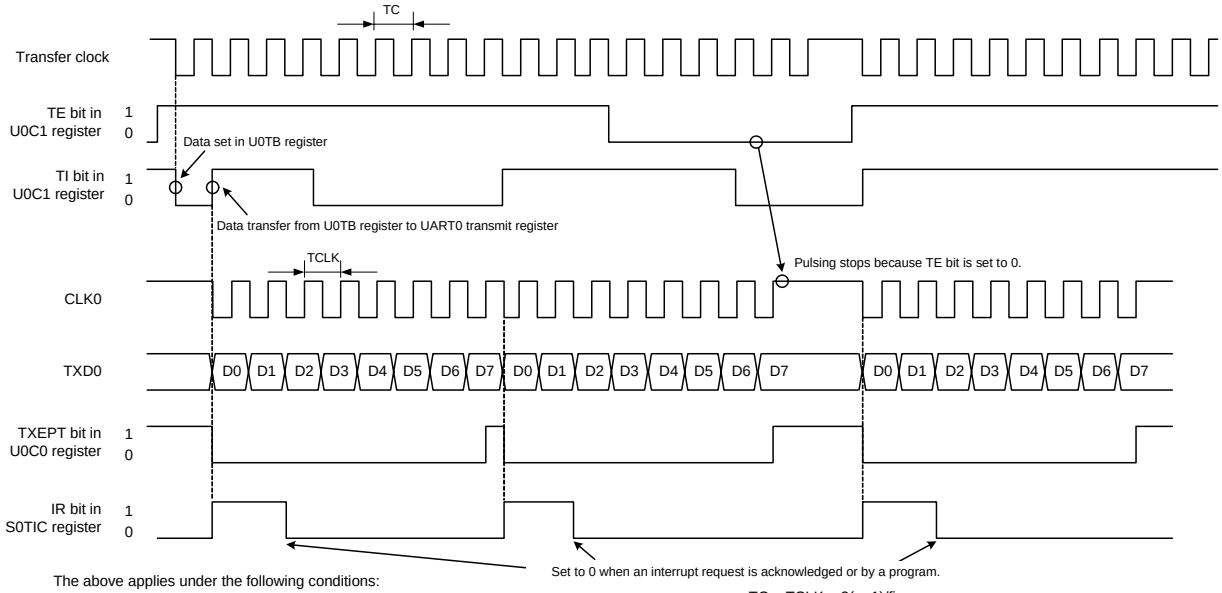
Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 21.4 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode.
After UART0 operating mode is selected, the TXD0 pin outputs a high-level signal until transfer starts. (When the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 21.4 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0 (P8_5)	Serial data output	Bits TXD0SEL1 to TXD0SEL0 in U0SR register = 01b When N-channel open-drain output is selected, PD8_5 bit in PD8 register = 0 For reception only: P8_5 can be used as a port by setting TXD0SEL1 to TXD0SEL0 bit = 00b.
RXD0 (P8_6)	Serial data input	Bits RXD0SEL1 to RXD0SEL0 in U0SR register = 01b PD8_6 bit in PD8 register = 0 For transmission only: P8_6 can be used as a port by setting bits RXD0SEL1 to RXD0SEL0 = 00b.
CLK0 (P8_4)	Transfer clock output	Bits CLK0SEL1 to CLK0SEL0 in U0SR register = 01b CKDIR bit in U0MR register = 0
	Transfer clock input	Bits CLK0SEL1 to CLK0SEL0 in U0SR register = 01b CKDIR bit in U0MR register = 1 PD8_4 bit in PD8 register = 0

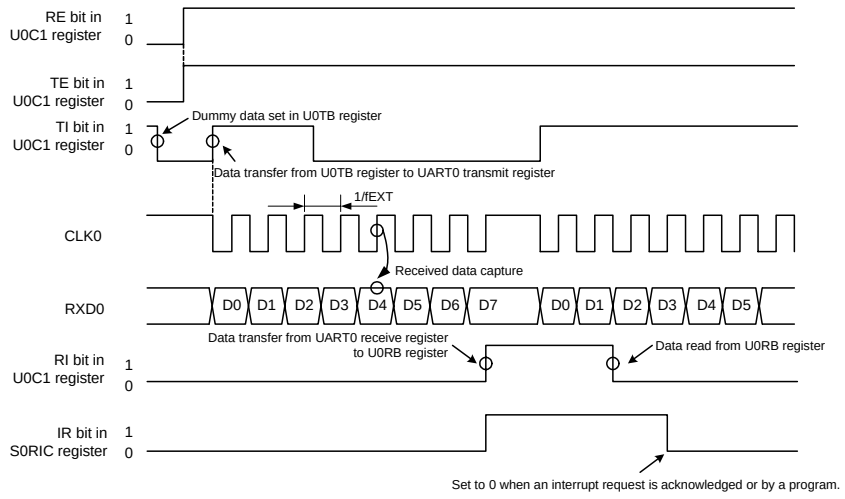
• Transmit Timing Example (Internal Clock Selected)


TC
Transfer clock
TE bit in U0C1 register
1
0
Data set in U0TB register
TI bit in U0C1 register
1
0
Data transfer from U0TB register to UART0 transmit register
TCLK
Pulsing stops because TE bit is set to 0.
CLK0
TXD0
D0 D1 D2 D3 D4 D5 D6 D7 D0 D1 D2 D3 D4 D5 D6 D7 D0 D1 D2 D3 D4 D5 D6 D7
TXEPT bit in U0C0 register
1
0
IR bit in S0TIC register
1
0
Set to 0 when an interrupt request is acknowledged or by a program.

The above applies under the following conditions:
- CKDIR bit in U0MR register = 0 (internal clock)
- CKPOL bit in U0C0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- U0IRS bit in U0C1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = TCLK = 2(n+1)/fi
fi: Frequency of U0BRG count source (f1, f8, f32, fC)
n: Value set in U0BRG register

• Receive Timing Example (External Clock Selected)



The above applies under the following conditions:
- CKDIR bit in U0MR register = 1 (external clock)
- CKPOL bit in U0C0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

The following should be met when a high-level is applied to the CLK0 pin before receiving data:
- TE bit in U0C1 register = 1 (transmission enabled)
- RE bit in U0C1 register = 1 (reception enabled)
- Dummy data write to the U0TB register

fEXT: Frequency of external clock

Figure 21.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

21.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.3.2 Polarity Select Function

Figure 21.4 shows the Transfer Clock Polarity. The CKPOL bit in the U0C0 register can be used to select the transfer clock polarity.

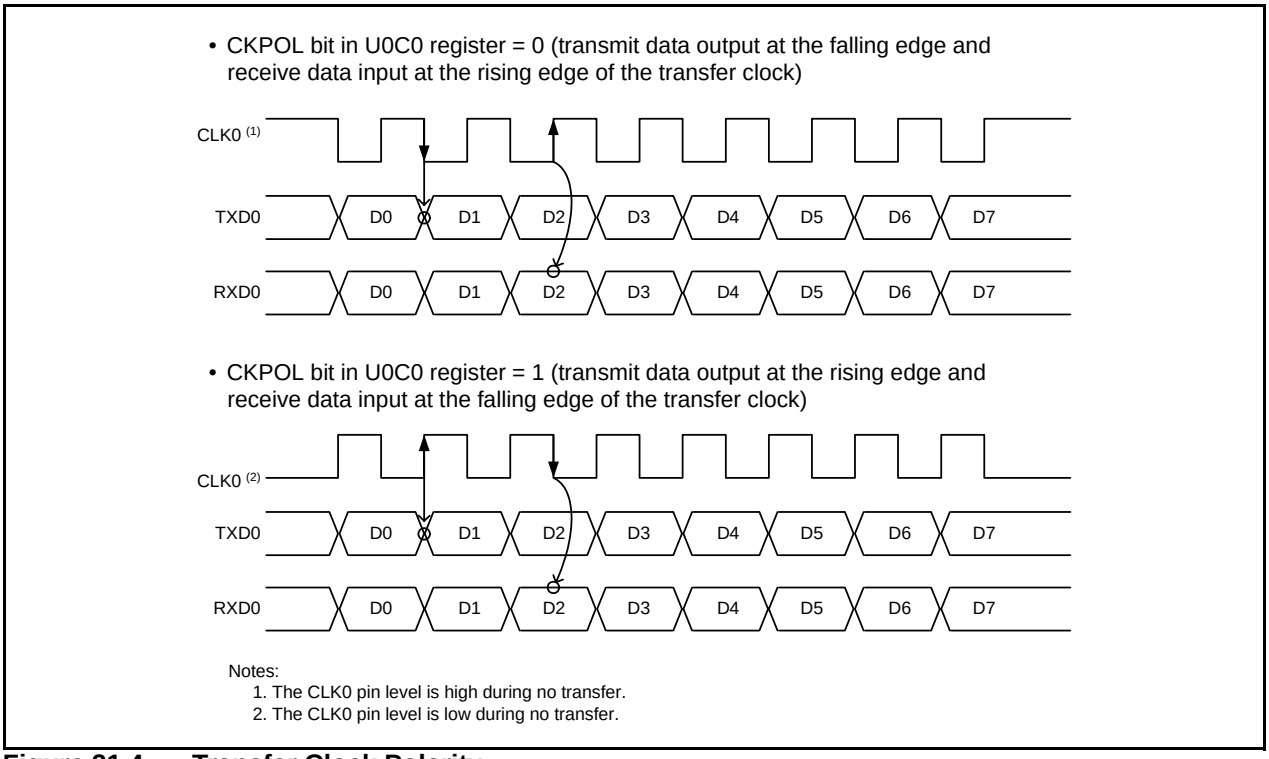

• CKPOL bit in U0C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
CLK0 (1)
TXD0
RXD0
D0
D1
D2
D3
D4
D5
D6
D7
• CKPOL bit in U0C0 register = 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
CLK0 (2)
Notes:
1. The CLK0 pin level is high during no transfer.
2. The CLK0 pin level is low during no transfer.

Figure 21.4 Transfer Clock Polarity

21.3.3 LSB First/MSB First Select Function

Figure 21.5 shows the Transfer Format. The UFORM bit in the U0C0 register can be used to select the transfer format.

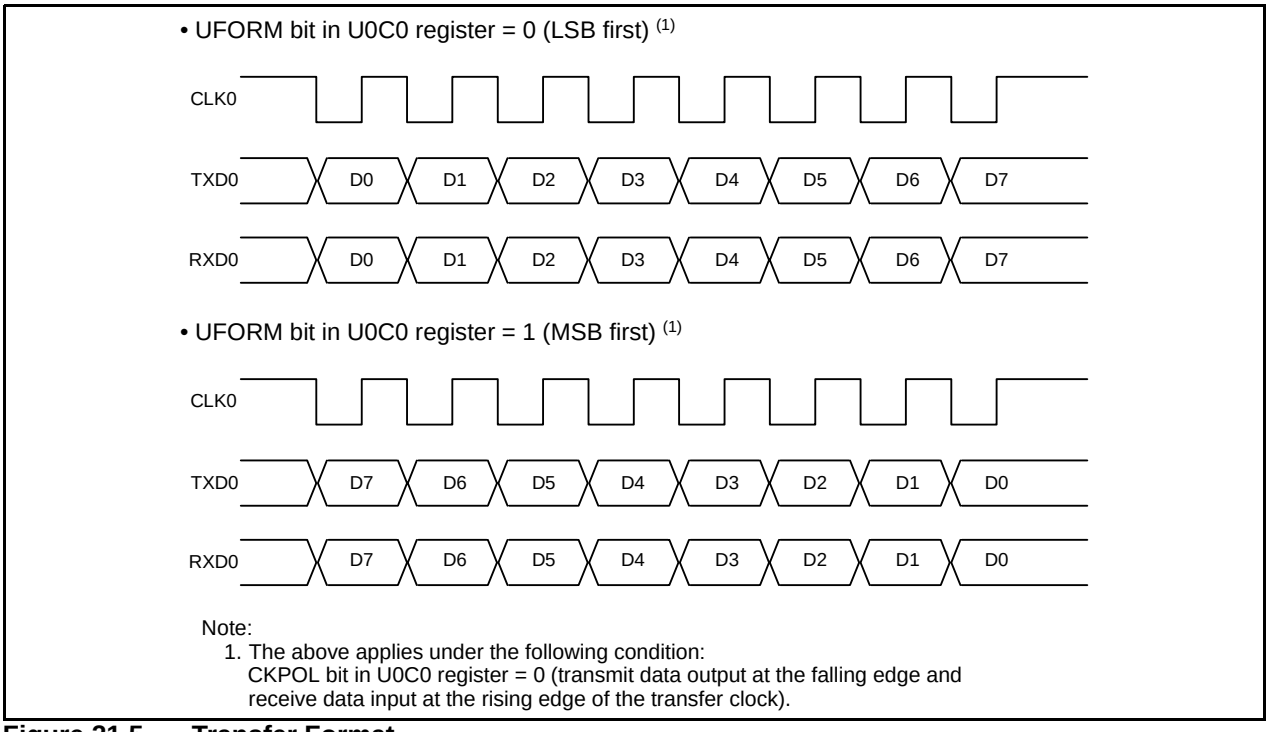

• UFORM bit in U0C0 register = 0 (LSB first) (1)
CLK0
TXD0
RXD0
D0
D1
D2
D3
D4
D5
D6
D7
• UFORM bit in U0C0 register = 1 (MSB first) (1)
Note:
1. The above applies under the following condition:
CKPOL bit in U0C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock).

Figure 21.5 Transfer Format

21.3.4 Continuous Receive Mode

Continuous receive mode is selected by setting the U0RRM bit in the U0C1 register to 1 (continuous receive mode enabled). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to 0 (data in the U0TB register). When the U0RRM bit is set to 1, do not write dummy data to the U0TB register by a program.

21.4 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired transfer rate and transfer data format.
Table 21.5 lists the UART Mode Specifications, and Table 21.6 lists the Registers Used and Settings in UART Mode.

Table 21.5 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bits (transfer data): Selectable from 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 or 2 bits
Transfer clocks	• The CKDIR bit in the U0MR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32, fC n = Value set in U0BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from CLK0 pin, n = Value set in U0BRG register: 00h to FFh
Transmit start conditions	• To start transmission, the following requirements must be met: - The TE bit in the U0C1 register is set to 1 (transmission enabled). - The TI bit in the U0C1 register is set to 0 (data in the U0TB register).
Receive start conditions	• To start reception, the following requirements must be met: - The RE bit in the U0C1 register is set to 1 (reception enabled). - Start bit detection
Interrupt request generation timing	• For transmission, one of the following can be selected. - The U0IRS bit is set to 0 (transmit buffer empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit is set to 1 (transfer completed): When data transmission from the UART0 transmit register is completed. • For reception When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U0RB register and receive the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the set number of stop bits is not detected. • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register will be undefined.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART0 receive register to the U0RB register.

Table 21.6 Registers Used and Settings in UART Mode

Register	Bit	Function
U0TB	b0 to b8	Set transmit data. (1)
U0RB	b0 to b8	Receive data can be read. (2)
	OER, FER, PER, SUM	Error flag
U0BRG	b0 to b7	Set the transfer rate.
U0MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit(s).
	PRY, PRYE	Select whether parity is included and whether odd or even.
U0C0	CLK0, CLK1	Select the count source for the U0BRG register.
	TXEPT	Transmit register empty flag
	NCH	Select the output format of the TXD0 pin.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 bits or 9 bits long.
U0C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U0IRS	Select the UART0 transmit interrupt source.
	U0RRM	Set to 0.

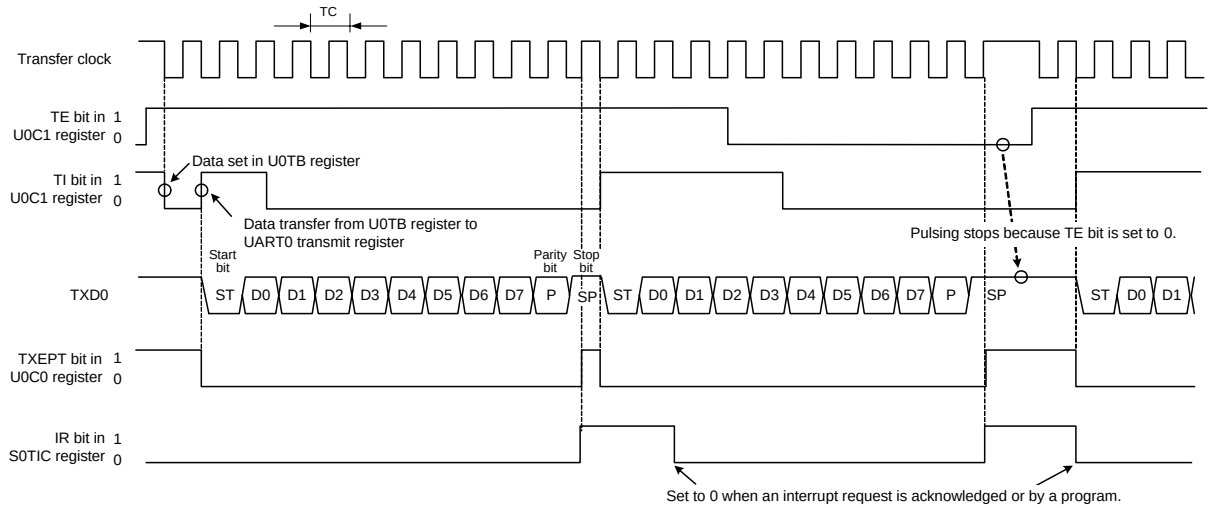
Notes:
1. The bits used for transmission/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits b7 and b8 when the transfer data is 7 bits long
   - Bit b8 when the transfer data is 8 bits long

Table 21.7 lists the I/O Pin Functions in UART Mode.
After the UART0 operating mode is selected, the TXD0 pin outputs a high-level signal until transfer starts. (When the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 21.7 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0 (P8_5)	Serial data output	Bits TXD0SEL1 to TXD0SEL0 in U0SR register = 01b When N-channel open-drain output is selected, PD8_5 bit in PD8 register = 0 For reception only: P8_5 can be used as a port by setting bits TXD0SEL1 to TXD0SEL0 = 00b.
RXD0 (P8_6)	Serial data input	Bits RXD1SEL1 to RXD0SEL0 in U0SR register = 01b PD8_6 bit in PD8 register = 0 For transmission only: P8_6 can be used as a port by setting bits RXD0SEL1 to RXD0SEL0 = 00b.
CLK0 (P8_4)	Programmable I/O port	Bits CLK0SEL1 to CLK0SEL0 in U0SR register = 00b (CLK0 pin not used)
	Transfer clock input	Bits CLK0SEL1 to CLK0SEL0 in U0SR register = 01b CKDIR bit in U0MR register = 1 PD8_4 bit in PD8 register = 0

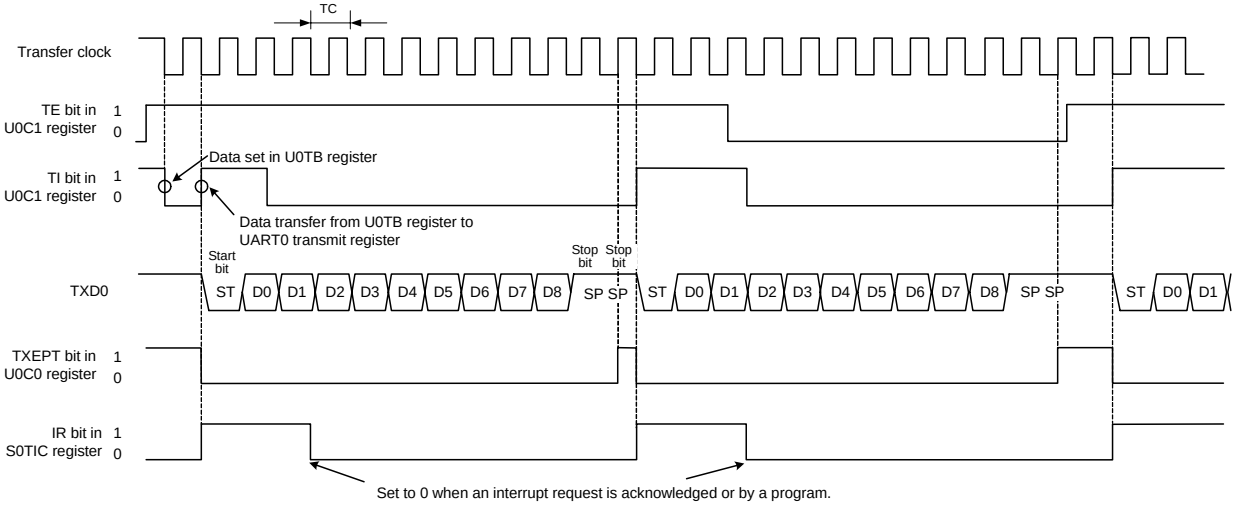
• Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)


TC
Transfer clock
TE bit in U0C1 register
TI bit in U0C1 register
Data set in U0TB register
Data transfer from U0TB register to UART0 transmit register
Pulsing stops because TE bit is set to 0.
Start bit
Parity bit
Stop bit
TXD0
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP
TXEPT bit in U0C0 register
IR bit in S0TIC register
Set to 0 when an interrupt request is acknowledged or by a program.

The above applies under the following conditions:
- PRYE bit in U0MR register = 1 (parity enabled)
- STPS bit in U0MR register = 0 (one stop bit)
- U0IRS bit in U0C1 register = 1
  (interrupt request generation when transmission is completed)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of U0BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U0BRG count source (external clock)
n: Value set in U0BRG register

• Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)


TC
Transfer clock
TE bit in U0C1 register
TI bit in U0C1 register
Data set in U0TB register
Data transfer from U0TB register to UART0 transmit register
Start bit
Stop bit
Stop bit
TXD0
ST D0 D1 D2 D3 D4 D5 D6 D7 D8 SP SP
TXEPT bit in U0C0 register
IR bit in S0TIC register
Set to 0 when an interrupt request is acknowledged or by a program.

The above applies under the following conditions:
- PRYE bit in U0MR register = 0 (parity disabled)
- STPS bit in U0MR register = 1 (two stop bits)
- U0IRS bit in U0C1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of U0BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U0BRG count source (external clock)
n: Value set in U0BRG register

Figure 21.6 Transmit Timing in UART Mode

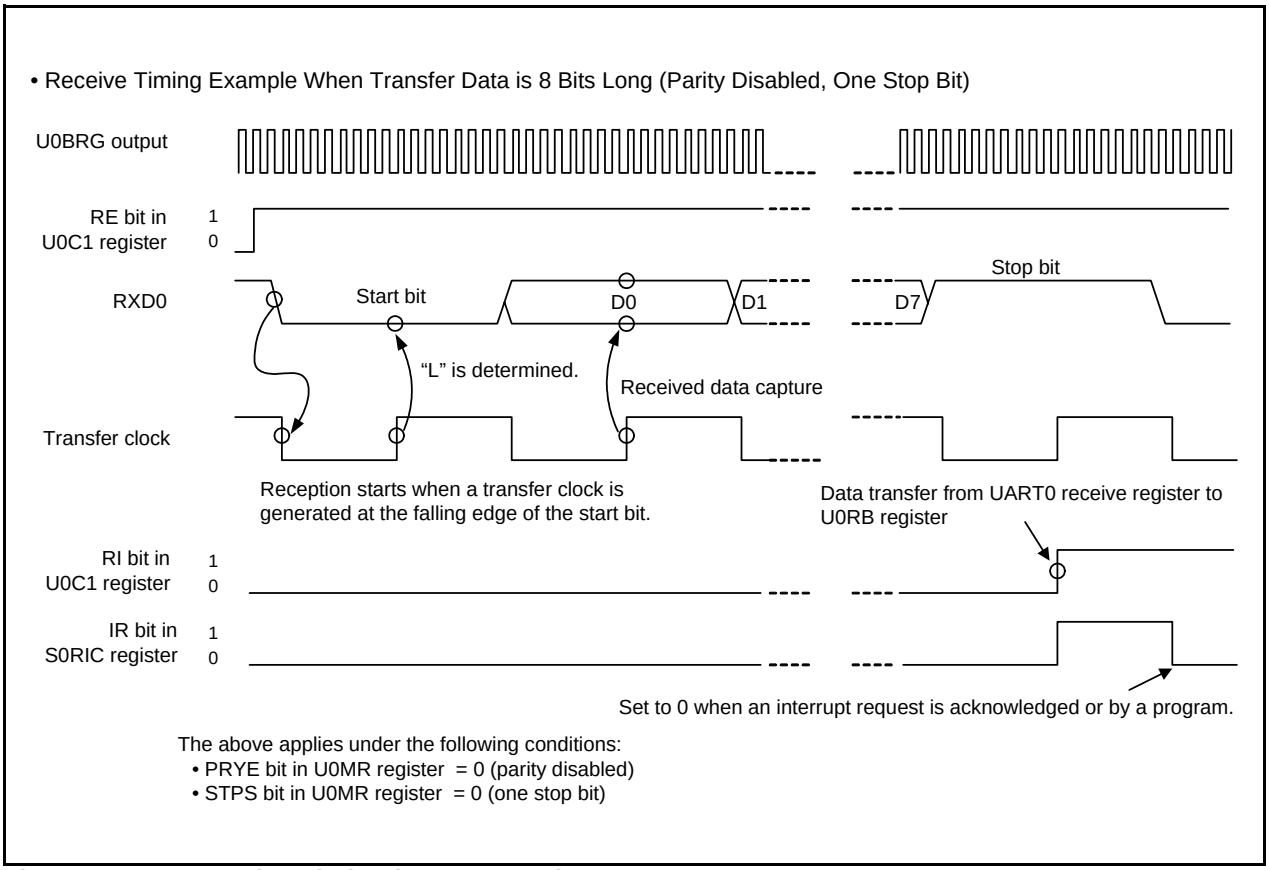

• Receive Timing Example When Transfer Data is 8 Bits Long (Parity Disabled, One Stop Bit)
U0BRG output
RE bit in U0C1 register
1
0
RXD0
Start bit
D0
D1
D7
Stop bit
"L" is determined.
Received data capture
Transfer clock
Reception starts when a transfer clock is generated at the falling edge of the start bit.
Data transfer from UART0 receive register to U0RB register
RI bit in U0C1 register
IR bit in S0RIC register
Set to 0 when an interrupt request is acknowledged or by a program.
The above applies under the following conditions:
• PRYE bit in U0MR register = 0 (parity disabled)
• STPS bit in U0MR register = 0 (one stop bit)

Figure 21.7 Receive Timing in UART Mode

21.4.1 Bit Rate

In UART mode, the bit rate is the frequency (divided by the U0BRG register) divided by 16.

UART mode

• Internal clock selected

$$\text{Setting value of U0BRG register} = \frac{fj}{\text{Bit rate} \times 16} - 1$$

fj: Count source frequency of U0BRG register (f1, f8, f32, or fC)

• External clock selected

$$\text{Setting value of U0BRG register} = \frac{fEXT}{\text{Bit rate} \times 16} - 1$$

fEXT: Count source frequency of U0BRG register (external clock)

Figure 21.8 Formula for Calculating Setting Value of U0BRG Register

Table 21.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	U0BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		U0BRG Setting Value	Actual Time (bps)	Setting Error (%)	U0BRG Setting Value	Actual Time (bps)	Setting Error (%)	U0BRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	—	—	—

Note:

1. For the high-speed on-chip oscillator, the correction value of the FR18S0 register should be written into the FRC0 register and the correction value of the FR18S1 register should be written into the FRC1 register. This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-1 mode).

21.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.5 Notes on Serial Interface (UART0)

- When reading data from the U0RB register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the U0RB register is read, bits PER and FER in the U0RB register and the RI bit in the U0C1 register are set to 0.
  To check receive errors, read the U0RB register and then use the read data.

  Program example to read the receive buffer register:
  ```
  MOV.W    00A6H,R0    ; Read the U0RB register
  ```

- When writing data to the U0TB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:
  ```
  MOV.B    #XXH,00A3H  ; Write to the high-order byte of the U0TB register
  MOV.B    #XXH,00A2H  ; Write to the low-order byte of the U0TB register
  ```

22. Serial Interface (UART2)

Note

The description offered in this chapter is based on the R8C/LA8A Group.
For other groups, refer to 1.1.2 Differences between Groups.

The serial interface consists of two channels, UART0 and UART2. This chapter describes UART2.

22.1 Introduction

UART2 has a dedicated timer to generate a transfer clock.
Figure 22.1 shows a Block Diagram of UART2. Figure 22.2 shows a Block Diagram of UART2 Transmit/Receive Unit. Table 22.1 lists the UART 2 Pin Configuration.

UART2 supports the following modes:

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Special mode 1 (I^2C mode)
- Multiprocessor communication function

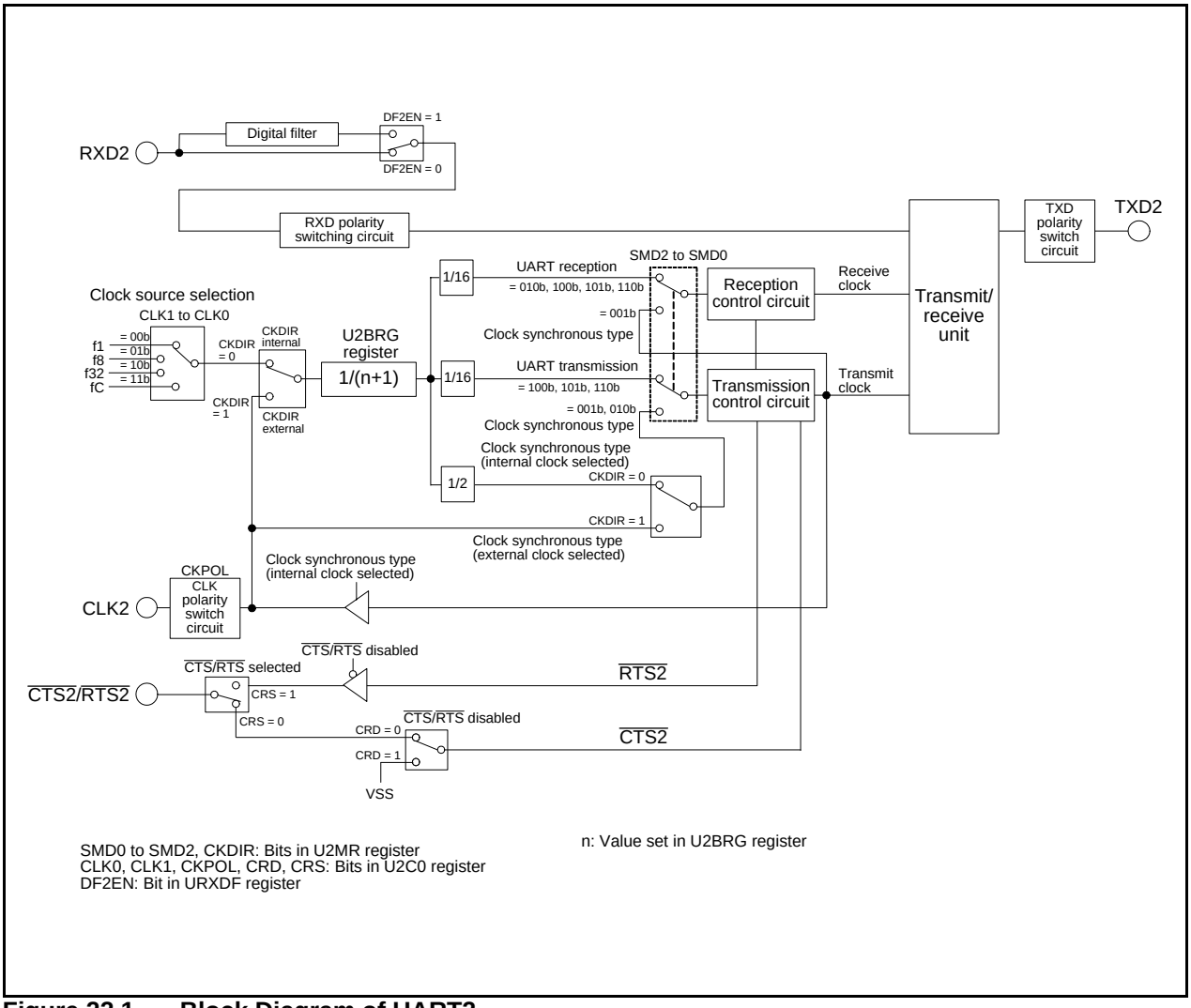


Figure 22.1 Block Diagram of UART2

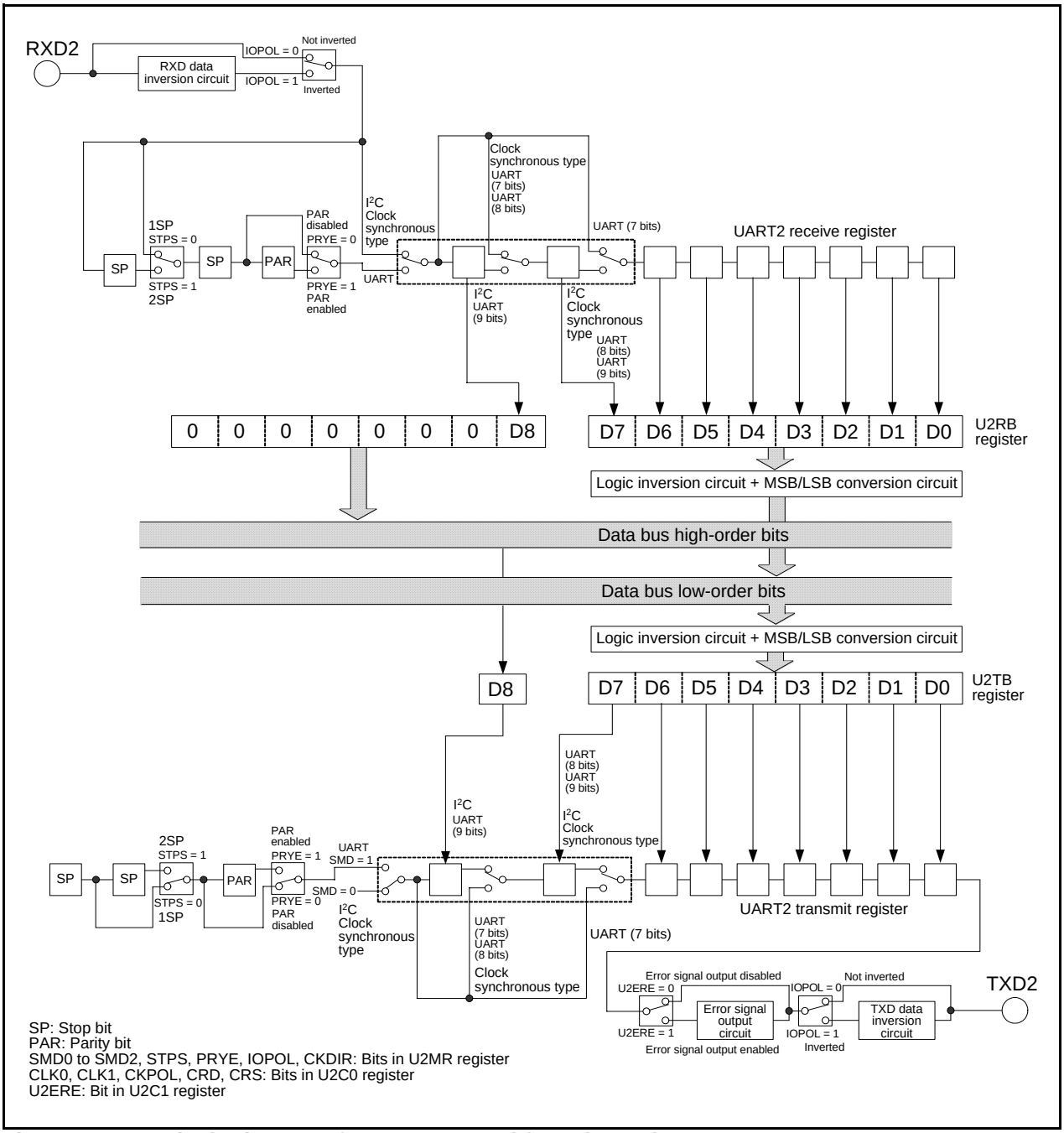


Figure 22.2 Block Diagram of UART2 Transmit/Receive Unit

Table 22.1 UART 2 Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TXD2	P7_1, P7_2, or P8_5	Output	Serial data output
RXD2	P7_1, P7_2, or P8_6	Input	Serial data input
CLK2	P7_0, P8_4	I/O	Transfer clock I/O
$\overline{\text{CTS2}}$	P7_3, P8_7	Input	Transmission control input
$\overline{\text{RTS2}}$	P7_3, P8_7	Output	Reception control input
SCL2	P7_1, P7_2, or P8_6	I/O	I2C mode clock I/O
SDA2	P7_1, P7_2, or P8_5	I/O	I2C mode data I/O

22.2 Registers

22.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	MSTURT2	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	UART0 standby bit	0: Active 1: Standby (1)	R/W
b2	MSTURT2	UART2 standby bit	0: Active 1: Standby (2)	R/W
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (3)	R/W
b4	MSTLCD	LCD standby bit	0: Active 1: Standby (4)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (5)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	A/D standby bit (6)	0: Active 1: Standby	R/W

Notes:

1. When the MSTURT0 bit is set to 1 (standby), any access to the UART0 associated registers (addresses 00A0h to 00A7h) is disabled.
2. When the MSTURT2 bit is set to 1 (standby), any access to the timer UART2 associated registers (addresses 00A8h to 00BFh) is disabled.
3. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
4. When the MSTLCD bit is set to 1 (standby), any access to the timer LCD associated registers (addresses 0200h to 0237h) is disabled.
5. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
6. When the MSTADC bit is set to 1 (standby), any access to the timer A/D associated registers (addresses 00C0h to 00D9h, 00DCh to 00DFh) is disabled.
   Set the MSTADC bit to 0 (active) when the temperature sensor is used.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

22.2.2 UART2 Transmit/Receive Mode Register (U2MR)

Address 00A8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOPOL	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit (1, 2)	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 0 1 0: I^2C mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	IOPOL	TXD, RXD I/O polarity switch bit	0: Not inverted 1: Inverted	R/W

Notes:
1. When setting bits SMD2 to SMD0 to 000b (serial interface disabled), set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. When bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode), the error flags (bits FER, PER, and SUM) in the U2RB register are disabled. When these bits are read, the values are undefined.

22.2.3 UART2 Bit Rate Register (U2BRG)

Address 00A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U2BRG divides the count source by n+1.	00h to FFh	W

Write to the U2BRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK1 to CLK0 in the U2C0 register before writing to the U2BRG register.

22.2.4 UART2 Transmit Buffer Register (U2TB)

Address 00ABh to 00AAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	MPTB
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data (D7 to D0)	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	MPTB	Transmit data (D8) (1) [When the multiprocessor communication function is not used] Transmit data (D8) [When the multiprocessor communication function is used] • To transfer an ID, set the MPTB bit to 1. • To transfer data, set the MPTB bit to 0.	W
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

Note:
1. Set bits b0 to b7 after setting the MPTB bit.

22.2.5 UART2 Transmit/Receive Control Register 0 (U2C0)

Address 00ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	CRD	TXEPT	CRS	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	U2BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: fC selected	R/W
b1	CLK1			R/W
b2	CRS	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function select bit	Enabled when CRD = 0 0: $\overline{\text{CTS}}$ function selected 1: $\overline{\text{RTS}}$ function selected	R/W
b3	TXEPT	Transmit register empty flag	0: Data in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	CRD	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ disable bit	0: $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function enabled 1: $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled	R/W
b5	NCH	Data output select bit	0: Pins TXD2/SDA2, SCL2 set as CMOS output 1: Pins TXD2/SDA2, SCL2 set as N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit (2)	0: LSB first 1: MSB first	R/W

Notes:
1. If bits CLK1 to CLK0 are switched, set the U2BRG register again.
2. The UFORM bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), or set to 101b (UART mode, transfer data 8 bits long).
   Set the UFORM bit to 1 when bits SMD2 to SMD0 are set to 010b (I^2C mode), and to 0 when bits SMD2 to SMD0 are set to 100b (UART mode, transfer data 7 bits long) or 110b (UART mode, transfer data 9 bits long).

22.2.6 UART2 Transmit/Receive Control Register 1 (U2C1)

Address 00ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	U2ERE	U2LCH	U2RRM	U2IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data in the U2TB register 1: No data in the U2TB register	R
b2	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Reception complete flag	0: No data in the U2RB register 1: Data in the U2RB register	R
b4	U2IRS	UART2 transmit interrupt source select bit	0: Transmit buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U2RRM	UART2 continuous receive mode enable bit	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	U2LCH	Data logic select bit (1)	0: Not inverted 1: Inverted	R/W
b7	U2ERE	Error signal output enable bit	0: Output disabled 1: Output enabled	R/W

Note:
1. The U2LCH bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), 100b (UART mode, transfer data 7 bits long), or 101b (UART mode, transfer data 8 bits long). Set the U2LCH bit to 0 when bits SMD2 to SMD0 are set to 010b (I^2C mode) or 110b (UART mode, transfer data 9 bits long).

22.2.7 UART2 Receive Buffer Register (U2RB)

Address 00AFh to 00AEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	MPRB
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	MPRB	—	Receive data (D8) (1) [When the multiprocessor communication function is not used] Receive data (D8) [When the multiprocessor communication function is used] • When the MPRB bit is set to 0, received D0 to D7 are data fields. • When the MPRB bit is set to 1, received D0 to D7 are ID fields.	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—	Reserved bit	Set to 0.	R/W
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Notes:
1. When bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled) or the RE bit in the U2C1 register is set to 0 (reception disabled), all of bits SUM, PER, FER, and OER are set to 0 (no error). The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error). Bits PER and FER are set to 0 by reading the lower byte of the U2RB register.
   When setting bits SMD2 to SMD0 in the U2MR register to 000b, set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are disabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). When read, the contents are undefined.

22.2.8 UART2 Digital Filter Function Select Register (URXDF)

Address 00B0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	DF2EN	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	DF2EN	RXD2 digital filter enable bit (1)	0: RXD2 digital filter disabled 1: RXD2 digital filter enabled	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. The RXD2 digital filter can be used only in clock asynchronous serial I/O (UART) mode. When bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode) or 010b (I^2C mode), set the DF2EN bit to 0 (RXD2 digital filter disabled).

22.2.9 UART2 Special Mode Register 5 (U2SMR5)

Address 00BBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MPIE	—	—	—	MP
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MP	Multiprocessor communication enable bit	0: Multiprocessor communication disabled 1: Multiprocessor communication enabled (1)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	MPIE	Multiprocessor communication control bit	When the MP bit is set to 1 (multiprocessor communication enabled), this bit is enabled. When the MPIE bit is set to 1, the following will result: • Receive data in which the multiprocessor bit is 0 is ignored. The settings of the RI bit in the U2C1 register and bits OER and FER in the U2RB register to 1 are disabled. • On receiving receive data in which the multiprocessor bit is 1, the MPIE bit is set to 0 and receive operation other than multiprocessor communication is performed.	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. When the MP bit is set to 1 (multiprocessor communication enabled), the settings of bits PRY and PRYE in the U2MR register are disabled. If bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), set the MP bit to 0 (multiprocessor communication disabled).

22.2.10 UART2 Special Mode Register 4 (U2SMR4)

Address 00BCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SWC9	SCLHI	ACKC	ACKD	STSPSEL	STPREQ	RSTAREQ	STAREQ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	STAREQ	Start condition generate bit (1)	0: Clear 1: Start	R/W
b1	RSTAREQ	Restart condition generate bit (1)	0: Clear 1: Start	R/W
b2	STPREQ	Stop condition generate bit (1)	0: Clear 1: Start	R/W
b3	STSPSEL	SCL, SDA output select bit	0: Start and stop conditions not output 1: Start and stop conditions output	R/W
b4	ACKD	ACK data bit	0: ACK 1: NACK	R/W
b5	ACKC	ACK data output enable bit	0: Serial interface data output 1: ACK data output	R/W
b6	SCLHI	SCL output stop enable bit	0: Disabled 1: Enabled	R/W
b7	SWC9	SCL wait bit 3	0: SCL hold low disabled 1: SCL hold low enabled	R/W

Note:
1. This bit is set to 0 when the condition is generated.

22.2.11 UART2 Special Mode Register 3 (U2SMR3)

Address 00BDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DL2	DL1	DL0	—	NODC	—	CKPH	—
After Reset	0	0	0	X	0	X	0	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b1	CKPH	Clock phase set bit	0: No clock delay 1: With clock delay	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	NODC	Clock output select bit	0: CLK2 set as CMOS output 1: CLK2 set as N-channel open-drain output	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	DL0	SDA2 digital delay setup bit (1, 2)	b7 b6 b5 0 0 0: No delay 0 0 1: 1 or 2 cycles of U2BRG count source 0 1 0: 2 or 3 cycles of U2BRG count source 0 1 1: 3 or 4 cycles of U2BRG count source 1 0 0: 4 or 5 cycles of U2BRG count source 1 0 1: 5 or6 cycles of U2BRG count source 1 1 0: 6 or 7 cycles of U2BRG count source 1 1 1: 7 or 8 cycles of U2BRG count source	R/W
b6	DL1			R/W
b7	DL2			R/W

Notes:
1. Bits DL2 to DL0 are used to generate a delay in SDA2 output digitally in I²C mode. In other than I²C mode, set these bits to 000b (no delay).
2. The amount of delay varies with the load on pins SCL2 and SDA2. When an external clock is used, the amount of delay increases by about 100 ns.

22.2.12 UART2 Special Mode Register 2 (U2SMR2)

Address 00BEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SDHI	SWC2	STAC	—	SWC	CSC	IICM2
After Reset	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICM2	I²C mode select bit 2	Refer to **Table 22.12 I²C Mode Functions**.	R/W
b1	CSC	Clock synchronization bit	0: Disabled 1: Enabled	R/W
b2	SWC	SCL wait output bit	0: Disabled 1: Enabled	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	STAC	UART2 initialization bit	0: Disabled 1: Enabled	R/W
b5	SWC2	SCL wait output bit 2	0: Transfer clock 1: Low-level output	R/W
b6	SDHI	SDA output disable bit	0: Enabled 1: Disabled (high impedance)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

22.2.13 UART2 Special Mode Register (U2SMR)

Address 00BFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	BBS	—	IICM
After Reset	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICM	I^2C mode select bit	0: Other than I^2C mode 1: I^2C mode	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	BBS	Bus busy flag (1)	0: Stop condition detected 1: Start condition detected (busy)	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. The BBS bit is set to 0 by writing 0 by a program (Writing 1 has no effect).

22.2.14 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RXD2SEL1	RXD2SEL0	—	—	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2/SDA2 pin select bit	b1 b0 0 0: TXD2/SDA2 pin not used 0 1: P7_1 assigned 1 0: P7_2 assigned 1 1: P8_5 assigned	R/W
b1	TXD2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	RXD2SEL0	RXD2/SCL2 pin select bit	b5 b4 0 0: RXD2/SCL2 pin not used 0 1: P7_2 assigned 1 0: P7_1 assigned 1 1: P8_6 assigned	R/W
b5	RXD2SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR0 register selects which pin is assigned as the UART2 input/output. To use the I/O pins for UART2, set this register.
Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value of this register during UART2 operation.

22.2.15 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CTS2SEL1	CTS2SEL0	—	—	CLK2SEL1	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bit	b1 b0 0 0: CLK2 pin not used 0 1: P7_0 assigned 1 0: P8_4 assigned 1 1: Do not set.	R/W
b1	CLK2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	CTS2SEL0	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin select bit	b5 b4 0 0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin not used 0 1: P7_3 assigned 1 0: P8_7 assigned 1 1: Do not set.	R/W
b5	CTS2SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR1 register selects which pin is assigned as the UART2 input/output. To use the I/O pins for UART2, set this register.
Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value of this register during UART2 operation.

22.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 22.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 22.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 22.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(2(n+1)) fj = f1, f8, f32, fC n = Value set in U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLK2 pin
Transmission/reception control	Selectable from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled.
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U2C1 register is set to 1 (transmission enabled) • The TI bit in the U2C1 register is set to 0 (data in the U2TB register) • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U2C1 register is set to 1 (reception enabled). • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
Interrupt request generation timing	For transmission, one of the following conditions can be selected. • The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). • The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. For reception • When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data I/O can be selected to occur synchronously with the rising or falling edge of the transfer clock. • LSB first, MSB first selection Whether data transmission/reception begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Receive operation is enabled immediately by reading the U2RB register. • Serial data logic switching This function inverts the logic value of transmit/receive data.

Notes:
1. If an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the U2C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data in the U2RB register will be undefined.

Table 22.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode

Register	Bit	Function
U2TB (1)	b0 to b7	Set transmit data.
U2RB (1)	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U2BRG	b0 to b7	Set the transfer rate.
U2MR (1)	SMD2 to SMD0	Set to 001b.
	CKDIR	Select an internal clock or external clock.
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Select either $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use the function.
	TXEPT	Transmit register empty flag
	CRD	Select the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function enabled or disabled.
	NCH	Select the output format of the TXD2 pin.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
U2C1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source
	U2RRM	Set to 1 to use continuous receive mode.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b2	Set to 0.
	NODC	Select the clock output format.
	b4 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Set to 0.
U2SMR5	MP	Set to 0.

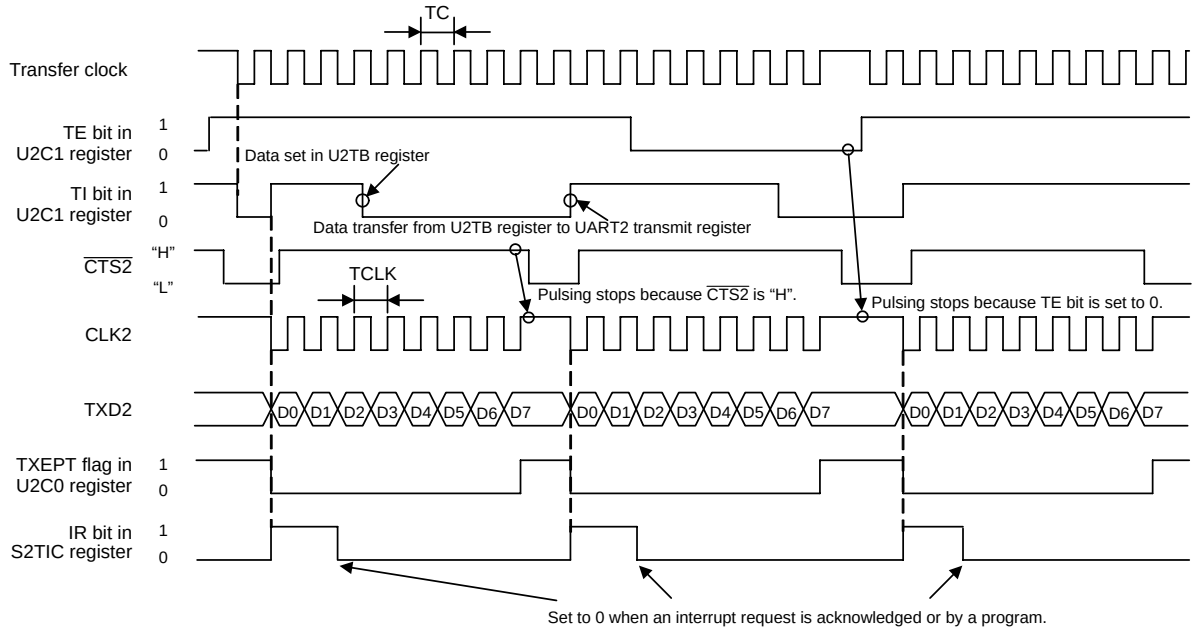
Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 22.4 lists the Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected).
After UART2 operating mode is selected, the TXD2 pin outputs a high-level signal until transfer starts.
(When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 22.3 shows the Transmit and Receive Timing in Clock Synchronous Serial I/O Mode.

Table 22.4 Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected)

Pin Name	Function	Selection Method
TXD2 (P7_1, P7_2, or P8_5)	Serial data output	• When TXD2 (P7_1) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 01b (P7_1) When N-channel open-drain output is selected, PD7_1 bit in PD7 register = 0 • When TXD2 (P7_2) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 10b (P7_2) When N-channel open-drain output is selected, PD7_2 bit in PD7 register = 0 • When TXD2 (P8_5) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 11b (P8_5) When N-channel open-drain output is selected, PD8_5 bit in PD8 register = 0 • For reception only: P7_1, P7_2 and P8_5 can be used as ports by setting TXD2SEL1 to TXD2SEL0 to 00b.
RXD2 (P7_1, P7_2, or P8_6)	Serial data input	• When RXD2 (P7_1) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 01b (P7_1) Bit PD7_1 in PD7 register = 0 • When RXD2 (P7_2) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 10b (P7_2) Bit PD7_2 in PD7 register = 0 • When RXD2 (P8_6) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 11b (P8_6) Bit PD8_6 in PD8 register = 0 • For transmission only: P7_1, P7_2 and P8_6 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b.
CLK2 (P7_0 or P8_4)	Transfer clock output	• When CLK2 (P7_0) Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 01b (P7_1) Bit CKDIR in U2MR register = 0 When N-channel open-drain output is selected, PD7_0 bit in PD7 register = 0 • When CLK2 (P8_4) Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 10b (P8_4) Bit CKDIR in U2MR register = 0 When N-channel open-drain output is selected, PD8_4 bit in PD8 register = 0
	Transfer clock input	• When CLK2 (P7_0) Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 01b (P7_0) Bit CKDIR in U2MR register = 1 Bit PD7_0 in PD7 register = 0 • When CLK2 (P8_4) Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 10b (P8_4) Bit CKDIR in U2MR register = 1 Bit PD8_4 in PD8 register = 0
$\overline{\text{CTS2}}/\overline{\text{RTS2}}$ (P7_3 or P8_7)	$\overline{\text{CTS}}$ input	• When $\overline{\text{CTS2}}$ (P7_3) Bits CTS2SEL1 to CTS2SEL0 in U2SR1 register = 01b (P7_3) Bit CRD in U2C0 register = 0 Bit CRS in U2C0 register = 0 Bit PD7_3 in PD7 register = 0 • When $\overline{\text{CTS2}}$ (P8_7) Bits CTS2SEL1 to CTS2SEL0 in U2SR1 register = 10b (P8_7) Bit CRD in U2C0 register = 0 Bit CRS in U2C0 register = 0 Bit PD8_7 in PD8 register = 0
	$\overline{\text{RTS}}$ output	• When $\overline{\text{RTS2}}$ (P7_3) Bits CTS2SEL1 to CTS2SEL0 in U2SR1 register = 01b (P7_3) Bit CRD in U2C0 register = 0 Bit CRS in U2C0 register = 1 • When $\overline{\text{RTS2}}$ (P8_7) Bits CTS2SEL1 to CTS2SEL1 in U2SR1 register = 10b (P8_7) Bit CRD in U2C0 register = 0 Bit CRS in U2C0 register = 1
	I/O port	Bits CTS2SEL1 to CTS2SEL0 to U2SR1 register = 00b

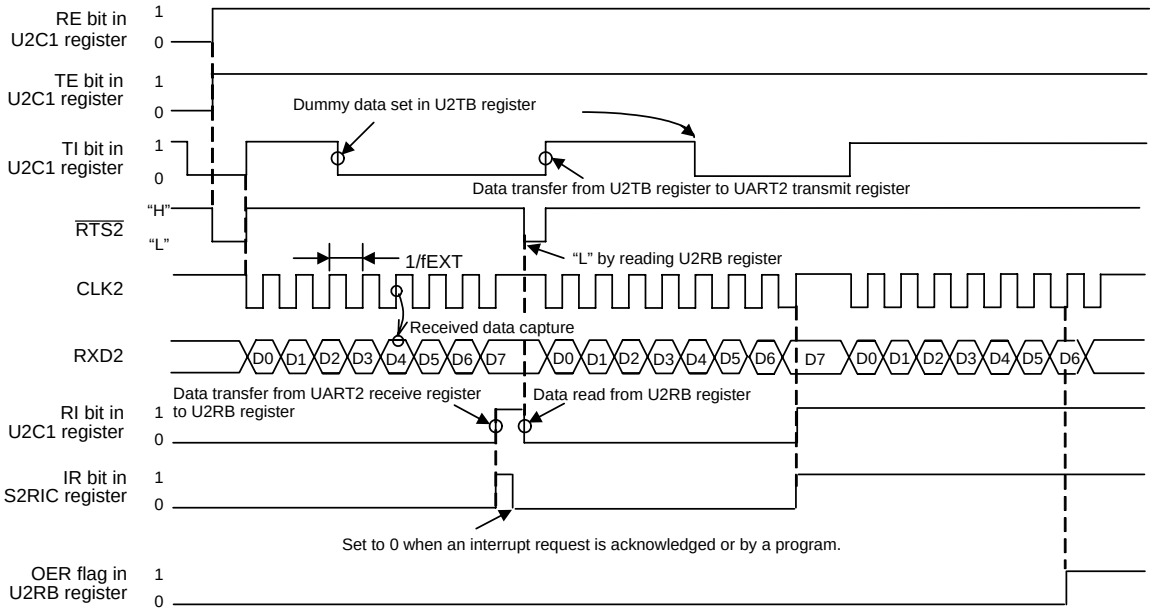
(1) Transmit Timing Example (Internal Clock Selected)


TC
Transfer clock
TE bit in U2C1 register
TI bit in U2C1 register
CTS2
"H"
"L"
TCLK
CLK2
TXD2
TXEPT flag in U2C0 register
IR bit in S2TIC register
1
0
Data set in U2TB register
Data transfer from U2TB register to UART2 transmit register
Pulsing stops because CTS2 is "H".
Pulsing stops because TE bit is set to 0.
D0 D1 D2 D3 D4 D5 D6 D7
Set to 0 when an interrupt request is acknowledged or by a program.

The above applies under the following conditions:
- CKDIR bit in U2MR register = 0 (internal clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- CKPOL bit in U2C0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the U2TB register is empty)

TC = TCLK = 2(n+1)/fj
fj: Frequency of U2BRG count source
(f1, f8, f32, fC)
n: Value set in U2BRG register

(2) Receive Timing Example (External Clock Selected)


RE bit in U2C1 register
TE bit in U2C1 register
TI bit in U2C1 register
RTS2
"H"
"L"
CLK2
RXD2
RI bit in U2C1 register
IR bit in S2RIC register
OER flag in U2RB register
1
0
Dummy data set in U2TB register
Data transfer from U2TB register to UART2 transmit register
1/fEXT
"L" by reading U2RB register
Received data capture
D0 D1 D2 D3 D4 D5 D6 D7
Data transfer from UART2 receive register to U2RB register
Data read from U2RB register
Set to 0 when an interrupt request is acknowledged or by a program.

The above applies under the following conditions:
- CKDIR bit in U2MR register = 1 (external clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 1 (RTS function selected)
- CKPOL bit in U2C0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

fEXT: Frequency of external clock

Make sure the following conditions are met when the CLK2 pin input is high before receiving data:
- TE bit in U2C0 register = 1 (transmission enabled)
- RE bit in U2C1 register = 1 (reception enabled)
- Dummy data write to the U2TB register

Figure 22.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

22.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

22.3.2 CLK Polarity Select Function

The CKPOL bit in the U2C0 register can be used to select the transfer clock polarity. Figure 22.4 shows the Transfer Clock Polarity.

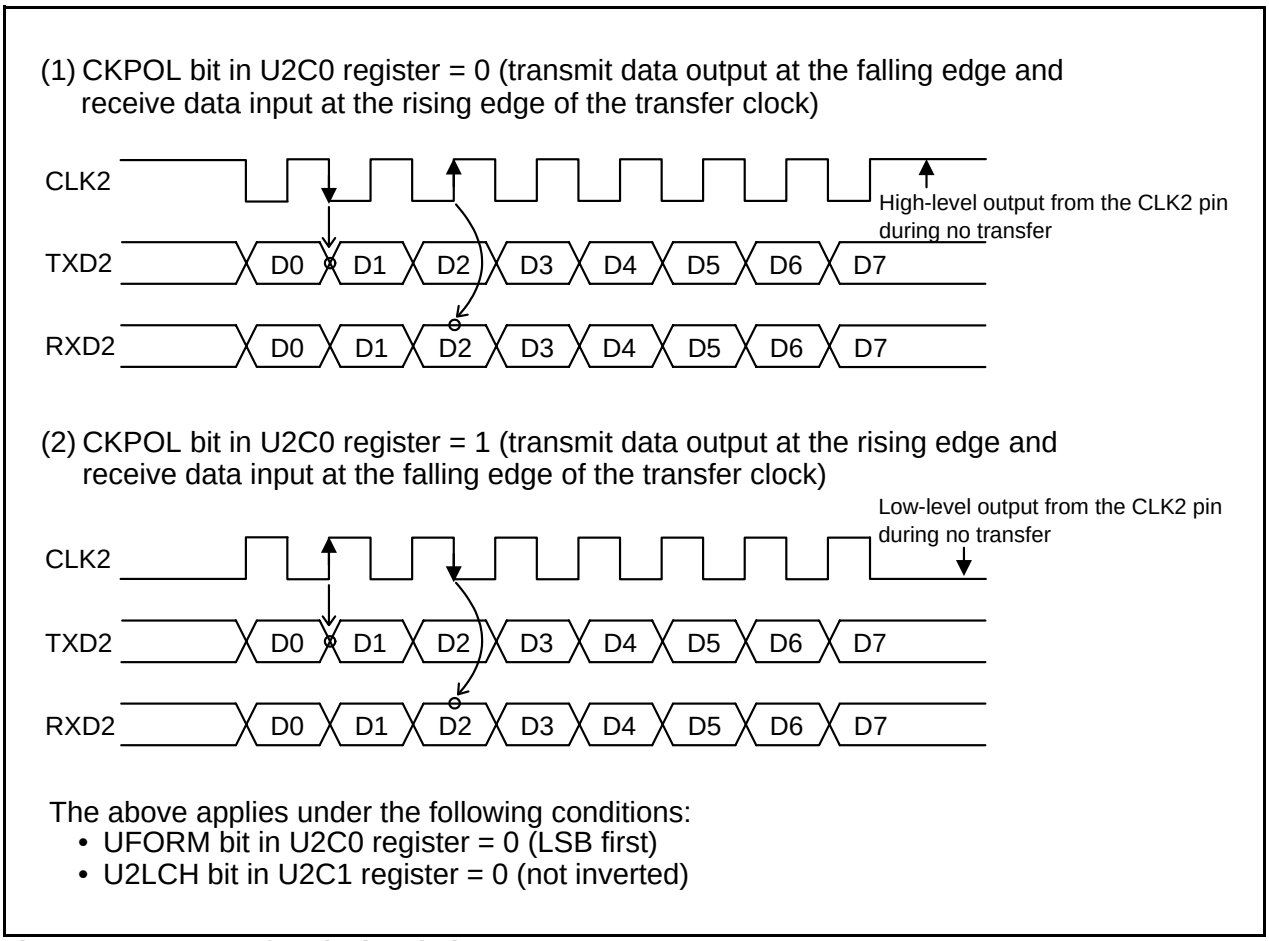

(1) CKPOL bit in U2C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
CLK2
TXD2
RXD2
D0
D1
D2
D3
D4
D5
D6
D7
High-level output from the CLK2 pin during no transfer
(2) CKPOL bit in U2C0 register = 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
Low-level output from the CLK2 pin during no transfer
The above applies under the following conditions:
• UFORM bit in U2C0 register = 0 (LSB first)
• U2LCH bit in U2C1 register = 0 (not inverted)

Figure 22.4 Transfer Clock Polarity

22.3.3 LSB First/MSB First Select Function

The UFORM bit in the U2C0 register can be used to select the transfer format. Figure 22.5 shows the Transfer Format.

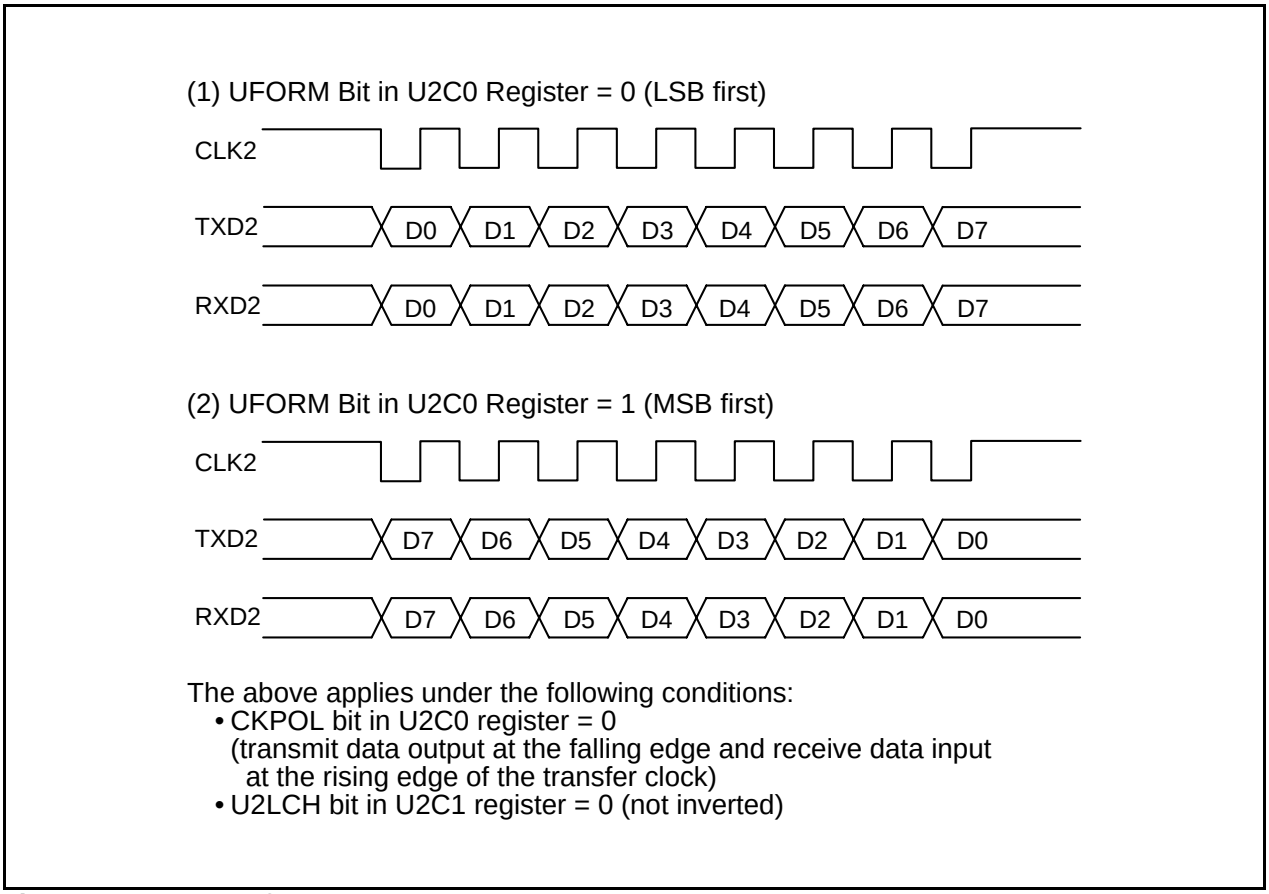

(1) UFORM Bit in U2C0 Register = 0 (LSB first)
CLK2
TXD2
D0 D1 D2 D3 D4 D5 D6 D7
RXD2
D0 D1 D2 D3 D4 D5 D6 D7
(2) UFORM Bit in U2C0 Register = 1 (MSB first)
CLK2
TXD2
D7 D6 D5 D4 D3 D2 D1 D0
RXD2
D7 D6 D5 D4 D3 D2 D1 D0
The above applies under the following conditions:
• CKPOL bit in U2C0 register = 0
(transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
• U2LCH bit in U2C1 register = 0 (not inverted)

Figure 22.5 Transfer Format

22.3.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled by reading the receive buffer register. If this mode is selected, writing dummy data to the transmit buffer register is not required to enable receive operation. However, a dummy reading of the receive buffer register is required when starting transmission.

When the U2RRM bit in the U2C1 register is set to 1 (continuous receive mode), the TI bit in the U2C1 register is set to 0 (data in the U2TB register) by reading the U2RB register. When the U2RRM bit is set to 1, do not write dummy data to the U2TB register by a program.

22.3.5 Serial Data Logic Switching Function

When the U2LCH bit in the U2C1 register is set to 1 (inverted), the data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 22.6 shows the Serial Data Logic Switching.

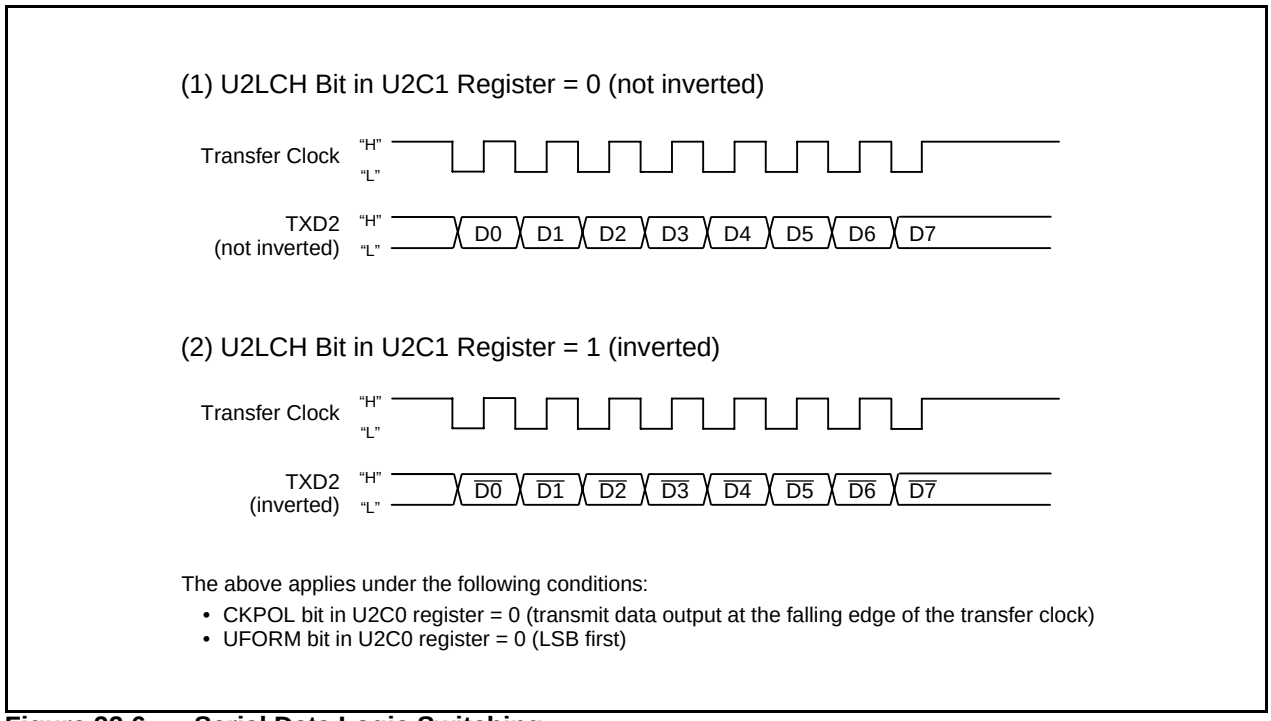


Figure 22.6 Serial Data Logic Switching

22.3.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit and receive operation when a low-level signal is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit and receive operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the input level is switched to high during a transmit or receive operation, the operation stops before the next data.
For the $\overline{\text{RTS}}$ function, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs a low-level signal when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the CLK2 pin.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

22.4 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting the desired transfer rate and transfer data format. Table 22.5 lists the UART Mode Specifications. Table 22.6 lists the Registers Used and Settings in UART Mode.

Table 22.5 UART Mode Specifications

Item	Specification
Transfer data format	• Character bits (transfer data): Selectable from 7, 8, or 9 bits • Start bit:1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 bit or 2 bits
Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(16(n + 1)) fj = f1, f8, f32, fC n = Value set in U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n + 1)) fEXT: Input from CLK2 pin n: Value set in U2BRG register: 00h to FFh
Transmission/reception control	Selectable from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled.
Transmit start conditions	To start transmission, the following requirements must be met: • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data in the U2TB register). • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.
Receive start conditions	To start reception, the following requirements must be met: • The RE bit in the U2C1 register is set to 1 (reception enabled). • Start bit detection
Interrupt request generation timing	For transmission, one of the following conditions can be selected. • The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). • The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. For reception • When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the bit one before the last stop bit of the next unit of data. • Framing error (2) This error occurs when the set number of stop bits is not detected. • Parity error (2) This error occurs when if parity is enabled, the number of 1's in the parity and character bits does not match the set number of 1's. • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.
Selectable functions	• LSB first, MSB first selection Whether data transmission/reception begins with bit 0 or begins with bit 7 can be selected. • Serial data logic switching This function inverts the logic of transmit/receive data. Start and stop bits are not inverted. • TXD, RXD I/O polarity switching This function inverts the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are inverted. • RAD2 digital filter selection The digital filter for the RXD2 input signal can be enabled or disabled.

Notes:
1. If an overrun error occurs, the receive data in the U2RB register will be undefined.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART2 receive register to the U2RB register.

Table 22.6 Registers Used and Settings in UART Mode

Register	Bit	Function
U2TB	b0 to b8	Set transmit data. (1)
U2RB	b0 to b8	Receive data can be read. (1, 2)
	OER, FER, PER, SUM	Error flag
U2BRG	b0 to b7	Set the transfer rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit(s).
	PRY, PRYE	Select whether parity is included and whether odd or even.
	IOPOL	Select the polarities of the TXD/RXD input/output.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Select $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use the function.
	TXEPT	Transmit register empty flag
	CRD	Select the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function enabled or disabled.
	NCH	Select the output format of the TXD2 pin.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 or 9 bits long.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2RRM	Set to 0.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Select the digital filter disabled or enabled.
U2SMR5	MP	Set to 0.

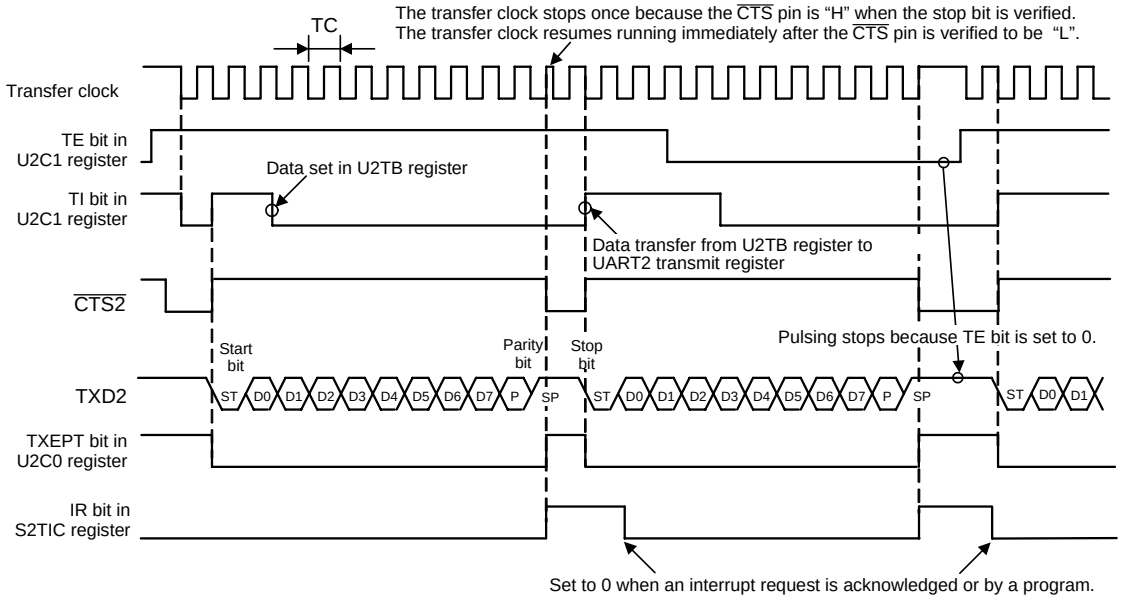
Notes:
1. The bits used for transmit/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits b7 and b8 when transfer data is 7 bits long
   - Bit b8 when transfer data is 8 bits long

Table 22.7 lists the I/O Pin Functions in UART Mode.
After UART2 operating mode is selected, the TXD2 pin outputs a high-level signal until transfer starts. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 22.7 shows the Transmit Timing in UART Mode. Figure 22.8 shows the Receive Timing in UART Mode.

Table 22.7 I/O Pin Functions in UART Mode

Pin Name	Function	Selection Method
TXD2 (P7_1, P7_2, or P8_5)	Serial data output	• When TXD2 (P7_1) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 01b (P7_1) When N-channel open-drain output is selected, PD7_1 bit in PD7 register = 0 • When TXD2 (P7_2) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 10b (P7_2) When N-channel open-drain output is selected, PD7_2 bit in PD7 register = 0 • When TXD2 (P8_5) Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 11b (P8_5) When N-channel open-drain output is selected, PD8_5 bit in PD8 register = 0 • For reception only: P7_1, P7_2 and P8_5 can be used as ports by setting TXD2SEL1 to TXD2SEL0 to 00b.
RXD2 (P7_1, P7_2, or P8_6)	Serial data input	• When RXD2 (P7_1) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 01b (P7_1) Bit PD7_1 in PD7 register = 0 RXD2 (P7_1, P7_2 or P8_6) • When RXD2 (P7_2) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 10b (P7_2) Bit PD7_2 in PD7 register = 0 • When RXD2 (P8_6) Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 11b (P8_6) Bit PD8_6 in PD8 register = 0 • For transmission only: P7_1, P7_2 and P8_6 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b.
CLK2 (P7_0 or P8_4)	I/O port	Bits CLK2SEL1 to CLK2SEL0 to U2SR1 register = 00b
	Transfer clock input	• When CLK2 (P7_0) Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 01b(P7_0) Bit CKDIR in U2MR register = 1 Bit PD7_0 in PD7 register = 0 • When CLK2 (P8_4) Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 10b (P8_4) Bit CKDIR in U2MR register = 1 Bit PD8_4 in PD8 register = 0
$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ (P7_3 or P8_7)	$\overline{\text{CTS}}$ input	• When $\overline{\text{CTS2}}$ (P7_3) Bits CTS2SEL1 to CTS2SEL0 in U2SR1 register = 01b (P7_3) Bit CRD in U2C0 register = 0 Bit CRS in U2C0 register = 0 Bit PD7_3 in PD7 register = 0 • When $\overline{\text{CTS2}}$ (P8_7) Bits CTS2SEL1 to CTS2SEL0 in U2SR1 register = 10b (P8_7) Bit CRD in U2C0 register = 0 Bit CRS in U2C0 register = 0 Bit PD8_7 in PD8 register = 0
	$\overline{\text{RTS}}$ output	• When $\overline{\text{RTS2}}$ (P7_3) Bits CTS2SEL1 to CTS2SEL0 register in U2SR1 register = 01b (P7_3) Bit CRD in U2C0 register = 0 Bit CRS in U2C0 register = 1 • When $\overline{\text{RTS2}}$ (P8_7) Bits CTS2SEL1 to CTS2SEL0 register in U2SR1 register = 10b (P8_7) Bit CRD in U2C0 register = 0 Bit CRS in U2C0 register = 1
	I/O port	Bits CTS2SEL1 to CTS2SEL0 in U2SR1 register = 00b

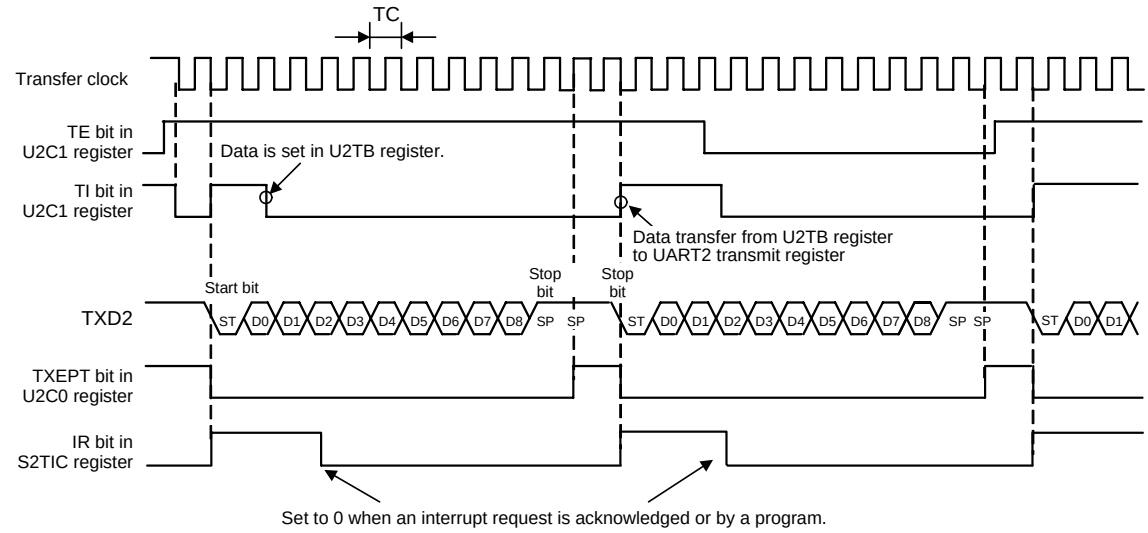
(1) Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)


TC
The transfer clock stops once because the CTS pin is "H" when the stop bit is verified.
The transfer clock resumes running immediately after the CTS pin is verified to be "L".
Transfer clock
TE bit in U2C1 register
Data set in U2TB register
TI bit in U2C1 register
Data transfer from U2TB register to UART2 transmit register
CTS2
Pulsing stops because TE bit is set to 0.
Start bit
Parity bit
Stop bit
TXD2
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP ST D0 D1 D2 D3 D4 D5 D6 D7 P SP ST D0 D1
TXEPT bit in U2C0 register
IR bit in S2TIC register
Set to 0 when an interrupt request is acknowledged or by a program.

The above applies under the following conditions:
- PRYE bit in U2MR register = 1 (parity enabled)
- STPS bit in U2MR register = 0 (one stop bit)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- U2IRS bit in U2C1 register = 1 (interrupt request generation when transmission is completed)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj: Frequency of U2BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U2BRG count source (external clock)
n: Value set in U2BRG register

(2) Transmit Timing Example When Transfer Data 9 Bits is Long (Parity Disabled, Two Stop Bits)


TC
Transfer clock
TE bit in U2C1 register
Data is set in U2TB register.
TI bit in U2C1 register
Data transfer from U2TB register to UART2 transmit register
Start bit
Stop bit
Stop bit
TXD2
ST D0 D1 D2 D3 D4 D5 D6 D7 D8 SP SP ST D0 D1 D2 D3 D4 D5 D6 D7 D8 SP SP ST D0 D1
TXEPT bit in U2C0 register
IR bit in S2TIC register
Set to 0 when an interrupt request is acknowledged or by a program.

The above applies under the following conditions:
- PRYE bit in U2MR register = 0 (parity disabled)
- STPS bit in U2MR register = 1 (two stop bits)
- CRD bit in U2C0 register = 1 (CTS/RTS function disabled)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj: Frequency of U2BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U2BRG count source (external clock)
n: Value set in U2BRG register

Figure 22.7 Transmit Timing in UART Mode

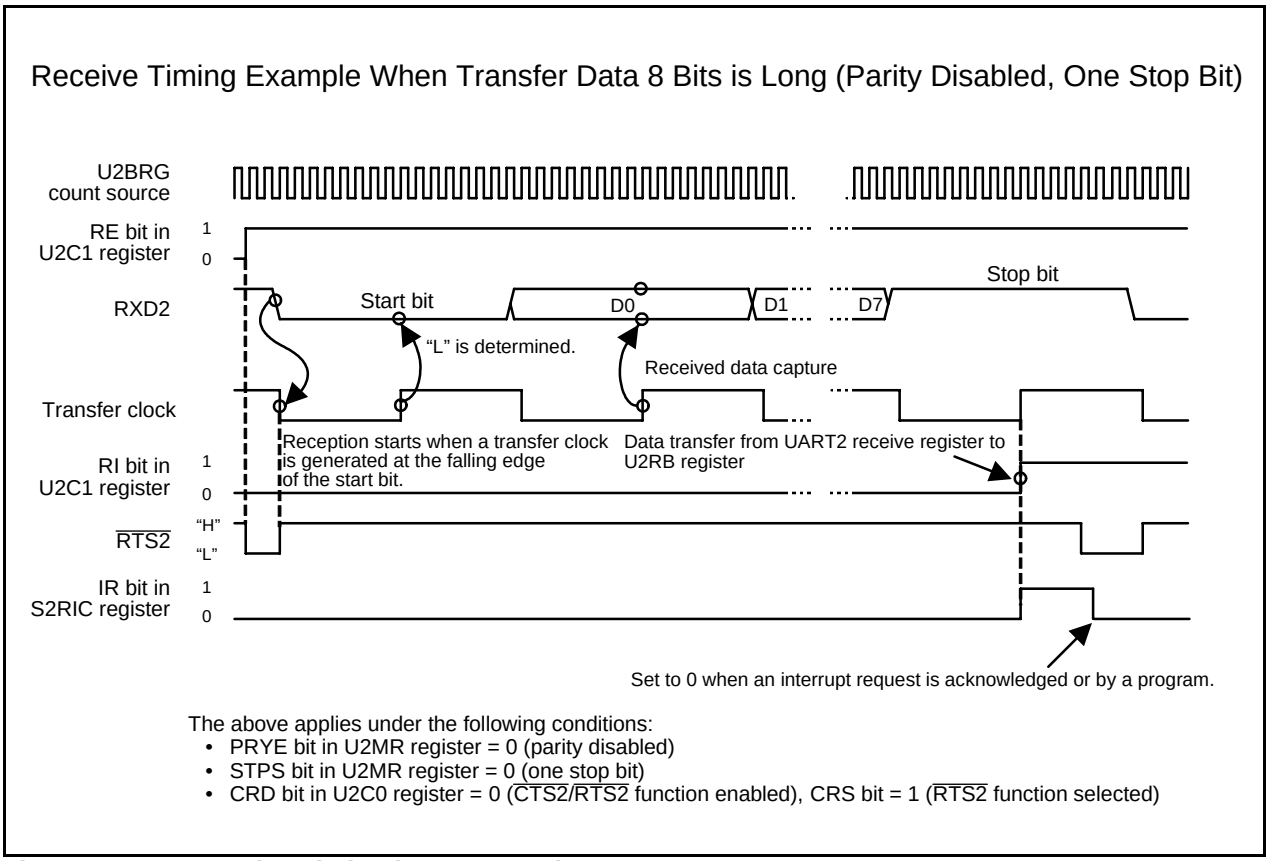

Receive Timing Example When Transfer Data 8 Bits is Long (Parity Disabled, One Stop Bit)
U2BRG count source
RE bit in U2C1 register
1
0
RXD2
Start bit
D0
D1
D7
Stop bit
"L" is determined.
Received data capture
Transfer clock
Reception starts when a transfer clock is generated at the falling edge of the start bit.
Data transfer from UART2 receive register to U2RB register
RI bit in U2C1 register
1
0
RTS2
"H"
"L"
IR bit in S2RIC register
1
0
Set to 0 when an interrupt request is acknowledged or by a program.
The above applies under the following conditions:
• PRYE bit in U2MR register = 0 (parity disabled)
• STPS bit in U2MR register = 0 (one stop bit)
• CRD bit in U2C0 register = 0 (CTS2/RTS2 function enabled), CRS bit = 1 (RTS2 function selected)

Figure 22.8 Receive Timing in UART Mode

22.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U2BRG register divided by 16. Table 22.8 lists the Bit Rate Setting Example in UART Mode (Internal Clock Selected).

Table 22.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	U2BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		U2BRG Setting Value	Actual Time (bps)	Setting Error (%)	U2BRG Setting Value	Actual Time (bps)	Setting Error (%)	U2BRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	—	—	—

Note:
1. For the high-speed on-chip oscillator, the correction value of the FR18S0 register should be written into the FRC0 register and the correction value of the FR18S1 register should be written into the FRC1 register. This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 001b (divide-by-2 mode).

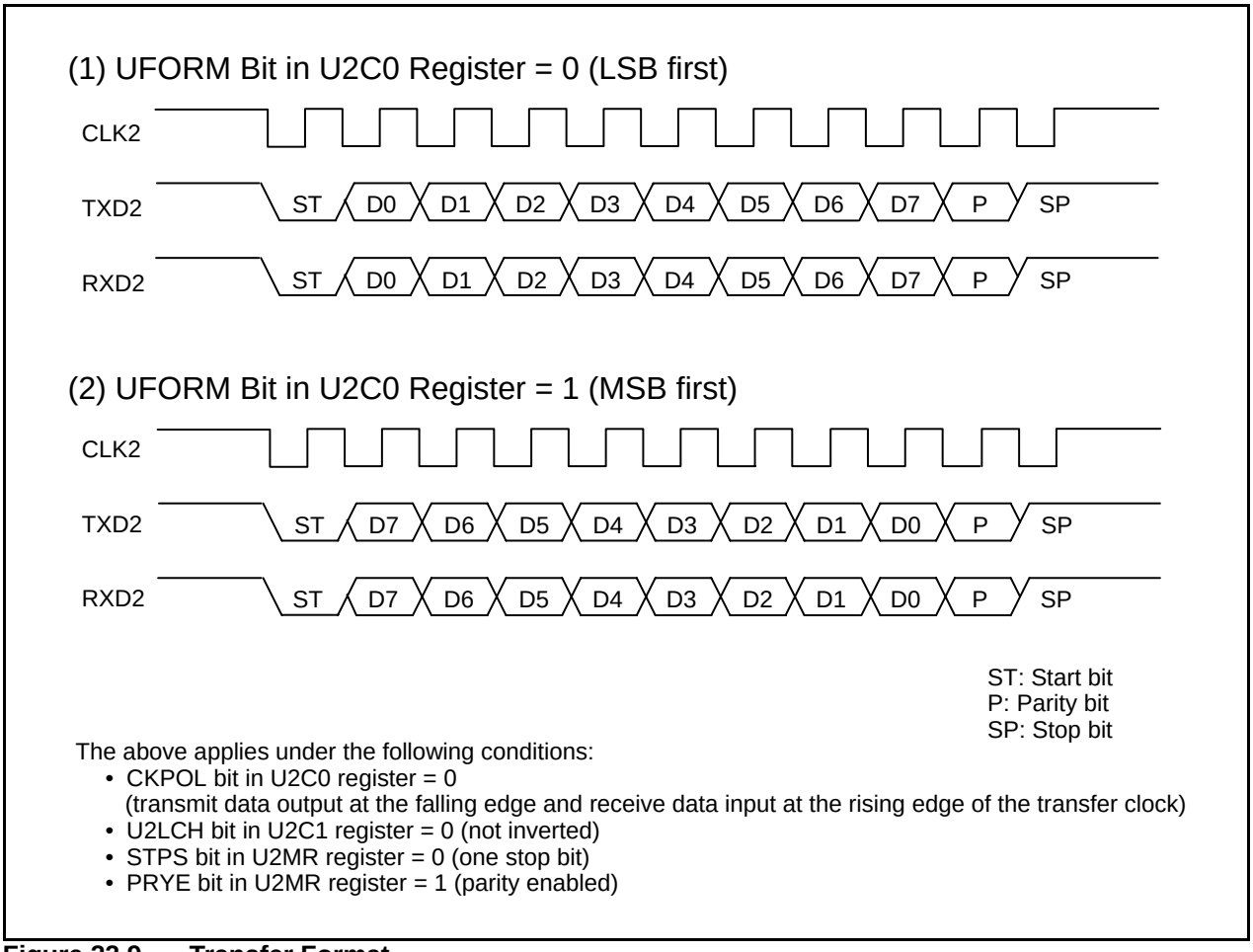
22.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

22.4.3 LSB First/MSB First Select Function

As shown in Figure 22.9, the UFORM bit in the U2C0 register can be used to select the transfer format. This function is enabled when transfer data is 8 bits long. Figure 22.9 shows the Transfer Format.


(1) UFORM Bit in U2C0 Register = 0 (LSB first)
CLK2
TXD2
RXD2
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP
(2) UFORM Bit in U2C0 Register = 1 (MSB first)
CLK2
TXD2
RXD2
ST D7 D6 D5 D4 D3 D2 D1 D0 P SP
ST: Start bit
P: Parity bit
SP: Stop bit

The above applies under the following conditions:
- CKPOL bit in U2C0 register = 0
  (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- U2LCH bit in U2C1 register = 0 (not inverted)
- STPS bit in U2MR register = 0 (one stop bit)
- PRYE bit in U2MR register = 1 (parity enabled)

Figure 22.9 Transfer Format

22.4.4 Serial Data Logic Switching Function

The data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 22.10 shows the Serial Data Logic Switching.

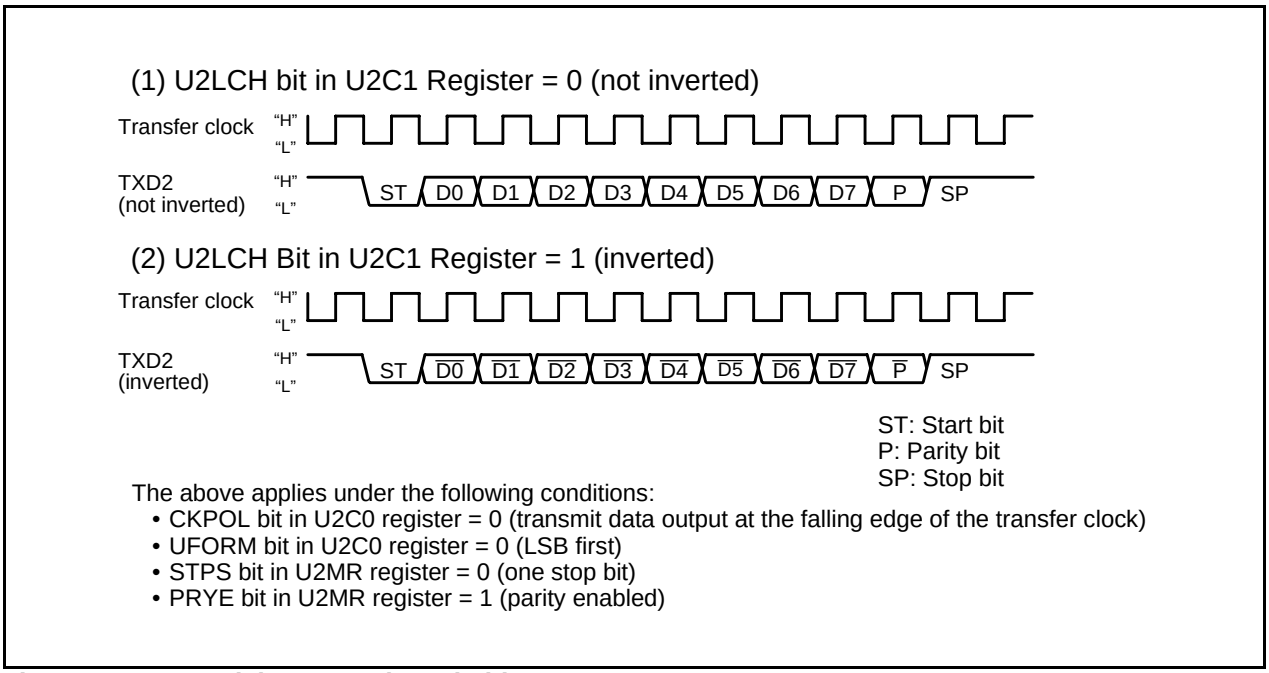

(1) U2LCH bit in U2C1 Register = 0 (not inverted)
Transfer clock
"H"
"L"
TXD2
(not inverted)
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP
(2) U2LCH Bit in U2C1 Register = 1 (inverted)
TXD2
(inverted)
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP
ST: Start bit
P: Parity bit
SP: Stop bit
The above applies under the following conditions:
• CKPOL bit in U2C0 register = 0 (transmit data output at the falling edge of the transfer clock)
• UFORM bit in U2C0 register = 0 (LSB first)
• STPS bit in U2MR register = 0 (one stop bit)
• PRYE bit in U2MR register = 1 (parity enabled)

Figure 22.10 Serial Data Logic Switching

22.4.5 TXD and RXD I/O Polarity Inverse Function

This function inverts the polarities of the TXD2 pin output and RXD2 pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted. Figure 22.11 shows the TXD and RXD I/O Inversion.

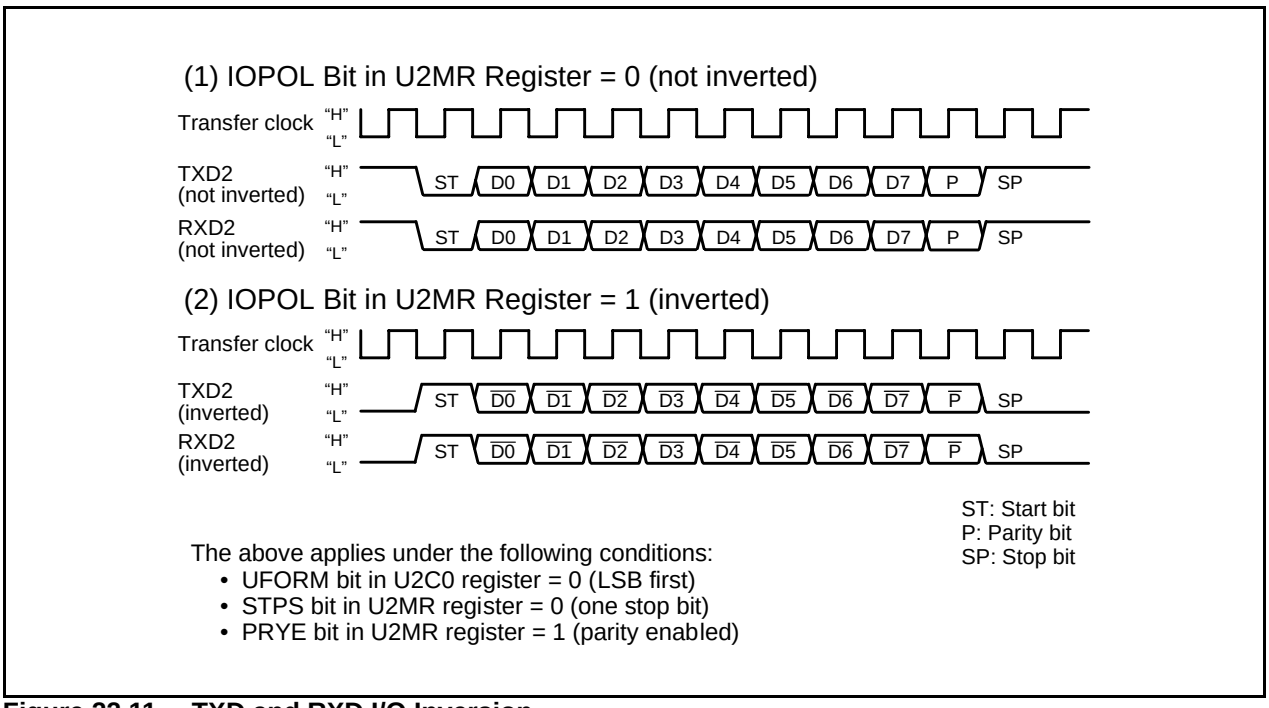

(1) IOPOL Bit in U2MR Register = 0 (not inverted)
Transfer clock
"H"
"L"
TXD2
(not inverted)
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP
RXD2
(not inverted)
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP
(2) IOPOL Bit in U2MR Register = 1 (inverted)
TXD2
(inverted)
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP
RXD2
(inverted)
ST D0 D1 D2 D3 D4 D5 D6 D7 P SP
ST: Start bit
P: Parity bit
SP: Stop bit
The above applies under the following conditions:
• UFORM bit in U2C0 register = 0 (LSB first)
• STPS bit in U2MR register = 0 (one stop bit)
• PRYE bit in U2MR register = 1 (parity enabled)

Figure 22.11 TXD and RXD I/O Inversion

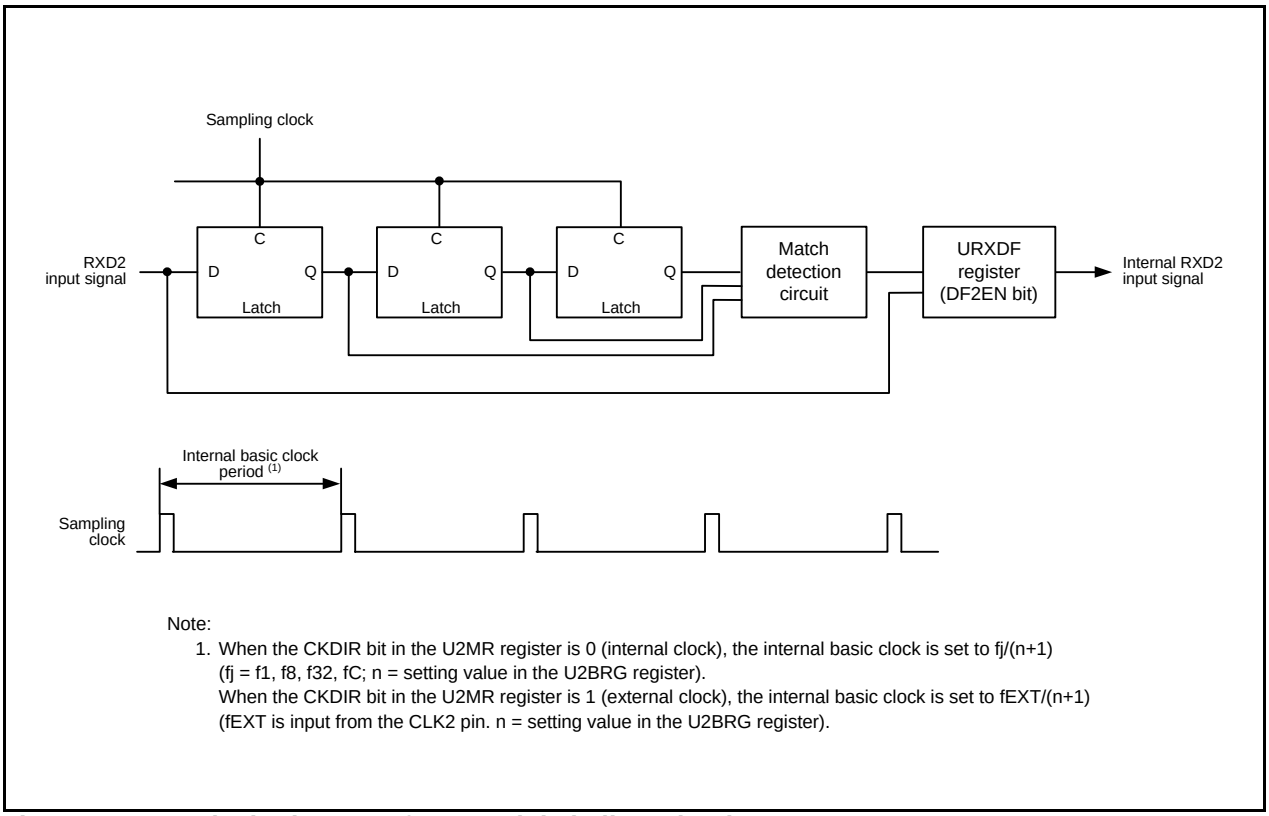
22.4.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit operation when a low-level signal is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the input level is switched to high during a transmit operation, the operation stops before the next data.
When the $\overline{\text{RTS}}$ function is used, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs a low-level signal when the MCU is ready for a receive operation.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

22.4.7 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise.
Figure 22.12 shows a Block Diagram of RXD2 Digital Filter Circuit.



Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1)
   (fj = f1, f8, f32, fC; n = setting value in the U2BRG register).
   When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1)
   (fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

Figure 22.12 Block Diagram of RXD2 Digital Filter Circuit

22.5 Special Mode 1 (I^2C Mode)

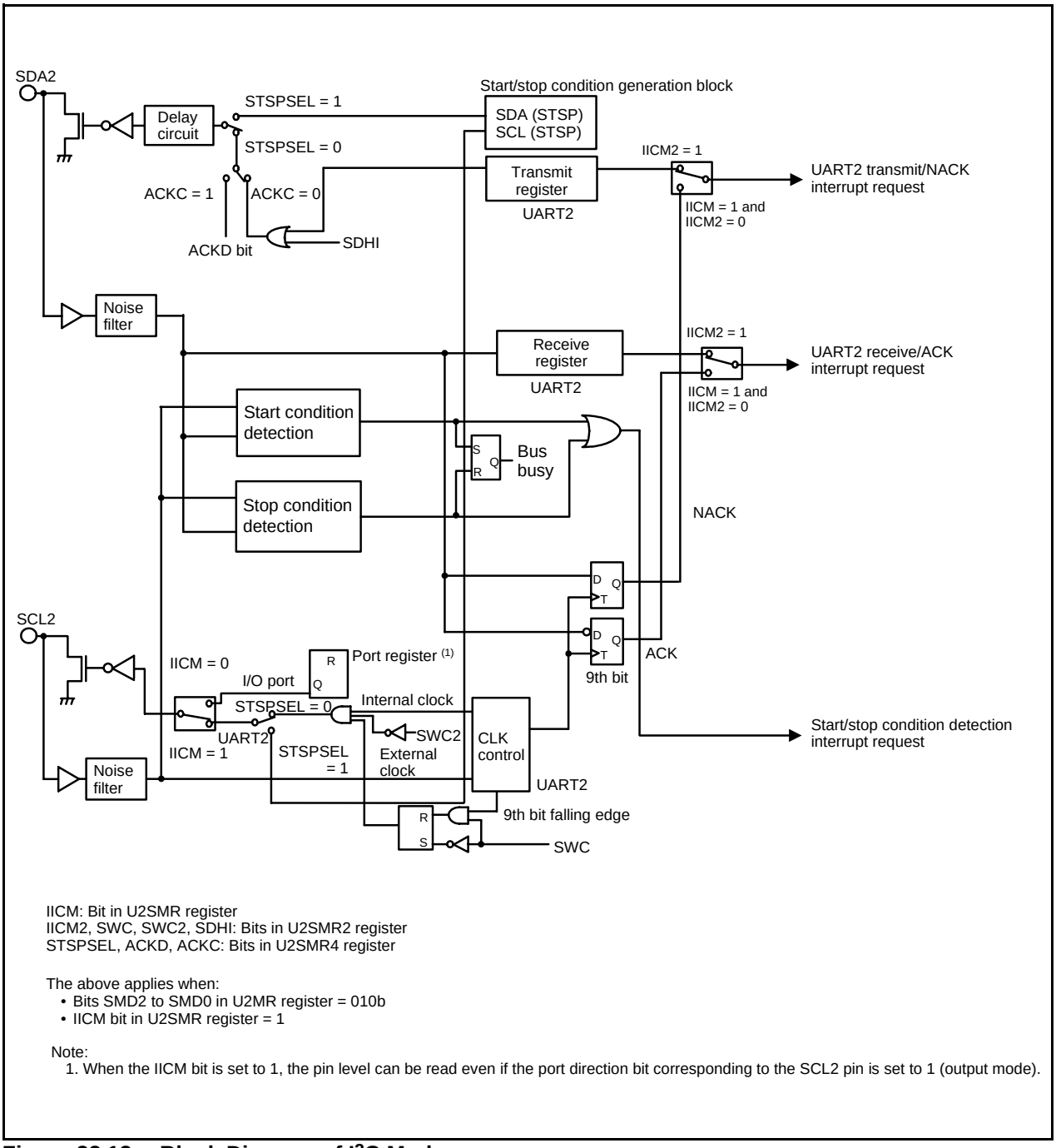
I^2C mode is provided for use as a simplified I^2C interface compatible mode. Table 22.9 lists the I^2C Mode Specifications. Tables 22.10 and 22.11 list the registers used in I^2C mode and the settings. Table 22.12 lists the I^2C Mode Functions, Figure 22.13 shows a Block Diagram of I^2C Mode, and Figure 22.14 shows the Transfer to U2RB Register and Interrupt Timing.

As shown in Table 22.12, the MCU is placed in I^2C mode by setting bits SMD2 to SMD0 to 010b and the IICM bit to 1. Because SDA2 transmit output has a delay circuit attached, SDA2 output does not change state until SCL2 goes low and remains stably low.

Table 22.9 I^2C Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• Master mode The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(2(n+1)) fj = f1, f8, f32, fC n = Value set in U2BRG register: 00h to FFh • Slave mode The CKDIR bit is set to 1 (external clock): Input from the SCL2 pin
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U2C1 register is set to 1 (reception enabled). • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
Interrupt request generation timing	Start/stop condition detection, no acknowledgement detection, or acknowledgement detection
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 8th bit of the next unit of data.
Selectable functions	• SDA2 digital delay No digital delay or a delay of 2 to 8 U2BRG count source clock cycles can be selected. • Clock phase setting With or without clock delay can be selected.

Notes:
1. If an external clock is selected, the requirements must be met while the external clock is held high.
2. If an overrun error occurs, the received data in the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.



IICM: Bit in U2SMR register
IICM2, SWC, SWC2, SDHI: Bits in U2SMR2 register
STSPSEL, ACKD, ACKC: Bits in U2SMR4 register

The above applies when:
- Bits SMD2 to SMD0 in U2MR register = 010b
- IICM bit in U2SMR register = 1

Note:
1. When the IICM bit is set to 1, the pin level can be read even if the port direction bit corresponding to the SCL2 pin is set to 1 (output mode).

Figure 22.13 Block Diagram of I²C Mode

Table 22.10 Registers Used and Settings in I²C Mode (1)

Register	Bit	Function	
		Master	Slave
U2TB (1)	b0 to b7	Set transmit data.	Set transmit data.
U2RB (1)	b0 to b7	Receive data can be read.	Receive data can be read.
	b8	ACK or NACK is set in this bit.	ACK or NACK is set in this bit.
	OER	Overrun error flag	Overrun error flag
U2BRG	b0 to b7	Set the transfer rate.	Disabled
U2MR (1)	SMD2 to SMD0	Set to 010b.	Set to 010b.
	CKDIR	Set to 0.	Set to 1.
	IOPOL	Set to 0.	Set to 0.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.	Disabled
	CRS	Disabled because CRD = 1.	Disabled because CRD = 1.
	TXEPT	Transmit register empty flag	Transmit register empty flag
	CRD	Set to 1.	Set to 1.
	NCH	Set to 1.	Set to 1.
	CKPOL	Set to 0.	Set to 0.
	UFORM	Set to 1.	Set to 1.
U2C1	TE	Set to 1 to enable transmission.	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set to 1 to enable reception.	Set to 1 to enable reception.
	RI	Reception complete flag	Reception complete flag
	U2IRS	Set to 1.	Set to 1.
	U2RRM, U2LCH, U2ERE	Set to 0.	Set to 0.
U2SMR	IICM	Set to 1.	Set to 1.
	BBS	Bus busy flag	Bus busy flag
	b3 to b7	Set to 0.	Set to 0.
U2SMR2	IICM2	Refer to **Table 22.12 I²C Mode Functions**.	Refer to **Table 22.12 I²C Mode Functions**.
	CSC	Set to 1 to enable clock synchronization.	Set to 0.
	SWC	Set to 1 to fix SCL2 output low at the falling edge of the 9th bit of clock.	Set to 1 to fix SCL2 output low at the falling edge of the 9th bit of clock.
	STAC	Set to 0.	Set to 1 to initialize UART2 at start condition detection.
	SWC2	Set to 1 to forcibly pull SCL2 output low.	Set to 1 to forcibly pull SCL2 output low.
	SDHI	Set to 1 to disable SDA2 output.	Set to 1 to disable SDA2 output.
	b7	Set to 0.	Set to 0.
U2SMR3	b0, b2, b4, NODC	Set to 0.	Set to 0.
	CKPH	Refer to **Table 22.12 I²C Mode Functions**.	Refer to **Table 22.12 I²C Mode Functions**.
	DL0 to DL2	Set the amount of SDA2 digital delay.	Set the amount of SDA2 digital delay.

Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in I²C mode.

Table 22.11 Registers Used and Settings in I²C Mode (2)

Register	Bit	Function	
		Master	Slave
U2SMR4	STAREQ	Set to 1 to generate a start condition.	Set to 0.
	RSTAREQ	Set to 1 to generate a restart condition.	Set to 0.
	STPREQ	Set to 1 to generate a stop condition.	Set to 0.
	STSPSEL	Set to 1 to output each condition.	Set to 0.
	ACKD	Select ACK or NACK.	Select ACK or NACK.
	ACKC	Set to 1 to output ACK data.	Set to 1 to output ACK data.
	SCLHI	Set to 1 to stop SCL2 output when a stop condition is detected.	Set to 0.
	SWC9	Set to 0.	Set to 1 to hold SCL2 low at the falling edge of the 9th bit of clock.
URXDF	DF2EN	Set to 0.	Set to 0.
U2SMR5	MP	Set to 0.	Set to 0.

Table 22.12 I²C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0 = 001b, IICM = 0)	I²C Mode (SMD2 to SMD0 = 010b, IICM = 1)			
		IICM2 = 0 (NACK/ACK interrupt)		IICM2 = 1 (UART transmit/receive interrupt)	
		CKPH = 0 (No Clock Delay)	CKPH = 1 (With Clock Delay)	CKPH = 0 (No Clock Delay)	CKPH = 1 (With Clock Delay)
Source of UART2 bus collision interrupt (1, 5)	—	Start condition detection or stop condition detection (Refer to **Table 22.13 STSPSEL Bit Functions**)			
Source of UART2 transmit/ NACK2 interrupt (1, 6)	UART2 transmission Transmission started or completed (selectable by U2IRS bit)	No acknowledgment detection (NACK) Rising edge of SCL2 9th bit		UART2 transmission Rising edge of SCL2 9th bit	UART2 transmission Falling edge of SCL2 next to 9th bit
Source of UART2 receive/ACK2 interrupt (1, 6)	UART2 reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK) Rising edge of SCL2 9th bit		UART2 reception Falling edge of SCL2 9th bit	
Timing for transferring data from UART receive shift register to U2RB register	CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Rising edge of SCL2 9th bit		Falling edge of SCL2 9th bit	Falling and rising edges of SCL2 9th bit
UART2 transmission output delay	No delay	With delay			
TXD2/SDA2 functions	TXD2 output	SDA2 I/O			
RXD2/SCL2 functions	RXD2 input	SCL2 I/O			
CLK2 function	CLK2 input or output port selected	— (Usable in I²C mode.)			
Noise filter width	15 ns	200 ns			
Read of RXD2 and SCL2 pin levels	Enabled when the corresponding port direction bit = 0	Enabled regardless of the content of the corresponding port direction bit.			
Initial value of TXD2 and SDA2 outputs	CKPOL = 0 (high) CKPOL = 1 (low)	The value set in the port register before setting I²C mode. (2)			
Initial and end values of SCL2	—	High	Low	High	Low
Storage of receive data	The 1st to 8th bits of the received data are stored in bits b0 to b7 in the U2RB register.	The 1st to 8th bits of the received data are stored in bits b7 to b0 in the U2RB register.		The 1st to 7th bits of the received data are stored in bits b6 to b0 in the U2RB register. 8th bit is stored in bit b8 in the U2RB register.	
					The 1st to 8th bits are stored in bits b7 to b0 in the U2RB register. (3)
Read of receive data	The U2RB register status is read.				Bits b6 to b0 in the U2RB register are read as bits b7 to b1. Bit b8 in the U2RB register is read as bit b0. (4)

Notes:
1. If the source of any interrupt is changed, the IR bit in the interrupt control register for the changed interrupt may inadvertently be set to 1 (interrupt requested). (Refer to **12.8 Notes on Interrupts**.)
   If one of the bits listed below is changed, the interrupt source, the interrupt timing, and others change. Always be sure to set the IR bit to 0 (interrupt not requested) after changing these bits:
   Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, and the CKPH bit in the U2SMR3 register.
2. Set the initial value of SDA2 output while bits SMD2 to SMD0 in the U2MR register are 000b (serial interface disabled).
3. Second data transfer to the U2RB register (rising edge of SCL2 9th bit)
4. First data transfer to the U2RB register (falling edge of SCL2 9th bit)
5. Refer to **Figure 22.16 STSPSEL Bit Functions**.
6. Refer to **Figure 22.14 Transfer to U2RB Register and Interrupt Timing**.

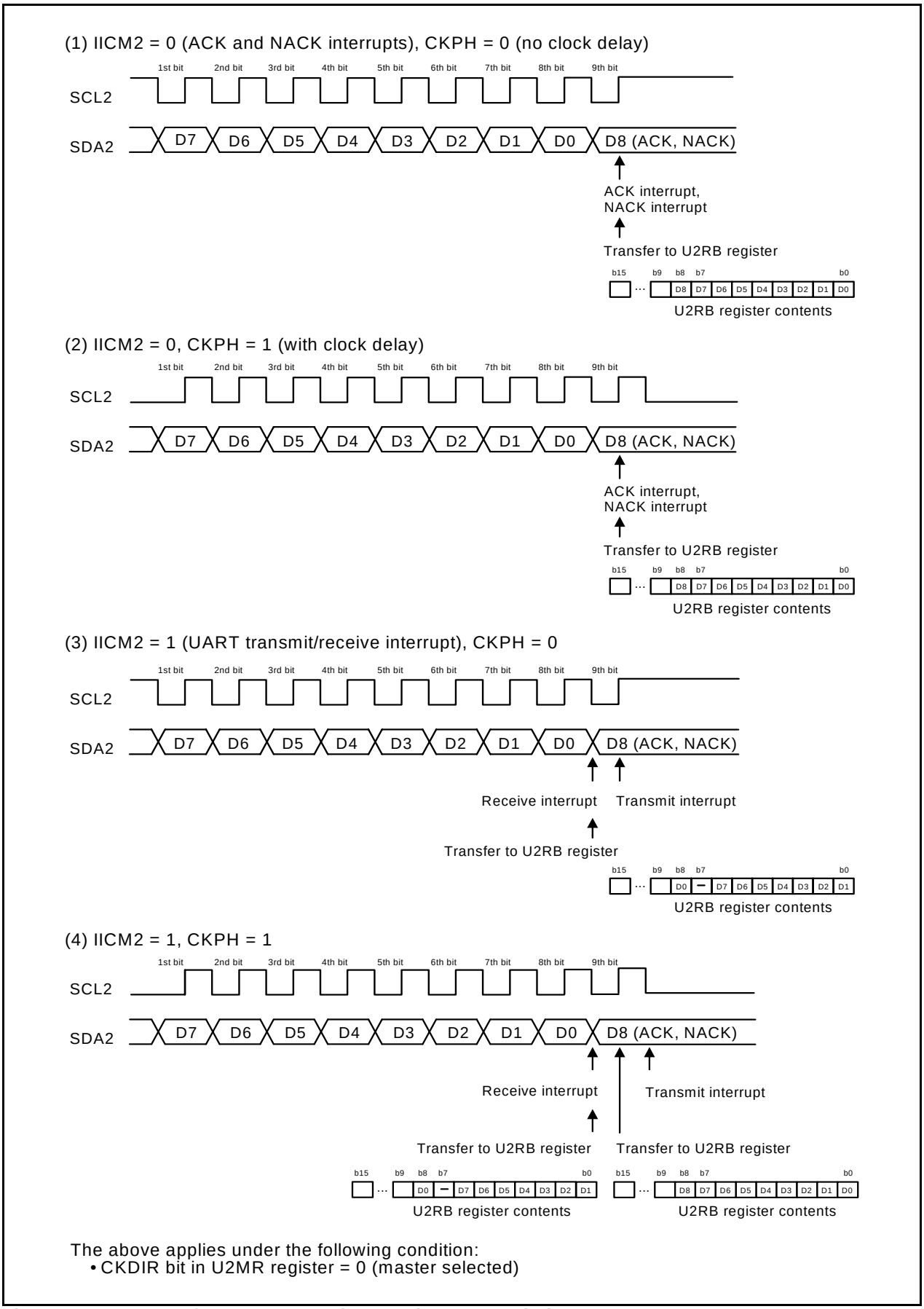

(1) IICM2 = 0 (ACK and NACK interrupts), CKPH = 0 (no clock delay)
1st bit 2nd bit 3rd bit 4th bit 5th bit 6th bit 7th bit 8th bit 9th bit
SCL2
SDA2
D7 D6 D5 D4 D3 D2 D1 D0 D8 (ACK, NACK)
ACK interrupt, NACK interrupt
Transfer to U2RB register
b15 b9 b8 b7 b0
D8 D7 D6 D5 D4 D3 D2 D1 D0
U2RB register contents
(2) IICM2 = 0, CKPH = 1 (with clock delay)
1st bit 2nd bit 3rd bit 4th bit 5th bit 6th bit 7th bit 8th bit 9th bit
SCL2
SDA2
D7 D6 D5 D4 D3 D2 D1 D0 D8 (ACK, NACK)
ACK interrupt, NACK interrupt
Transfer to U2RB register
b15 b9 b8 b7 b0
D8 D7 D6 D5 D4 D3 D2 D1 D0
U2RB register contents
(3) IICM2 = 1 (UART transmit/receive interrupt), CKPH = 0
1st bit 2nd bit 3rd bit 4th bit 5th bit 6th bit 7th bit 8th bit 9th bit
SCL2
SDA2
D7 D6 D5 D4 D3 D2 D1 D0 D8 (ACK, NACK)
Receive interrupt
Transmit interrupt
Transfer to U2RB register
b15 b9 b8 b7 b0
D0 – D7 D6 D5 D4 D3 D2 D1
U2RB register contents
(4) IICM2 = 1, CKPH = 1
1st bit 2nd bit 3rd bit 4th bit 5th bit 6th bit 7th bit 8th bit 9th bit
SCL2
SDA2
D7 D6 D5 D4 D3 D2 D1 D0 D8 (ACK, NACK)
Receive interrupt
Transmit interrupt
Transfer to U2RB register
Transfer to U2RB register
b15 b9 b8 b7 b0
D0 – D7 D6 D5 D4 D3 D2 D1
U2RB register contents
b15 b9 b8 b7 b0
D8 D7 D6 D5 D4 D3 D2 D1 D0
U2RB register contents
The above applies under the following condition:
• CKDIR bit in U2MR register = 0 (master selected)

Figure 22.14 Transfer to U2RB Register and Interrupt Timing

22.5.1 Detection of Start and Stop Conditions

Whether a start or a stop condition has been detected is determined.
A start condition detect interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition detect interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.
Because the start and stop condition detect interrupts share an interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.
Figure 22.15 shows the Detection of Start and Stop Conditions.

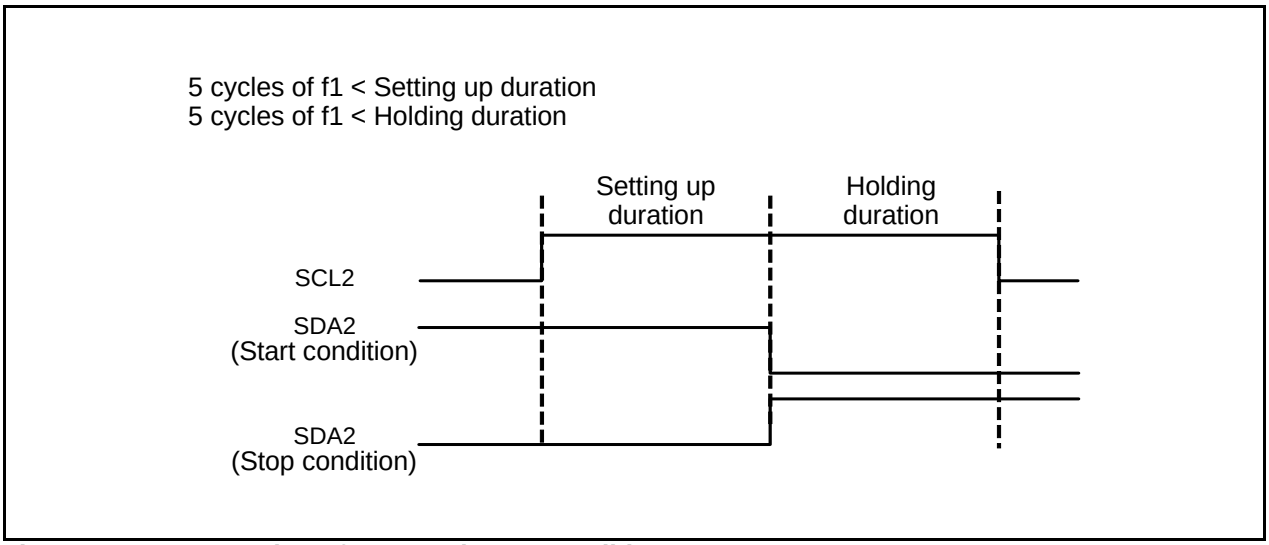


Figure 22.15 Detection of Start and Stop Conditions

22.5.2 Output of Start and Stop Conditions

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).
A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).
A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).

The output procedure is as follows:
(1) Set the STAREQ, RSTAREQ, or STPREQ bit to 1 (start).
(2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).
Table 22.13 lists the STSPSEL Bit Functions. Figure 22.16 shows the STSPSEL Bit Functions.

Table 22.13 STSPSEL Bit Functions

Function	STSPSEL = 0	STSPSEL = 1
SCL2/SDA2 pin output	Output of a transfer clock and data. Output of start/stop conditions is accomplished by a program using ports (no automatic generation by hardware)	Output of start/stop conditions according to bits STAREQ, RSTAREQ, and STPREQ
Start/stop condition interrupt request generation timing	Generation of start/stop conditions	Completion of start/stop condition generation

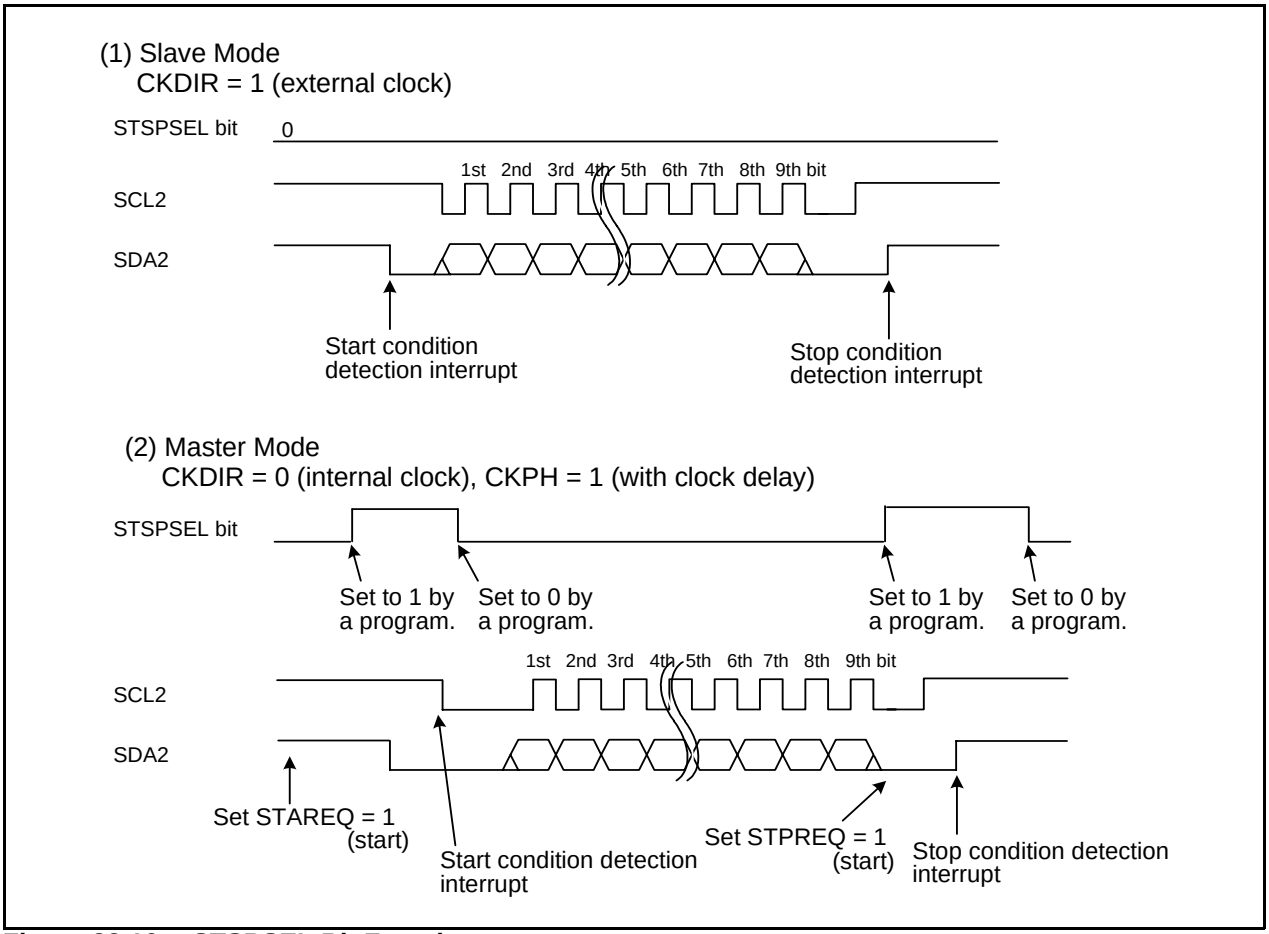

(1) Slave Mode
CKDIR = 1 (external clock)
STSPSEL bit
0
1st 2nd 3rd 4th 5th 6th 7th 8th 9th bit
SCL2
SDA2
Start condition detection interrupt
Stop condition detection interrupt
(2) Master Mode
CKDIR = 0 (internal clock), CKPH = 1 (with clock delay)
STSPSEL bit
Set to 1 by a program.
Set to 0 by a program.
Set to 1 by a program.
Set to 0 by a program.
1st 2nd 3rd 4th 5th 6th 7th 8th 9th bit
SCL2
SDA2
Set STAREQ = 1 (start)
Start condition detection interrupt
Set STPREQ = 1 (start)
Stop condition detection interrupt

Figure 22.16 STSPSEL Bit Functions

22.5.3 Transfer Clock

The transfer clock is used to transmit and receive data as is shown in **Figure 22.14 Transfer to U2RB Register and Interrupt Timing**.

The CSC bit in the U2SMR2 register is used to synchronize an internally generated clock (internal SCL2) and an external clock supplied to the SCL2 pin. When the CSC bit is set to 1 (clock synchronization enabled), if a falling edge on the SCL2 pin is detected while the internal SCL2 is high, the internal SCL2 goes low. The value of the U2BRG register is reloaded and counting of the low-level intervals starts. When the internal SCL2 changes state from low to high while the SCL2 pin is low, counting stops. When the SCL2 pin goes high, counting restarts. In this way, the UART2 transfer clock is equivalent to AND of the internal SCL2 and the clock signal applied to the SCL2 pin. The transfer clock works from a half cycle before the falling edge of the internal SCL2 1st bit to the rising edge of the 9th bit. To use this function, select an internal clock for the transfer clock.

The SWC bit in the U2SMR2 register can be used to select whether the SCL2 pin is fixed low or freed from low-level output at the falling edge of the 9th clock pulse.

If the SCLHI bit in the U2SMR4 register is set to 1 (enabled), SCL2 output is turned off (placed in the high impedance state) when a stop condition is detected.

Setting the SWC2 bit in the U2SMR2 register to 1 (low-level output) allows a low-level signal to be forcibly output from the SCL2 pin even during transmission or reception. Setting the SWC2 bit to 0 (transfer clock) allows the transfer clock to be output from or supplied to the SCL2 pin, instead of outputting a low-level signal.

If the SWC9 bit in the U2SMR4 register is set to 1 (SCL hold low enabled) when the CKPH bit in the U2SMR3 register is 1, the SCL2 pin is fixed low at the falling edge of the clock pulse next to the 9th. Setting the SWC9 bit to 0 (SCL hold low disabled) frees the SCL2 pin from low-level output.

22.5.4 SDA Output

The data written to bits b7 to b0 (D7 to D0) in the U2TB register is output in descending order from D7.

The 9th bit (D8) is ACK or NACK.

Set the initial value of SDA2 transmit output when IICM is set to 1 (I^2C mode) and bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled).

Bits DL2 to DL0 in the U2SMR3 register allow addition of no delays or a delay of two to eight U2BRG count source clock cycles to the SDA2 output.

Setting the SDHI bit in the U2SMR2 register to 1 (SDA output disabled) forcibly places the SDA2 pin in the high impedance state. Do not write to the SDHI bit at the rising edge of the UART2 transfer clock.

22.5.5 SDA Input

When the IICM2 bit is set to 0, the 1st to 8th bits (D7 to D0) of received data are stored in bits b7 to b0 in the U2RB register. The 9th bit (D8) is ACK or NACK.
When the IICM2 bit is set to 1, the 1st to 7th bits (D7 to D1) of received data are stored in bits b6 to b0 in the U2RB register and the 8th bit (D0) is stored in bit b8 in the U2RB register. Even when the IICM2 bit is set to 1, if the CKPH bit is 1, the same data as when the IICM2 bit is 0 can be read by reading the U2RB register after the rising edge of the 9th bit of the clock.

22.5.6 ACK and NACK

When the STSPSEL bit in the U2SMR4 register is set to 0 (start and stop conditions not output) and the ACKC bit in the U2SMR4 register is set to 1 (ACK data output), the value of the ACKD bit in the U2SMR4 register is output from the SDA2 pin.
When the IICM2 bit is set to 0, a NACK interrupt request is generated if the SDA2 pin remains high at the rising edge of the 9th bit of the transmit clock. An ACK interrupt request is generated if the SDA2 pin is low at the rising edge of the 9th bit of the transmit clock.

22.5.7 Initialization of Transmission/Reception

When a start condition is detected while the STAC bit is set to 1 (UART2 initialization enabled), the serial interface operates as described below.

- The transmit shift register is initialized, and the contents of the U2TB register are transferred to the transmit shift register. In this way, the serial interface starts sending data when the next clock pulse is applied. However, the UART2 output value does not change state and remains the same as when a start condition was detected until the first bit of data is output in synchronization with the input clock.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit is set to 1 (SCL wait output enabled). Consequently, the SCL2 pin is pulled low at the falling edge of the 9th clock.

Note that when UART2 transmission/reception is started using this function, the TI bit does not change state. Select the external clock as the transfer clock to start UART2 transmission/reception with this setting.

22.6 Multiprocessor Communication Function

When the multiprocessor communication function is used, data transmission/reception can be performed between a number of processors sharing communication lines by asynchronous serial communication, in which a multiprocessor bit is added to the data. For multiprocessor communication, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles; an ID transmission cycle for specifying the receiving station, and a data transmission cycle for the specified receiving station. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. When the multiprocessor bit is set to 1, the cycle is an ID transmission cycle; when the multiprocessor bit is set to 0, the cycle is a data transmission cycle. Figure 22.17 shows a Multiprocessor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A).
The transmitting station first sends the ID code of the receiving station to perform communication as communication data with a 1 multiprocessor bit added. It then sends transmit data as communication data with a 0 multiprocessor bit added.
When communication data in which the multiprocessor bit is 1 is received, the receiving station compares that data with its own ID. If they match, the data to be sent next is received. If they do not match, the receive station continues to skip communication data until data in which the multiprocessor bit is 1 is again received.

UART2 uses the MPIE bit in the U2SMR5 register to implement this function. When the MPIE bit is set to 1, data transfer from the UART2 receive register to the U2RB register, receive error detection, and the settings of the status flags, the RI bit in the U2C1 register, bits FER and OER in the U2RB register, are disabled until data in which the multiprocessor bit is 1 is received. On receiving a receive character in which the multiprocessor bit is 1, the MPRB bit in the U2RB register is set to 1 and the MPIE in the U2SMR5 register bit is set to 0, thus normal reception is resumed.

When the multiprocessor format is specified, the parity bit specification is invalid. All other bit settings are the same as those in normal asynchronous mode (UART mode). The clock used for multiprocessor communication is the same as that in normal asynchronous mode (UART mode).

Figure 22.18 shows a Block Diagram of Multiprocessor Communication Function.
Table 22.14 lists the Registers and Settings for Multiprocessor Communication Function.

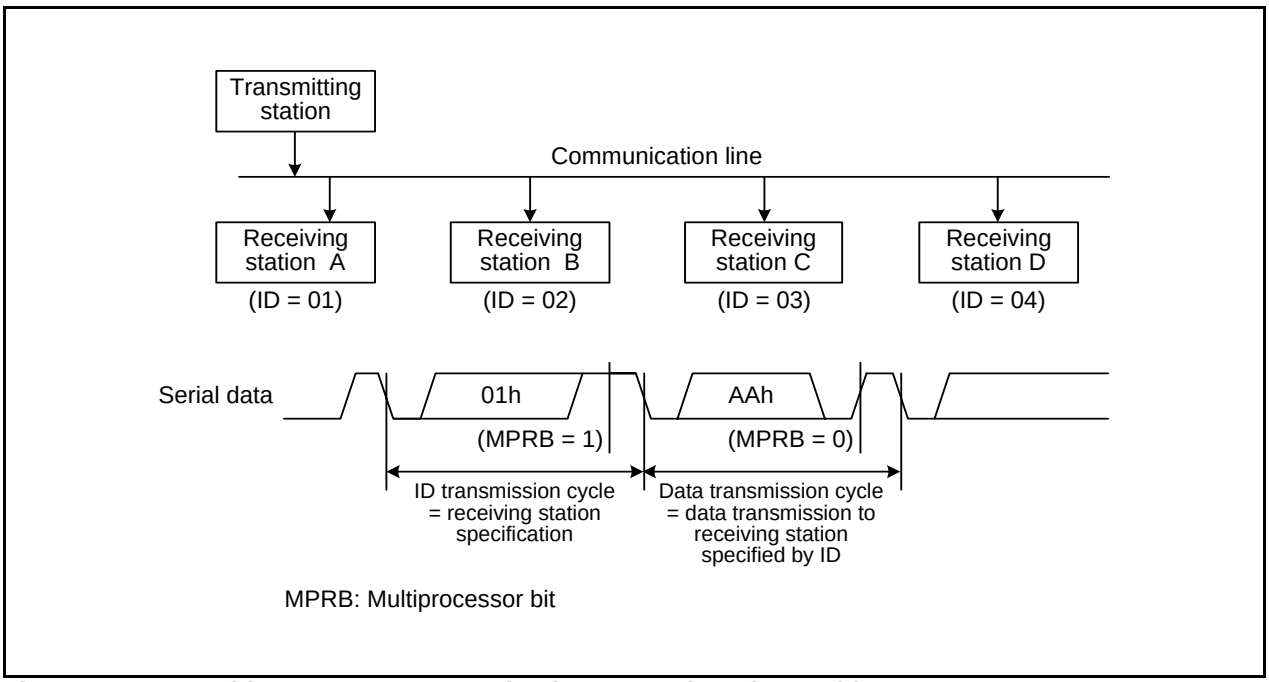
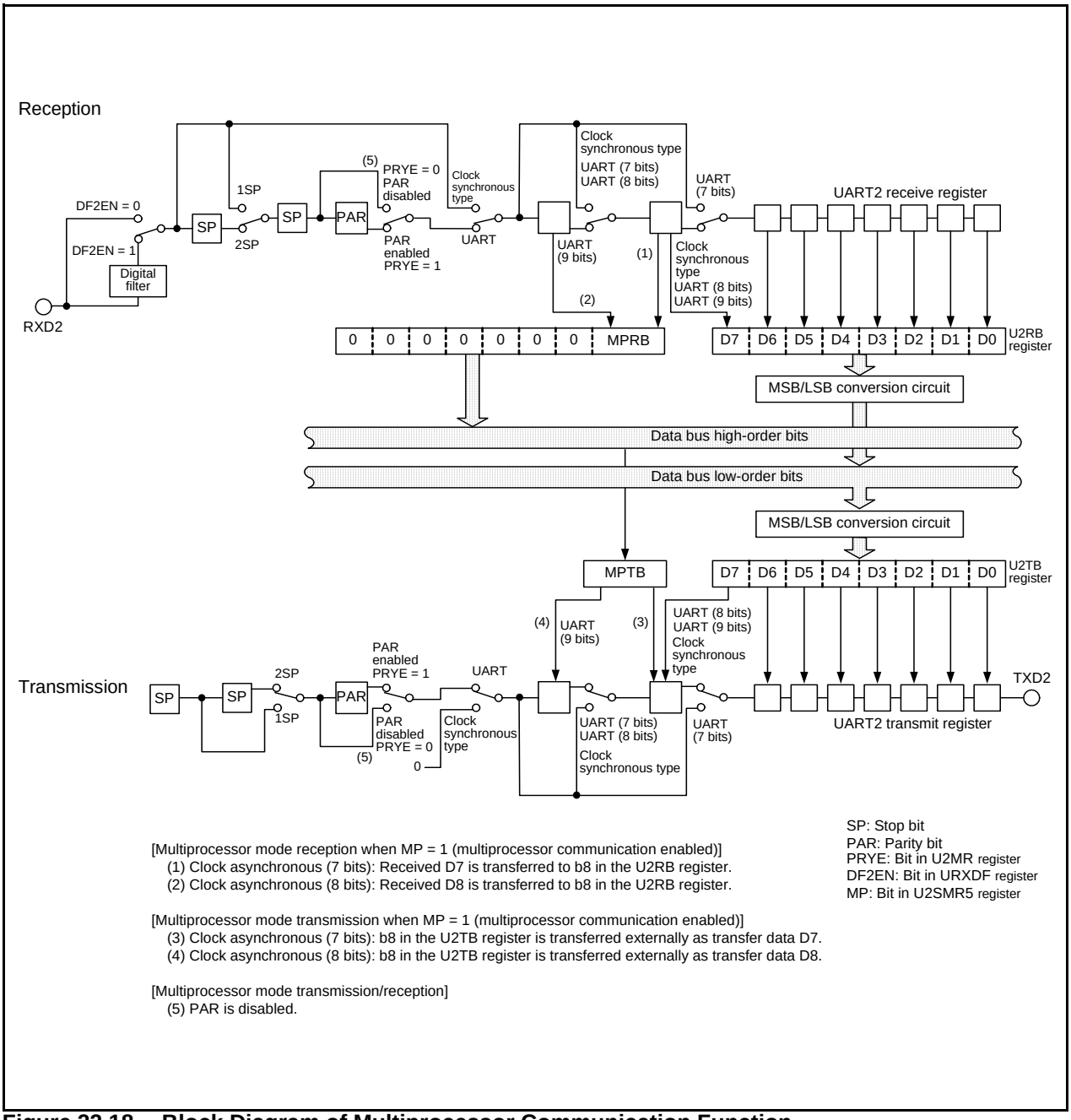


Figure 22.17 Multiprocessor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A)



SP: Stop bit
PAR: Parity bit
PRYE: Bit in U2MR register
DF2EN: Bit in URXDF register
MP: Bit in U2SMR5 register

[Multiprocessor mode reception when MP = 1 (multiprocessor communication enabled)]
(1) Clock asynchronous (7 bits): Received D7 is transferred to b8 in the U2RB register.
(2) Clock asynchronous (8 bits): Received D8 is transferred to b8 in the U2RB register.

[Multiprocessor mode transmission when MP = 1 (multiprocessor communication enabled)]
(3) Clock asynchronous (7 bits): b8 in the U2TB register is transferred externally as transfer data D7.
(4) Clock asynchronous (8 bits): b8 in the U2TB register is transferred externally as transfer data D8.

[Multiprocessor mode transmission/reception]
(5) PAR is disabled.

Figure 22.18 Block Diagram of Multiprocessor Communication Function

Table 22.14 Registers and Settings for Multiprocessor Communication Function

Register	Bit	Function
U2TB (1)	b0 to b7	Set transmit data.
	MPTB	Set to 0 or 1.
U2RB (2)	b0 to b7	Receive data can be read.
	MPRB	Multiprocessor bit
	OER, FER, SUM	Error flag
U2BRG	b0 to b7	Set the transfer rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long.
		Set to 101b when transfer data is 8 bits long.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit(s).
	PRY, PRYE	Parity detection function disabled
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the U2BRG count source.
	CRS	Function disabled because CRD = 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select the output format of the TXD2 pin.
	CKPOL	Set to 0.
	UFORM	Set to 0.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2LCH	Set to 0.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
U2SMR5	MP	Set to 1.
	MPIE	Set to 1.
URXDF	DF2EN	Select the digital filter enabled or disabled.

Notes:
1. Set the MPTB bit to 1 when the ID data frame is transmitted. Set this bit to 0 when the data frame is transmitted.
2. When the MPRB bit is set to 1, received D7 to D0 are ID fields. When this bit is set to 0, received D7 to D0 are data fields.

22.6.1 Multiprocessor Transmission

Figure 22.19 shows a Sample Flowchart of Multiprocessor Data Transmission. Set the MPBT bit in the U2TB register to 1 for ID transmission cycles. Set the MPBT bit in the U2TB register to 0 for data transmission cycles. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode).

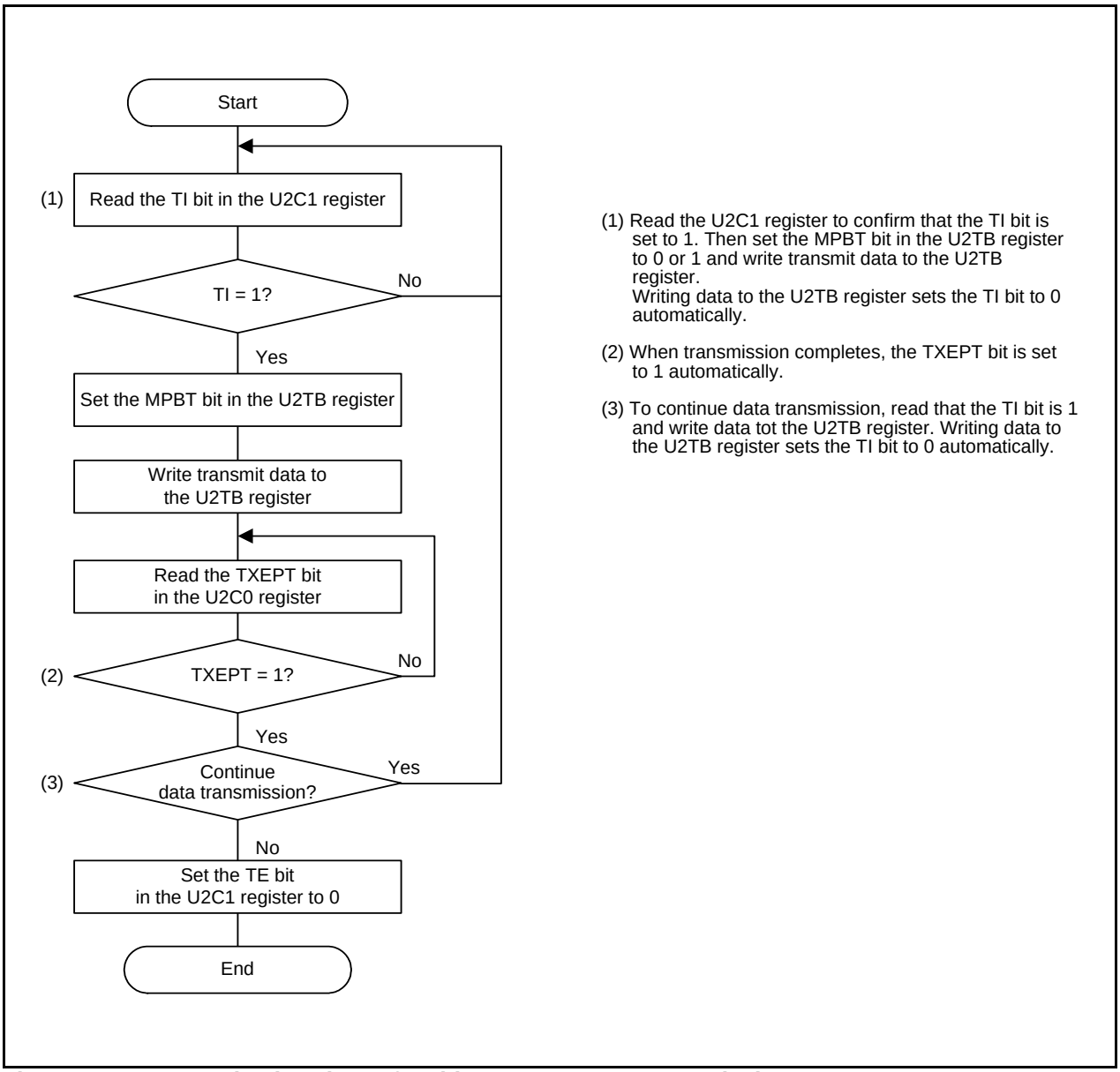

Start
(1)
Read the TI bit in the U2C1 register
TI = 1?
No
Yes
Set the MPBT bit in the U2TB register
Write transmit data to the U2TB register
Read the TXEPT bit in the U2C0 register
(2)
TXEPT = 1?
No
Yes
(3)
Continue data transmission?
Yes
No
Set the TE bit in the U2C1 register to 0
End
(1) Read the U2C1 register to confirm that the TI bit is set to 1. Then set the MPBT bit in the U2TB register to 0 or 1 and write transmit data to the U2TB register.
Writing data to the U2TB register sets the TI bit to 0 automatically.
(2) When transmission completes, the TXEPT bit is set to 1 automatically.
(3) To continue data transmission, read that the TI bit is 1 and write data tot the U2TB register. Writing data to the U2TB register sets the TI bit to 0 automatically.

Figure 22.19 Sample Flowchart of Multiprocessor Data Transmission

22.6.2 Multiprocessor Reception

Figure 22.20 shows a Sample Flowchart of Multiprocessor Data Reception. When the MPIE bit in the U2SMR5 register is set to 1, communication data is ignored until data in which the multiprocessor bit is 1 is received. Communication data with a 1 multiprocessor bit added is transferred to the U2RB register as receive data. At this time, a reception complete interrupt request is generated. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode). Figure 22.21 shows a Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One Stop Bit).

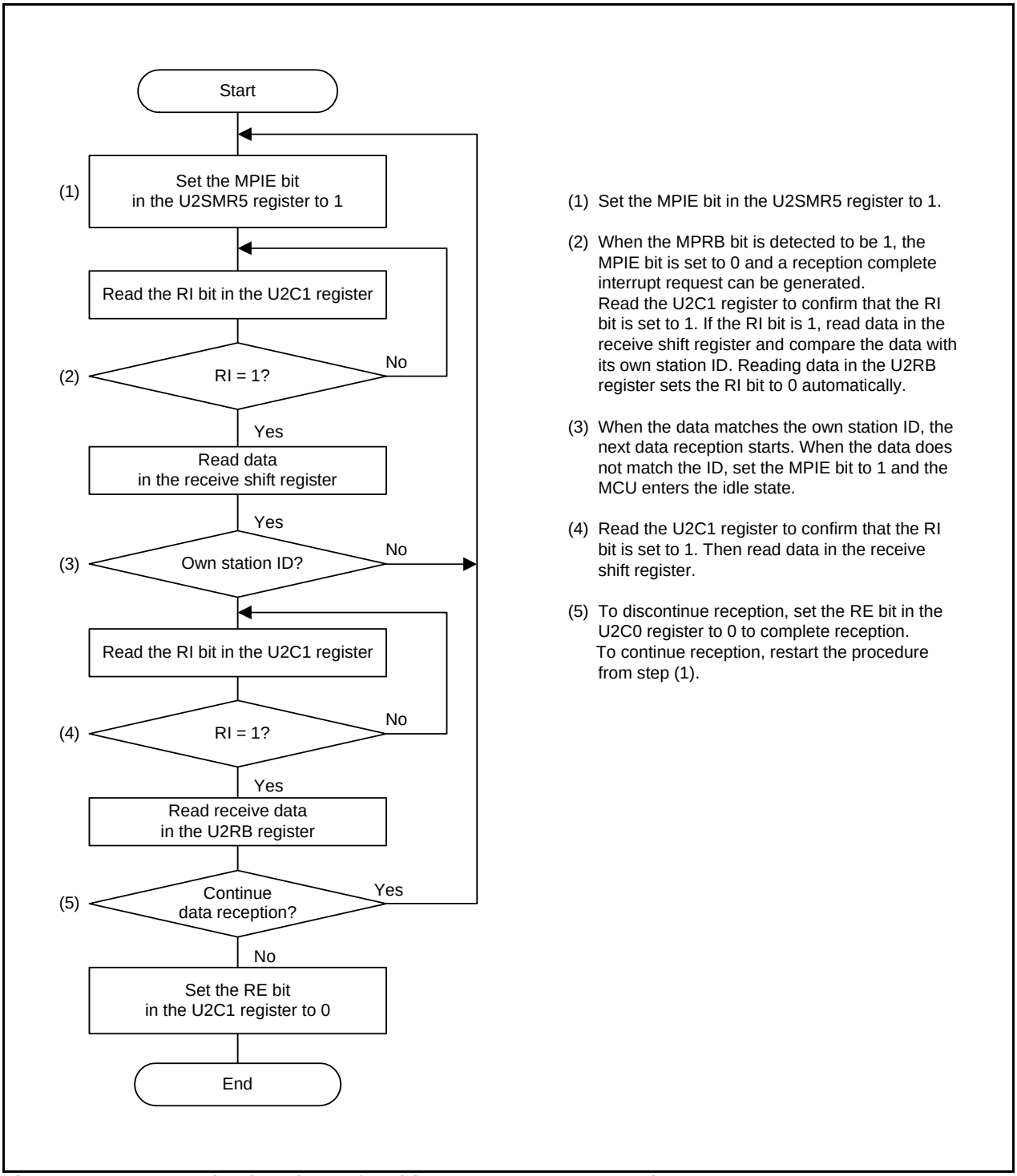

Start
(1)
Set the MPIE bit in the U2SMR5 register to 1
Read the RI bit in the U2C1 register
(2)
RI = 1?
No
Yes
Read data in the receive shift register
Yes
(3)
Own station ID?
No
Read the RI bit in the U2C1 register
(4)
RI = 1?
No
Yes
Read receive data in the U2RB register
(5)
Continue data reception?
Yes
No
Set the RE bit in the U2C1 register to 0
End
(1) Set the MPIE bit in the U2SMR5 register to 1.
(2) When the MPRB bit is detected to be 1, the MPIE bit is set to 0 and a reception complete interrupt request can be generated. Read the U2C1 register to confirm that the RI bit is set to 1. If the RI bit is 1, read data in the receive shift register and compare the data with its own station ID. Reading data in the U2RB register sets the RI bit to 0 automatically.
(3) When the data matches the own station ID, the next data reception starts. When the data does not match the ID, set the MPIE bit to 1 and the MCU enters the idle state.
(4) Read the U2C1 register to confirm that the RI bit is set to 1. Then read data in the receive shift register.
(5) To discontinue reception, set the RE bit in the U2C0 register to 0 to complete reception. To continue reception, restart the procedure from step (1).

Figure 22.20 Sample Flowchart of Multiprocessor Data Reception

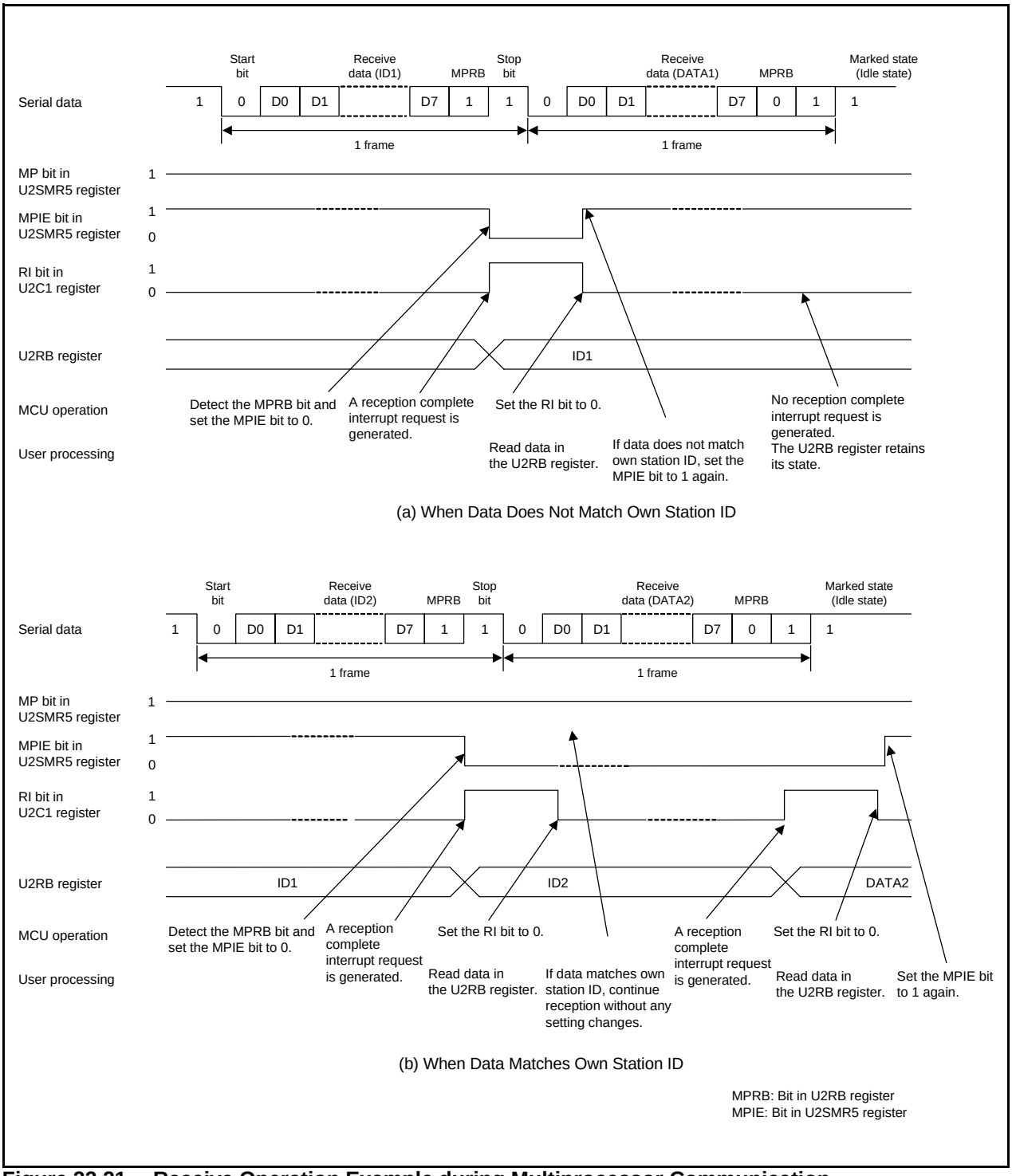
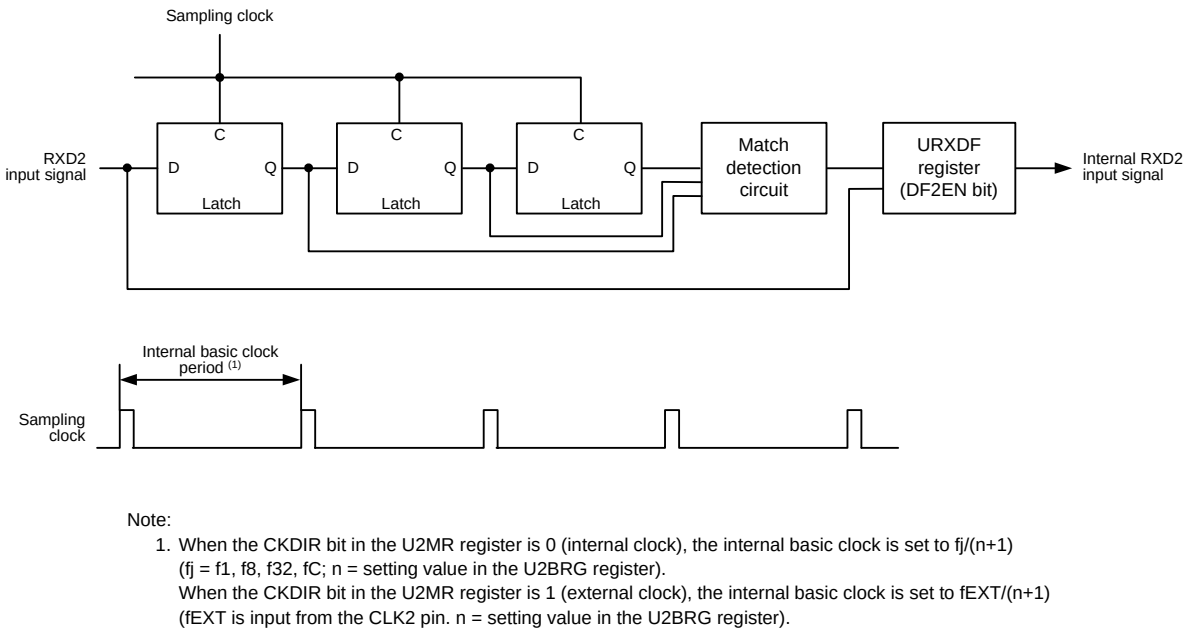

Start bit
Receive data (ID1)
MPRB
Stop bit
Receive data (DATA1)
MPRB
Marked state (Idle state)
Serial data
1 frame
1 frame
MP bit in U2SMR5 register
MPIE bit in U2SMR5 register
RI bit in U2C1 register
U2RB register
ID1
MCU operation
User processing
Detect the MPRB bit and set the MPIE bit to 0.
A reception complete interrupt request is generated.
Set the RI bit to 0.
Read data in the U2RB register.
If data does not match own station ID, set the MPIE bit to 1 again.
No reception complete interrupt request is generated.
The U2RB register retains its state.
(a) When Data Does Not Match Own Station ID
Start bit
Receive data (ID2)
MPRB
Stop bit
Receive data (DATA2)
MPRB
Marked state (Idle state)
Serial data
1 frame
1 frame
MP bit in U2SMR5 register
MPIE bit in U2SMR5 register
RI bit in U2C1 register
U2RB register
ID1
ID2
DATA2
MCU operation
User processing
Detect the MPRB bit and set the MPIE bit to 0.
A reception complete interrupt request is generated.
Set the RI bit to 0.
Read data in the U2RB register.
If data matches own station ID, continue reception without any setting changes.
A reception complete interrupt request is generated.
Set the RI bit to 0.
Read data in the U2RB register.
Set the MPIE bit to 1 again.
(b) When Data Matches Own Station ID
MPRB: Bit in U2RB register
MPIE: Bit in U2SMR5 register

Figure 22.21 Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One Stop Bit)

22.6.3 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise.
Figure 22.12 shows a Block Diagram of RXD2 Digital Filter Circuit.



Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1) (fj = f1, f8, f32, fC; n = setting value in the U2BRG register).
When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1) (fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

Figure 22.22 Block Diagram of RXD2 Digital Filter Circuit

22.7 Notes on Serial Interface (UART2)

22.7.1 Clock Synchronous Serial I/O Mode

22.7.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs a high-level signal when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

22.7.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register is set to 1 (transmission enabled).
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
- If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.

22.7.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmission even if the MCU is used for reception only. Dummy data is output from the TXD2 pin during reception.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and setting dummy data in the U2TB register. When an external clock is selected, the shift clock is generated by setting the TE bit to 1 (transmission enabled), setting dummy data in the U2TB register, and inputting an external clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register is set to 1 (reception enabled).
- The TE bit in the U2C1 register is set to 1 (transmission enabled).
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register).

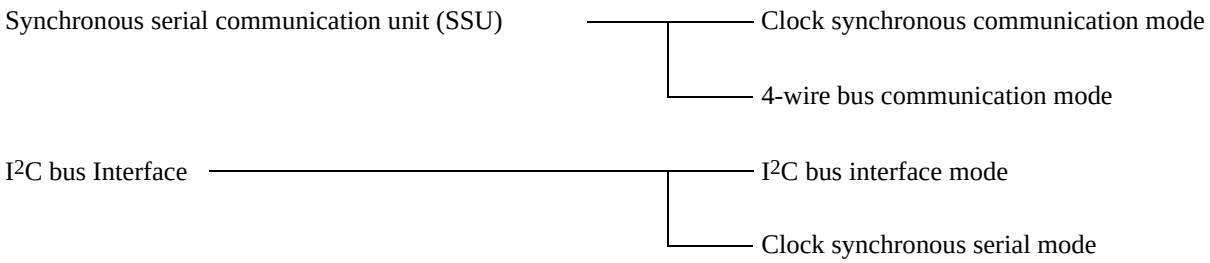
22.7.2 Special Mode 1 (I^2C Mode)

To generate start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than half cycle of the transfer clock before changing each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

23. Clock Synchronous Serial Interface

The clock synchronous serial interface is configured as follows.

Clock synchronous serial interface


Synchronous serial communication unit (SSU)
Clock synchronous communication mode
4-wire bus communication mode
I2C bus Interface
I2C bus interface mode
Clock synchronous serial mode

The clock synchronous serial interface uses the registers at addresses 0193h to 019Dh. Registers, bits, symbols, and functions vary even for the same addresses depending on the mode. Refer to the registers of each function for details. Also, the differences between clock synchronous communication mode and clock synchronous serial mode are the options of the transfer clock, clock output format, and data output format.

23.1 Mode Selection

The clock synchronous serial interface supports four modes.

Table 23.1 lists the Mode Selections. Refer to **24. Synchronous Serial Communication Unit (SSU)**, **25. I2C bus Interface** and the sections that follow for details of each mode.

Table 23.1 Mode Selections

IICSEL Bit in SSUIICSR Register	Bit 7 in 0198h (ICE Bit in ICCR1 Register)	Bit 0 in 019Dh (SSUMS Bit in SSMR2 Register, FS Bit in SAR Register)	Function	Mode
0	0	0	Synchronous serial communication unit	Clock synchronous communication mode
0	0	1		4-wire bus communication mode
1	1	0	I2C bus interface	I2C bus interface mode
1	1	1		Clock synchronous serial mode

24. Synchronous Serial Communication Unit (SSU)

The synchronous serial communication unit (SSU) supports clock synchronous serial data communication.

24.1 Introduction

Table 24.1 shows the Synchronous Serial Communication Unit Specifications. Figure 24.1 shows a Block Diagram of Synchronous Serial Communication Unit.

Table 24.1 Synchronous Serial Communication Unit Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 to 16 bits Continuous transmission and reception of serial data are enabled since both transmitter and receiver have buffer structures.
Operating modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication)
Master/slave device	Selectable
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin $\overline{\text{SSO}}$ (I/O): Data I/O pin $\overline{\text{SCS}}$ (I/O): Chip-select I/O pin
Transfer clocks	• When the MSS bit in the SSCRH register is set to 0 (operation as a slave device), an external clock is selected (input from the SSCK pin). • When the MSS bit in the SSCRH register is set to 1 (operation as the master device), an internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4, output from the SSCK pin) is selected. • The clock polarity and the phase of SSCK can be selected.
Receive error detection	• Overrun error An overrun error occurs during reception and completes in error. While the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and when the next serial data reception is completed, the ORER bit is set to 1.
Multimaster error detection	• Conflict error When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operation as the master device) and when starting a serial communication, the CE bit in the SSSR register is set to 1 if a low-level signal applies to the $\overline{\text{SCS}}$ pin input. When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operation as a slave device) and the $\overline{\text{SCS}}$ pin input changes state from low to high, the CE bit in the SSSR register is set to 1.
Interrupt requests	5 interrupt requests (transmit end, transmit data empty, receive data full, overrun error, and conflict error) (1).
Selectable functions	• Data transfer direction Selectable MSB first or LSB first • SSCK clock polarity Selectable a low or high level when the clock stops • SSCK clock phase Selectable edges for data change and data download

Note:
1. All sources use a single interrupt vector table for the synchronous serial communication unit.

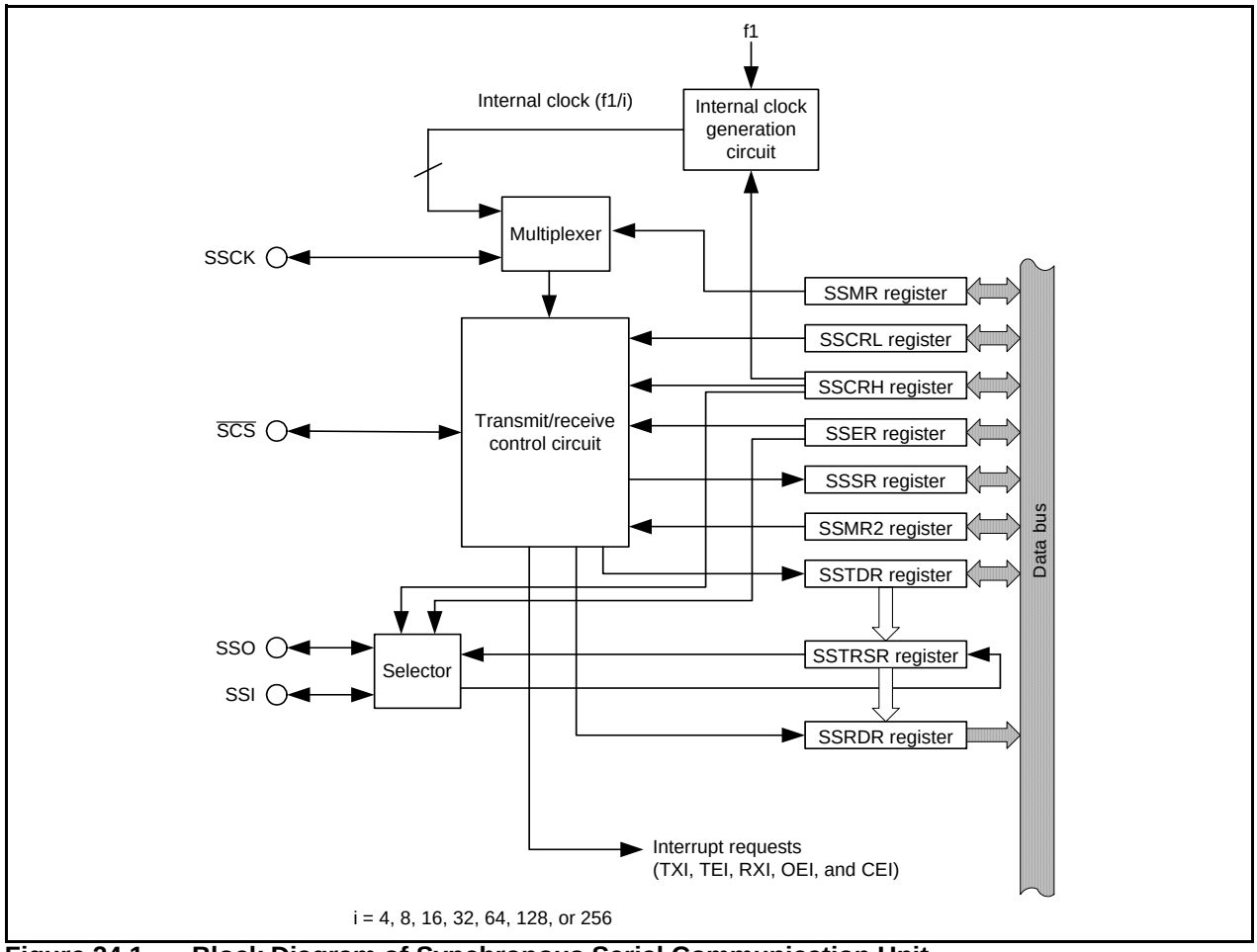


Figure 24.1 Block Diagram of Synchronous Serial Communication Unit

Table 24.2 Pin Configuration of Synchronous Serial Communication Unit

Pin Name	Assigned Pin	I/O	Function
SSI	P8_1, P6_2	I/O	Data I/O
$\overline{\text{SCS}}$	P8_0, P6_1	I/O	Chip-select signal I/O
SSCK	P8_2, P6_3	I/O	Clock I/O
SSO	P8_3, P6_4	I/O	Data I/O

24.2 Registers

24.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	MSTURT2	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	UART0 standby bit	0: Active 1: Standby (1)	R/W
b2	MSTURT2	UART2 standby bit	0: Active 1: Standby (2)	R/W
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (3)	R/W
b4	MSTLCD	LCD standby bit	0: Active 1: Standby (4)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (5)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	A/D standby bit (6)	0: Active 1: Standby	R/W

Notes:
1. When the MSTURT0 bit is set to 1 (standby), any access to the UART0 associated registers (addresses 00A0h to 00A7h) is disabled.
2. When the MSTURT2 bit is set to 1 (standby), any access to the timer UART2 associated registers (addresses 00A8h to 00BFh) is disabled.
3. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
4. When the MSTLCD bit is set to 1 (standby), any access to the timer LCD associated registers (addresses 0200h to 0237h) is disabled.
5. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
6. When the MSTADC bit is set to 1 (standby), any access to the timer A/D associated registers (addresses 00C0h to 00D9h, 00DCh to 00DFh) is disabled.
   Set the MSTADC bit to 0 (active) when the temperature sensor is used.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

24.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SSOSEL0	SCSSEL0	SSCKSEL0	SSISEL0	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I^{2}C bus switch bit	0: SSU function selected 1: I^{2}C bus function selected	R/W
b1	—	Reserved bits	Set to 0.	—
b2	—			
b3	—			
b4	SSISEL0	SSI pin select bit	0: P8_1 assigned 1: P6_2 assigned	R/W
b5	SSCKSEL0	SSCK/SCL pin select bit	0: P8_2 assigned 1: P6_3 assigned	R/W
b6	SCSSEL0	SCS pin select bit	0: P8_0 assigned 1: P6_1 assigned	R/W
b7	SSOSEL0	SSO/SDA pin select bit	0: P8_3 assigned 1: P6_4 assigned	R/W

24.2.3 SS Bit Counter Register (SSBR)

Address 0193h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	BS3	BS2	BS1	BS0
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BS0	SSU data transfer length set bit (1)	b3 b2 b1 b0 0 0 0 0: 16 bits 1 0 0 0: 8 bits 1 0 0 1: 9 bits 1 0 1 0: 10 bits 1 0 1 1: 11 bits 1 1 0 0: 12 bits 1 1 0 1: 13 bits 1 1 1 0: 14 bits 1 1 1 1: 15 bits	R/W
b1	BS1			R/W
b2	BS2			R/W
b3	BS3			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Note:
1. Do not write to bits BS0 to BS3 during SSU operation.

To set the SSBR register, set the RE bit in the SSER register to 0 (reception disabled) and the TE bit to 0 (transmission disabled).

Bits BS0 to BS3 (SSU Data Transfer Length Set Bit)

From 8 to 16 bits can be used as the SSU data transfer length.

24.2.4 SS Transmit Data Register (SSTDR)

Address 0195h to 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	This register stores transmit data. (1) When the SSTRSR register is detected as empty, the stored transmit data is transferred to the SSTRSR register and transmission starts. When the next transmit data is written to the SSTDR register during the data transmission from the SSTRSR register, continuous transmission is enabled. When the MLS bit in the SSMR register is set to 1 (transfer data with LSB first), the MSB-LSB inverted data is read after writing to the SSTDR register.	R/W

Note:
1. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSTDR register in 16-bit units.

24.2.5 SS Receive Data Register (SSRDR)

Address 0197h to 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	This register stores receive data. (1, 2) The receive data is transferred to the SSRDR register and the receive operation is completed when 1 byte of data has been received by the SSTRSR register. At this time, the next reception is enabled. Continuous reception is enabled using registers SSTRSR and SSRDR.	R

Notes:
1. When the ORER bit in the SSSR register is set to 1 (overrun error), the SSRDR register retains the data received before an overrun error occurs. When an overrun error occurs, the receive data is discarded.
2. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSRDR register in 16-bit units.

24.2.6 SS Control Register H (SSCRH)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RSSTP	MSS	—	—	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bit (1)	b2 b1 b0 0 0 0: f1/256 0 0 1: f1/128 0 1 0: f1/64 0 1 1: f1/32 1 0 0: f1/16 1 0 1: f1/8 1 1 0: f1/4 1 1 1: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	MSS	Master/slave device select bit (2)	0: Operation as a slave device 1: Operation as the master device	R/W
b6	RSSTP	Receive single stop bit (3)	0: Receive operation is continued after receiving 1 byte of data 1: Receive operation is completed after receiving 1 byte of data	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. The set clock is used when the MSS bit is set to 1 (operates as master device).
2. The SSCK pin functions as the transfer clock output pin when the MSS bit is set to 1 (operation as the master device). The MSS bit is set to 0 (operation as a slave device) when the CE bit in the SSSR register is set to 1 (conflict error occurs).
3. The RSSTP bit is disabled when the MSS bit is set to 0 (operation as a slave device).

24.2.7 SS Control Register L (SSCRL)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	SOL	SOLP	—	—	SRES	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	SRES	SSU control unit reset bit	When 1 is written to this bit, the SSU control unit and the SSTRSR register are reset. The value of the SSU internal register (1) is retained.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	—			
b4	SOLP	SOL write protect bit (2)	When 0 is written to this bit, the output level can be changed by the SOL bit. The SOLP bit remains unchanged even if 1 is written to it. When read, the content is 1.	R/W
b5	SOL	Serial data output value setting bit	When read 0: Serial data output is low 1: Serial data output is high When written (2, 3) 0: Data output is low 1: Data output is high	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Registers SSBR, SSCRH, SSCRL, SSMR, SSER, SSSR, SSMR2, SSTDR, and SSRDR.
2. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained.
   If the content of the SOL bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output.
   When writing to the SOL bit, set the SOLP bit to 0 and the SOL bit to 0 or 1 simultaneously by the MOV instruction.
3. Do not write to the SOL bit during data transfer.

24.2.8 SS Mode Register (SSMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counter 3 to 0	b3 b2 b1 b0 0 0 0 0: 16 bits left 0 0 0 1: 1 bit left 0 0 1 0: 2 bits left 0 0 1 1: 3 bits left 0 1 0 0: 4 bits left 0 1 0 1: 5 bits left 0 1 1 0: 6 bits left 0 1 1 1: 7 bits left 1 0 0 0: 8 bits left 1 0 0 1: 9 bits left 1 0 1 0: 10 bits left 1 0 1 1: 11 bits left 1 1 0 0: 12 bits left 1 1 0 1: 13 bits left 1 1 1 0: 14 bits left 1 1 1 1: 15 bits left	R
b1	BC1			R
b2	BC2			R
b3	BC3			R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	CPHS	SSCK clock phase select bit (1)	0: Data change at odd edges (Data download at even edges) 1: Data change at even edges (Data download at odd edges)	R/W
b6	CPOS	SSCK clock polarity select bit (1)	0: High when clock stops 1: Low when clock stops	R/W
b7	MLS	MSB first/LSB first select bit	0: Transfer data with MSB first 1: Transfer data with LSB first	R/W

Note:

1. Refer to **24.3.1.1 Association between Transfer Clock Polarity, Phase, and Data** for the settings of bits CPHS and CPOS.
   When the SSUMS bit in the SSMR2 register is set to 0 (clock synchronous communication mode), set the CPHS bit to 0 and the CPOS bit to 0.

24.2.9 SS Enable Register (SSER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE	RE	—	—	CEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE	Conflict error interrupt enable bit	0: Conflict error interrupt request disabled 1: Conflict error interrupt request enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b4	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt requests disabled 1: Receive data full and overrun error interrupt requests enabled	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

24.2.10 SS Status Register (SSSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	—	—	ORER	—	CE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE	Conflict error flag (1)	0: No conflict error 1: Conflict error (2)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	ORER	Overrun error flag (1)	0: No overrun error 1: Overrun error (3)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	RDRF	Receive data register full flag (1, 4)	0: No data in the SSRDR register 1: Data in the SSRDR register	R/W
b6	TEND	Transmit end flag (1, 5)	0: TDRE bit is set to 0 when transmitting the last bit of transmit data 1: TDRE bit is set to 1 when transmitting the last bit of transmit data	R/W
b7	TDRE	Transmit data empty flag (1, 5, 6)	0: No data transferred from registers SSTDR to SSTRSR 1: Data transferred from registers SSTDR to SSTRSR	R/W

Notes:

1. Writing 1 to the CE, ORER, RDRF, TEND, or TDRE bit is disabled. To set any of these bits to 0, first read 1 then write 0.
2. When the serial communication is started while the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operation as the master device), the CE bit is set to 1 if a low-level signal is applied to the $\overline{SCS}$ pin input. Refer to **24.5.4 SCS Pin Control and Arbitration** for more information.
   When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operation as a slave device) and the $\overline{SCS}$ pin input changes the level from low to high during transfer, the CE bit is set to 1.
3. Indicates when an overrun error occurs during reception and completes in error. If the next serial data receive operation is completed while the RDRF bit is set to 1 (data in the SSRDR register), the ORER bit is set to 1.
   After the ORER bit is set to 1 (overrun error), receive operation is disabled while the bit remains 1. Transmit operation is also disabled while the MSS bit is set to 1 (operation as the master device).
4. The RDRF bit is set to 0 when reading the data from the SSRDR register.
5. Bits TEND and TDRE are set to 0 when writing data to the SSTDR register.
6. The TDRE bit is set to 1 when the TE bit in the SSER register is set to 1 (transmission enabled).

To access the SSSR register successively, insert one or more NOP instructions between the instructions used for access.

24.2.11 SS Mode Register 2 (SSMR2)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BIDE	SCKS	CSS1	CSS0	SCKOS	SOOS	CSOS	SSUMS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SSUMS	SSU mode select bit (1)	0: Clock synchronous communication mode 1: 4-wire bus communication mode	R/W
b1	CSOS	$\overline{SCS}$ pin open-drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b2	SOOS	Serial data open-drain output select bit (1)	0: CMOS output (5) 1: N-channel open-drain output	R/W
b3	SCKOS	SSCK pin open-drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b4	CSS0	$\overline{SCS}$ pin select bit (2)	b5 b4 0 0: Function as a port 0 1: Function as the $\overline{SCS}$ input pin 1 0: Function as the $\overline{SCS}$ output pin (3) 1 1: Function as the $\overline{SCS}$ output pin (3)	R/W
b5	CSS1			R/W
b6	SCKS	SSCK pin select bit	0: Function as a port 1: Function as the serial clock pin	R/W
b7	BIDE	Bidirectional mode enable bit (1, 4)	0: Standard mode (communication using 2 pins of data input and data output) 1: Bidirectional mode (communication using 1 pin of data input and data output)	R/W

Notes:
1. Refer to **24.3.2.1 Association between Data I/O Pins and SS Shift Register** for information on the combinations of data I/O pins.
2. The $\overline{SCS}$ pin functions as a port, regardless of the values of bits CSS0 and CSS1 when the SSUMS bit is set to 0 (clock synchronous communication mode).
3. This bit functions as the $\overline{SCS}$ input pin before starting transfer.
4. The BIDE bit is disabled when the SSUMS bit is set to 0 (clock synchronous communication mode).
5. When the SOOS bit is set to 0 (CMOS output), set the port direction register bits corresponding to pins SSI and SSO to 0 (input mode).

24.3 Common Items for Multiple Modes

24.3.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.

To use the synchronous serial communication unit, set the SCKS bit in the SSMR2 register to 1 and select the SSCK pin as the serial clock pin.

When the MSS bit in the SSCRH register is set to 1 (operation as the master device), an internal clock can be selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs a clock at the transfer rate selected by bits CKS0 to CKS2 in the SSCRH register.

When the MSS bit in the SSCRH register is set to 0 (operation as a slave device), an external clock can be selected and the SSCK pin functions as input.

24.3.1.1 Association between Transfer Clock Polarity, Phase, and Data

The association between the transfer clock polarity, phase, and data changes according to the combination of the SSUMS bit in the SSMR2 register and bits CPHS and CPOS in the SSMR register.

Figure 24.2 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.

Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SSMR register. When the MLS bit is set to 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is set to 0, transfer is started from the MSB and proceeds to the LSB.

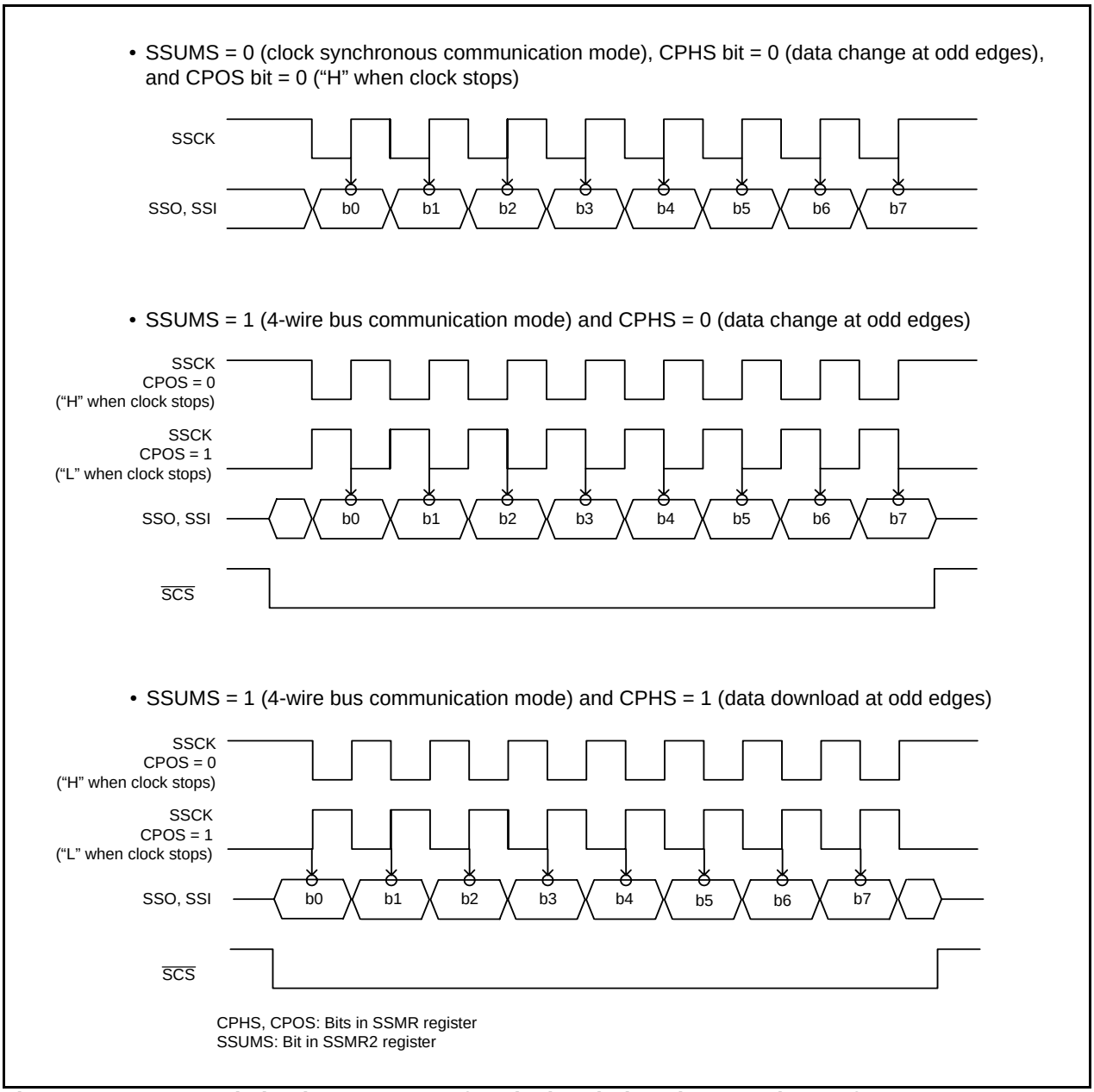


Figure 24.2 Association between Transfer Clock Polarity, Phase, and Transfer Data

24.3.2 SS Shift Register (SSTRSR)

The SSTRSR register is a shift register for transmitting and receiving serial data.
When transmit data is transferred from the SSTDR register to the SSTRSR register and the MLS bit in the SSMR register is set to 0 (MSB first), bit 0 in the SSTDR register is transferred to bit 0 in the SSTRSR register. When the MLS bit is set to 1 (LSB first), bit 7 in the SSTDR register is transferred to bit 0 in the SSTRSR register.

24.3.2.1 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and the SSTRSR register (SS shift register) changes according to a combination of the MSS bit in the SSCRH register and the SSUMS bit in the SSMR2 register. The connection also changes according to the BIDE bit in the SSMR2 register.
Figure 24.3 shows the Association between Data I/O Pins and SSTRSR Register.

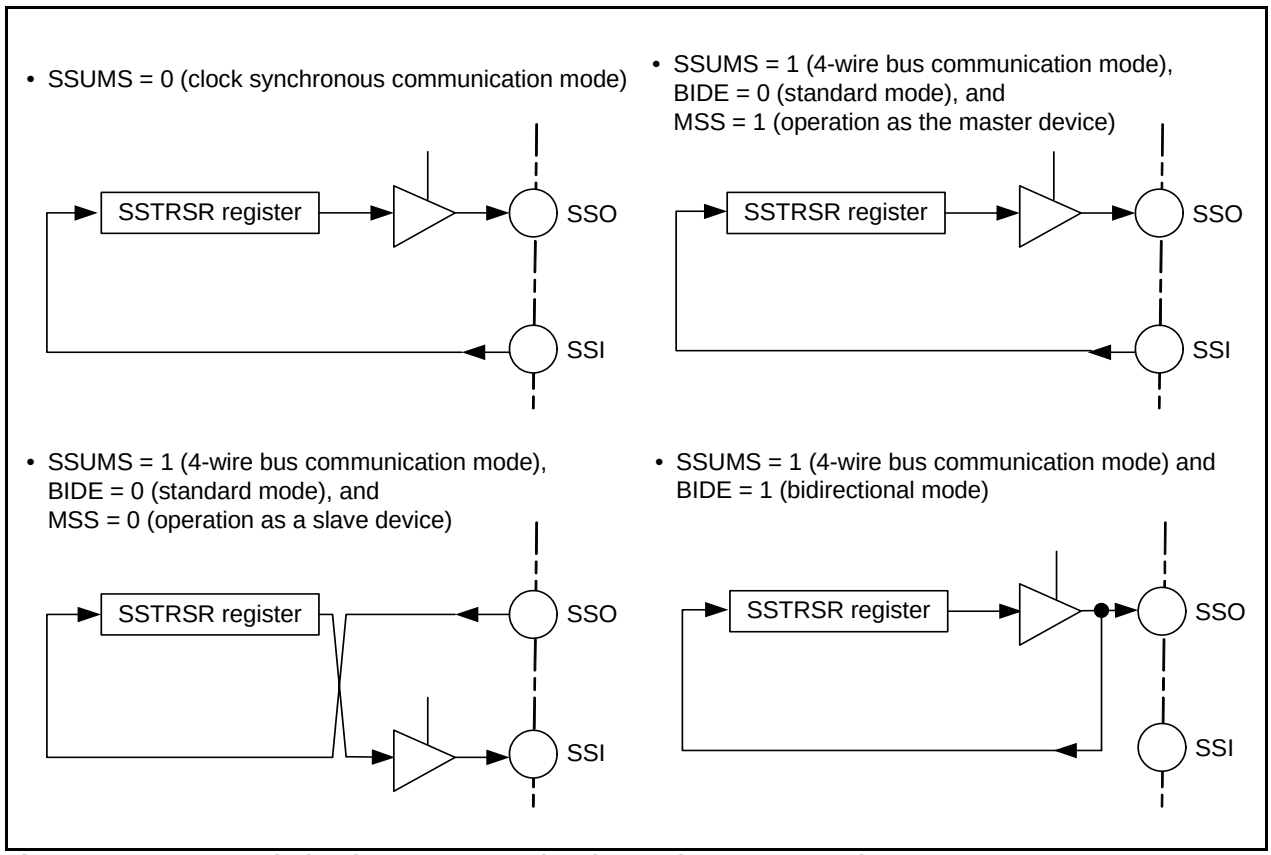

• SSUMS = 0 (clock synchronous communication mode)
SSTRSR register
SSO
SSI
• SSUMS = 1 (4-wire bus communication mode), BIDE = 0 (standard mode), and MSS = 1 (operation as the master device)
SSTRSR register
SSO
SSI
• SSUMS = 1 (4-wire bus communication mode), BIDE = 0 (standard mode), and MSS = 0 (operation as a slave device)
SSTRSR register
SSO
SSI
• SSUMS = 1 (4-wire bus communication mode) and BIDE = 1 (bidirectional mode)
SSTRSR register
SSO
SSI

Figure 24.3 Association between Data I/O Pins and SSTRSR Register

24.3.3 Interrupt Requests

The synchronous serial communication unit has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Since these interrupt requests are assigned to the synchronous serial communication unit interrupt vector table, determining interrupt sources by flags is required.
Table 24.3 shows the Interrupt Requests of Synchronous Serial Communication Unit.

Table 24.3 Interrupt Requests of Synchronous Serial Communication Unit

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1 and TDRE = 1
Transmit end	TEI	TEIE = 1 and TEND = 1
Receive data full	RXI	RIE = 1 and RDRF = 1
Overrun error	OEI	RIE = 1 and ORER = 1
Conflict error	CEI	CEIE = 1 and CE = 1

CEIE, RIE, TEIE, TIE: Bits in SSER register
ORER, RDRF, TEND, TDRE: Bits in SSSR register

If the generation conditions in Table 24.3 are met, an interrupt request of the synchronous serial communication unit is generated. Set each interrupt source to 0 by the synchronous serial communication unit interrupt routine.

However, bits TDRE and TEND are automatically set to 0 by writing transmit data to the SSTDR register and the RDRF bit is automatically set to 0 by reading the SSRDR register. In particular, the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR) at the same time transmit data is written to the SSTDR register. If the TDRE bit is further set to 0 (data not transferred from registers SSTDR to SSTRSR), additional 1 byte may be transmitted.

24.3.4 Communication Modes and Pin Functions

The synchronous serial communication unit switches the functions of the I/O pins in each communication mode according to the setting of the MSS bit in the SSCRH register and bits RE and TE in the SSER register. Table 24.4 shows the Association between Communication Modes and I/O Pins.

Table 24.4 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	— (1)	Input
				1	0	— (1)	Output	Input
					1	Input	Output	Input
			1	0	1	Input	— (1)	Output
				1	0	— (1)	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	— (1)	Input	Input
				1	0	Output	— (1)	Input
					1	Output	Input	Input
			1	0	1	Input	— (1)	Output
				1	0	— (1)	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode (2)	1	1	0	0	1	— (1)	Input	Input
				1	0	— (1)	Output	Input
			1	0	1	— (1)	Input	Output
				1	0	— (1)	Output	Output

Notes:
1. This pin can be used as a programmable I/O port.
2. Do not set both bits TE and RE to 1 in 4-wire bus (bidirectional) communication mode.

SSUMS, BIDE: Bits in SSMR2 register
MSS: Bit in SSCRH register
TE, RE: Bits in SSER register

24.4 Clock Synchronous Communication Mode

24.4.1 Initialization in Clock Synchronous Communication Mode

Figure 24.4 shows Initialization in Clock Synchronous Communication Mode. Before data transmission or reception, set the TE bit in the SSER register to 0 (transmission disabled) and the RE bit to 0 (reception disabled), and initialize the synchronous serial communication unit.
Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.
Setting the RE bit to 0 does not change the contents of flags RDRF and ORER or the contents of the SSRDR register.

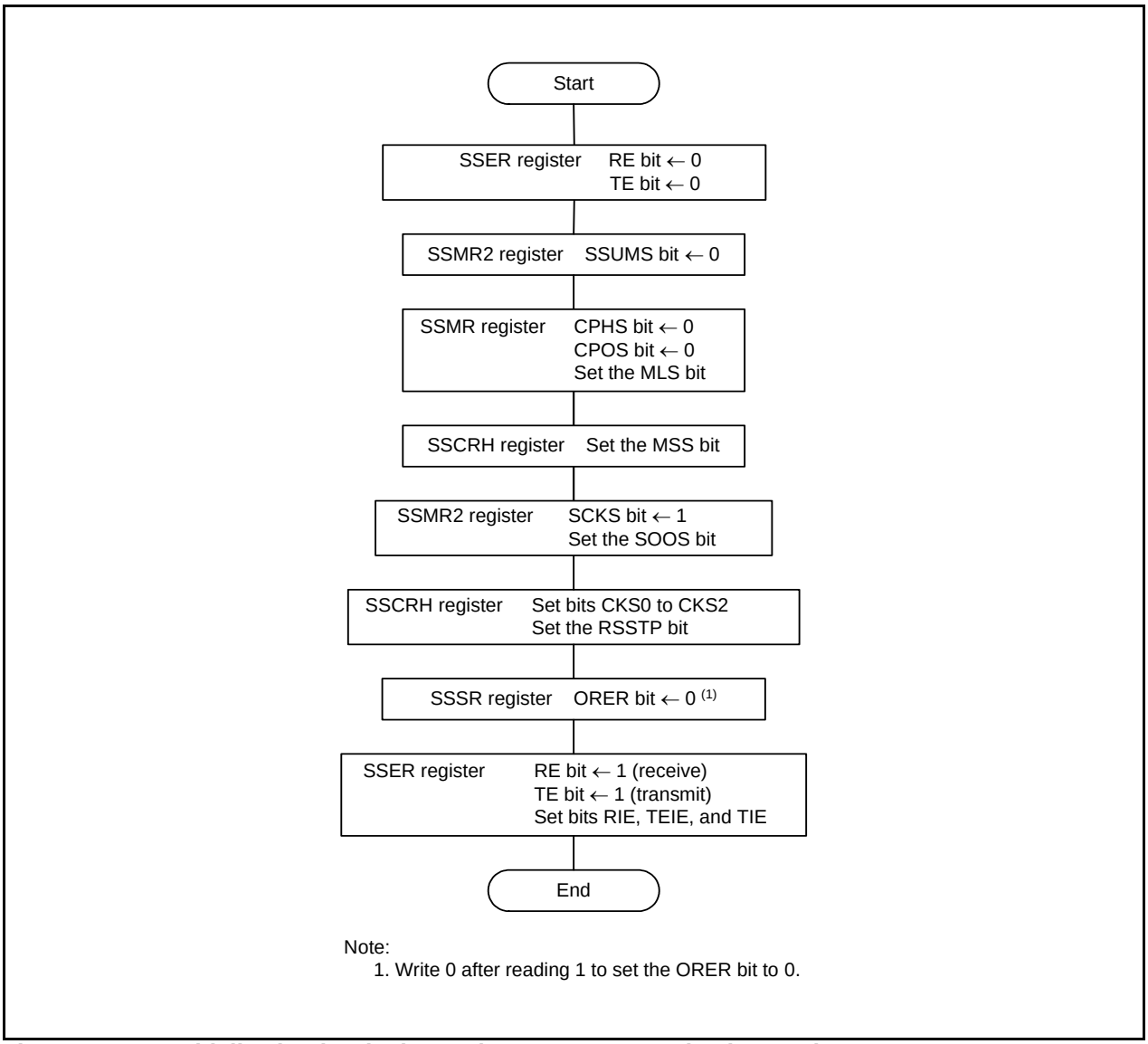

Start
SSER register RE bit ← 0
TE bit ← 0
SSMR2 register SSUMS bit ← 0
SSMR register CPHS bit ← 0
CPOS bit ← 0
Set the MLS bit
SSCRH register Set the MSS bit
SSMR2 register SCKS bit ← 1
Set the SOOS bit
SSCRH register Set bits CKS0 to CKS2
Set the RSSTP bit
SSSR register ORER bit ← 0 (1)
SSER register RE bit ← 1 (receive)
TE bit ← 1 (transmit)
Set bits RIE, TEIE, and TIE
End
Note:
1. Write 0 after reading 1 to set the ORER bit to 0.

Figure 24.4 Initialization in Clock Synchronous Communication Mode

24.4.2 Data Transmission

Figure 24.5 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and data. When the synchronous serial communication unit is set as a slave device, it outputs data synchronized with the input clock.

When the TE bit is set to 1 (transmission enabled) before writing the transmit data to the SSTDR register, the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1 at this time, a TXI interrupt request is generated.

When one frame of data is transferred while the TDRE bit is set to 0, data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while the TDRE bit is set to 1, the TEND bit in the SSSR register is set to 1 (TDRE bit is set to 1 when the last bit of the transmit data is transmitted) and the state is retained. When the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled) at this time, a TEI interrupt request is generated. The SSCK pin is fixed high after transmit-end.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

Figure 24.6 shows a Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode).

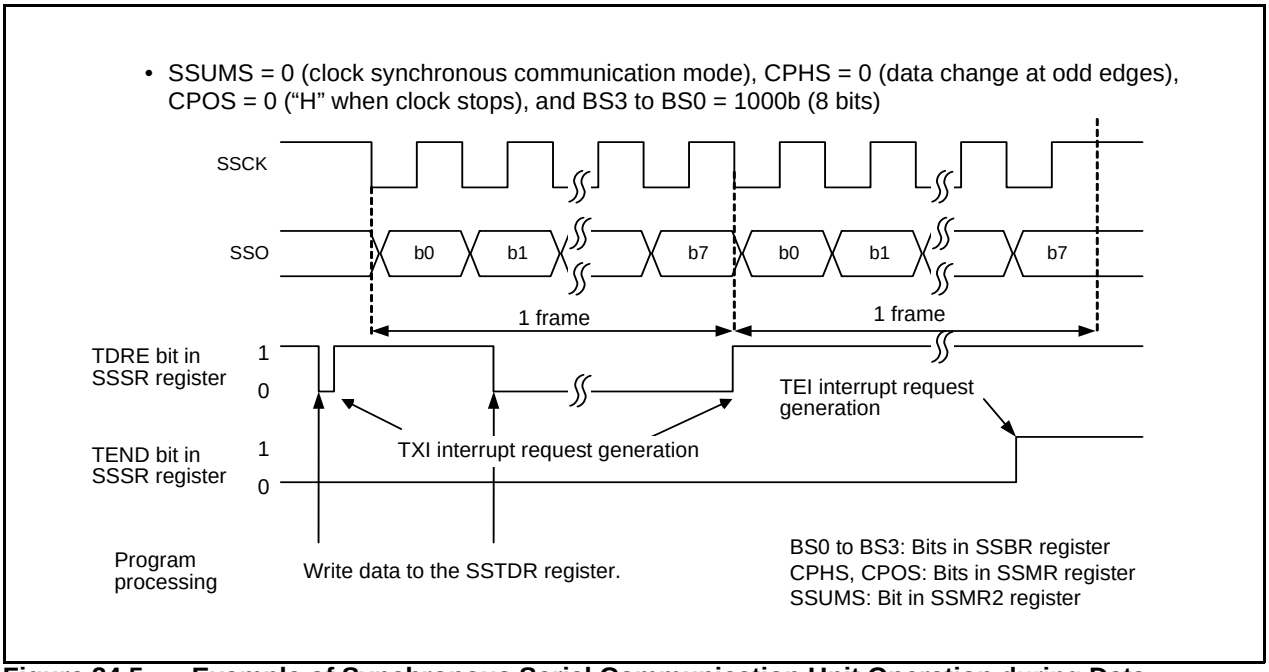
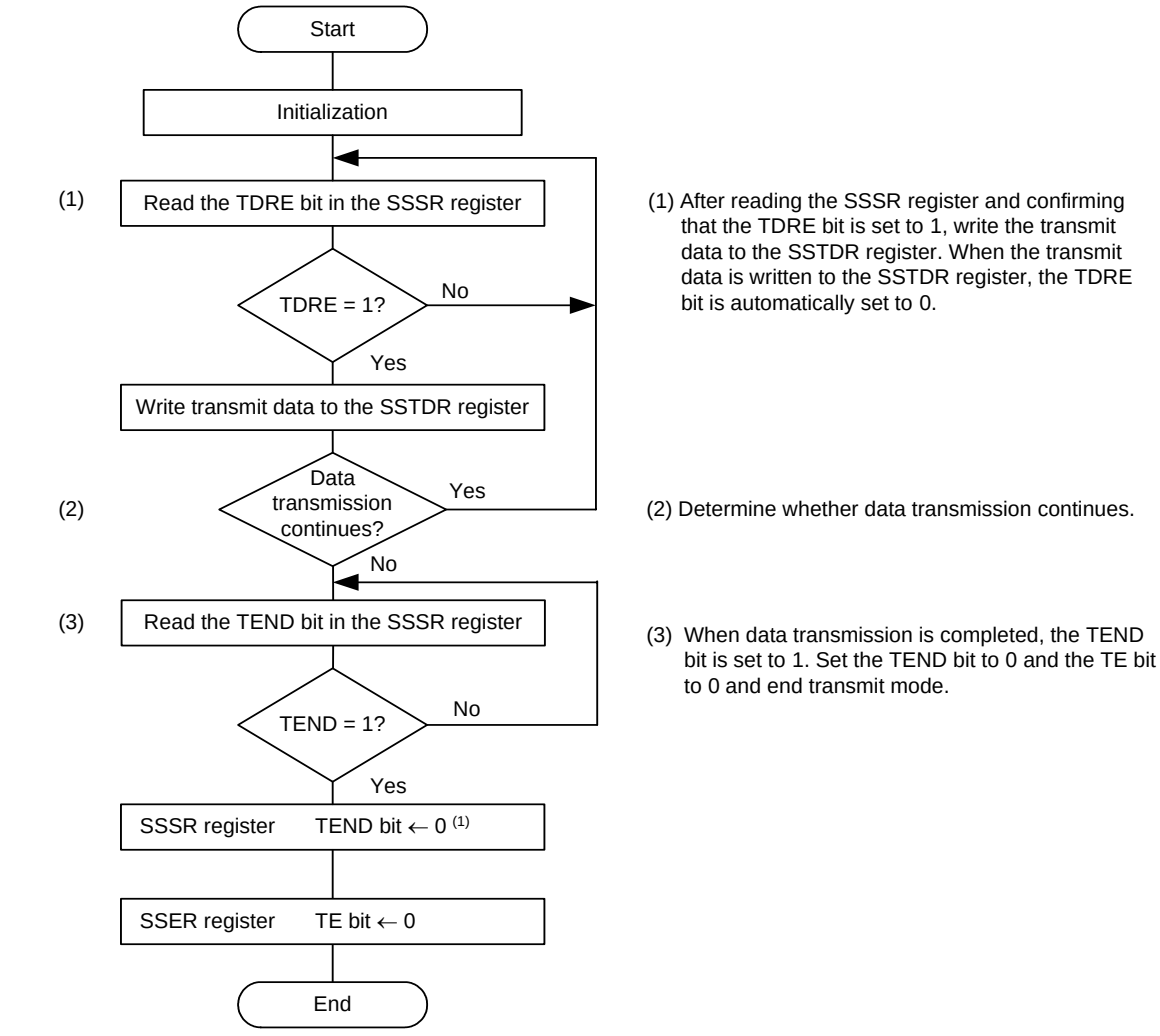


Figure 24.5 Example of Synchronous Serial Communication Unit Operation during Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)


Start
Initialization
(1)
Read the TDRE bit in the SSSR register
TDRE = 1?
No
Yes
Write transmit data to the SSTDR register
Data transmission continues?
(2)
Yes
No
(3)
Read the TEND bit in the SSSR register
TEND = 1?
No
Yes
SSSR register TEND bit ← 0 (1)
SSER register TE bit ← 0
End
(1) After reading the SSSR register and confirming that the TDRE bit is set to 1, write the transmit data to the SSTDR register. When the transmit data is written to the SSTDR register, the TDRE bit is automatically set to 0.
(2) Determine whether data transmission continues.
(3) When data transmission is completed, the TEND bit is set to 1. Set the TEND bit to 0 and the TE bit to 0 and end transmit mode.

Note:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 24.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)

24.4.3 Data Reception

Figure 24.7 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and inputs data. When the synchronous serial communication unit is set as a slave device, it inputs data synchronized with the input clock.

When the synchronous serial communication unit is set as the master device, it outputs a receive clock and starts receiving by performing dummy read from the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled) at this time, an RXI interrupt request is generated. If the SSDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (receive operation is completed after receiving 1 byte of data). The synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (reception disabled) and the RSSTP bit to 0 (receive operation is continued after receiving the 1 byte of data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (reception enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

Figure 24.8 shows a Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode).

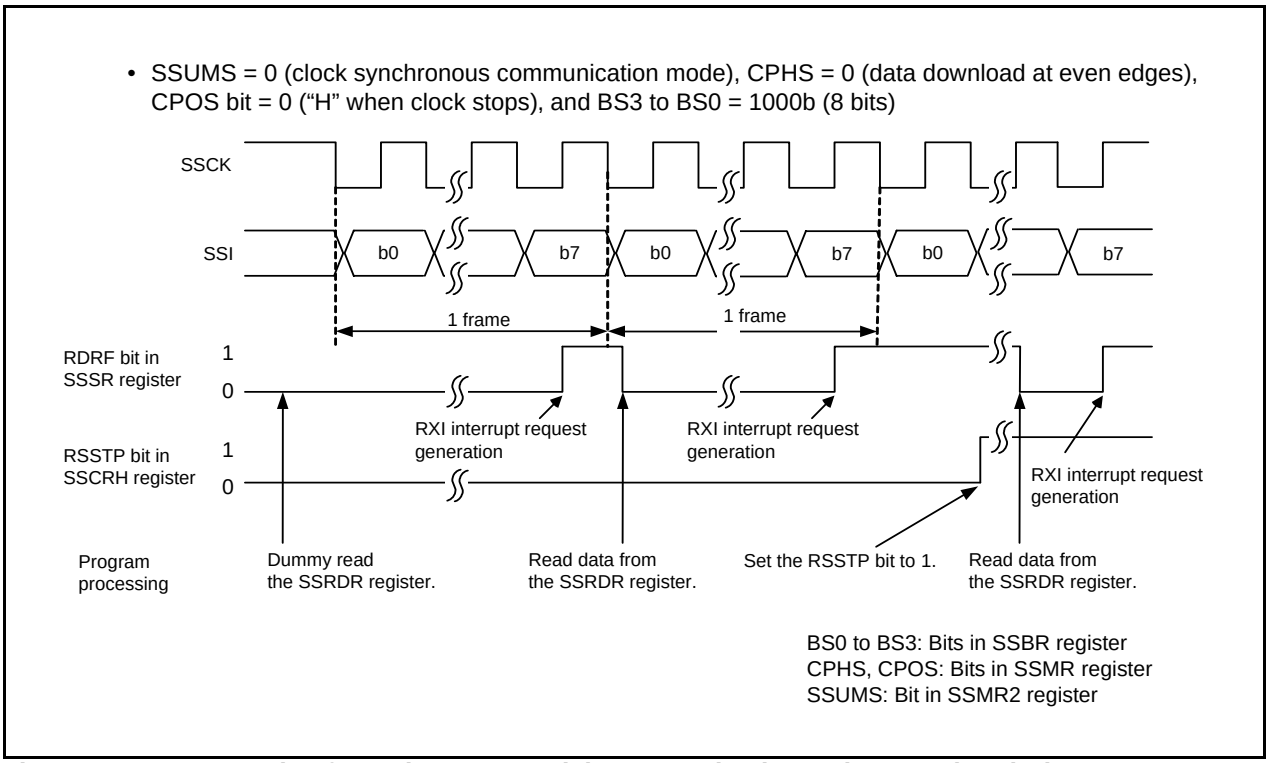

• SSUMS = 0 (clock synchronous communication mode), CPHS = 0 (data download at even edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)
SSCK
SSI
b0
b7
b0
b7
b0
b7
1 frame
1 frame
RDRF bit in SSSR register
1
0
RSSTP bit in SSCRH register
1
0
RXI interrupt request generation
RXI interrupt request generation
RXI interrupt request generation
Program processing
Dummy read the SSRDR register.
Read data from the SSRDR register.
Set the RSSTP bit to 1.
Read data from the SSRDR register.
BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register
SSUMS: Bit in SSMR2 register

Figure 24.7 Example of Synchronous Serial Communication Unit Operation during Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

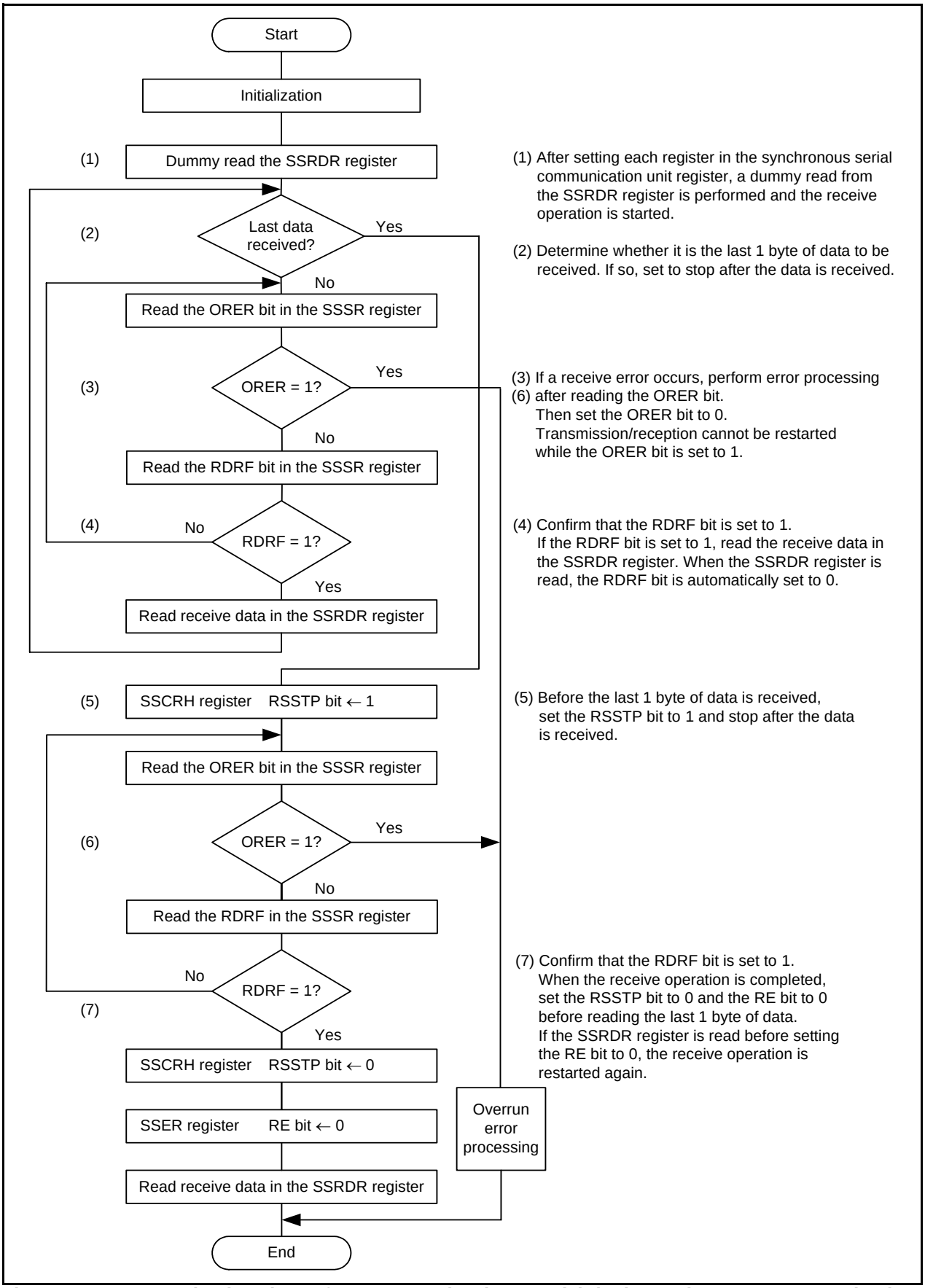

Start
Initialization
(1)
Dummy read the SSRDR register
(2)
Last data received?
Yes
No
Read the ORER bit in the SSSR register
(3)
ORER = 1?
Yes
No
Read the RDRF bit in the SSSR register
(4)
No
RDRF = 1?
Yes
Read receive data in the SSRDR register
(5)
SSCRH register RSSTP bit ← 1
Read the ORER bit in the SSSR register
(6)
ORER = 1?
Yes
No
Read the RDRF in the SSSR register
No
RDRF = 1?
(7)
Yes
SSCRH register RSSTP bit ← 0
SSER register RE bit ← 0
Read receive data in the SSRDR register
Overrun error processing
End
(1) After setting each register in the synchronous serial communication unit register, a dummy read from the SSRDR register is performed and the receive operation is started.
(2) Determine whether it is the last 1 byte of data to be received. If so, set to stop after the data is received.
(3) If a receive error occurs, perform error processing
(6) after reading the ORER bit.
Then set the ORER bit to 0.
Transmission/reception cannot be restarted while the ORER bit is set to 1.
(4) Confirm that the RDRF bit is set to 1.
If the RDRF bit is set to 1, read the receive data in the SSRDR register. When the SSRDR register is read, the RDRF bit is automatically set to 0.
(5) Before the last 1 byte of data is received, set the RSSTP bit to 1 and stop after the data is received.
(7) Confirm that the RDRF bit is set to 1.
When the receive operation is completed, set the RSSTP bit to 0 and the RE bit to 0 before reading the last 1 byte of data.
If the SSRDR register is read before setting the RE bit to 0, the receive operation is restarted again.

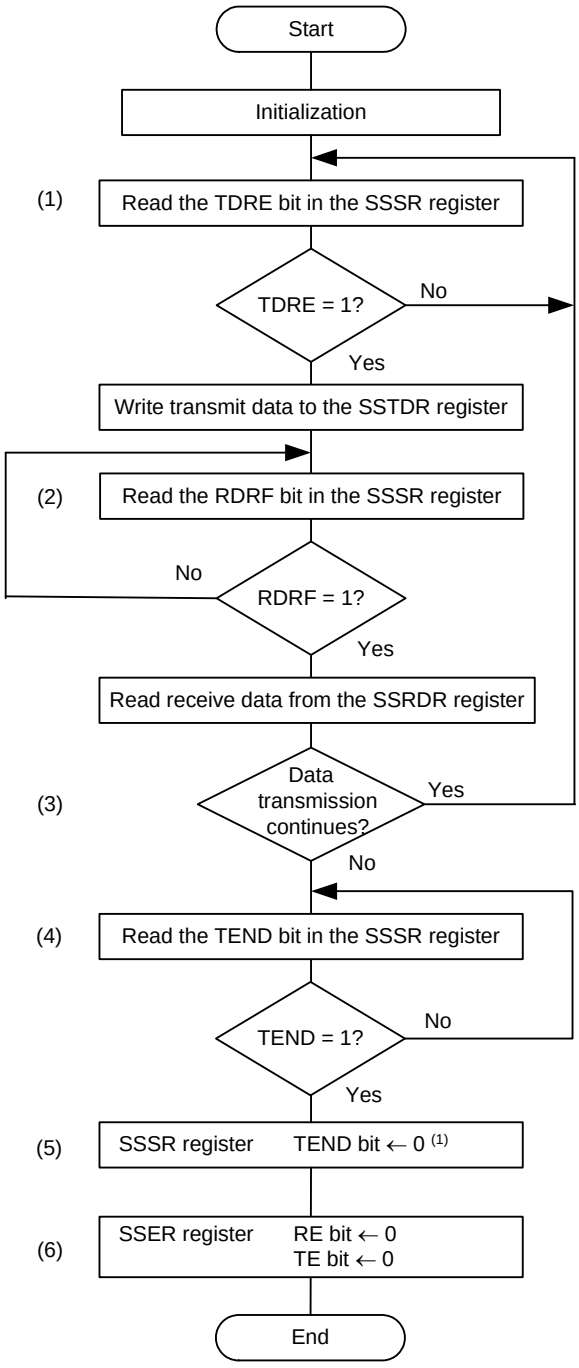
Figure 24.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)

24.4.3.1 Data Transmission/Reception

Data transmission/reception is an operation combining data transmission and reception which were described earlier. Transmission/reception is started by writing data to the SSTDR register.
When the last transfer clock (the data transfer length can be set from 8 to 16 bits using the SSBR register) rises or the ORER bit is set to 1 (overrun error) while the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), the transmit/receive operation is stopped.
Before switching from transmit mode (TE = 1) or receive mode (RE = 1) to transmit/receive mode (TE = RE = 1), set the TE bit to 0 and RE bit to 0 once. After confirming that the TEND bit is set to 0 (TDRE bit is set to 0 when the last bit of the transmit data is transmitted), the RDRF bit is set to 0 (no data in the SSRDR register), and the ORER bit is set to 0 (no overrun error), set bits TE and RE to 1.
Figure 24.9 shows a Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode).
When exiting transmit/receive mode after this mode is used (TE = RE = 1), a clock may be output if transmit/receive mode is exited after reading the SSRDR register. To avoid any clock outputs, perform either of the following:

- First set the RE bit to 0, and then set the TE bit to 0.
- Set bits TE and RE at the same time.

When subsequently switching to receive mode (TE = 0 and RE = 1), first set the SRES bit to 1, and set this bit to 0 to reset the SSU control unit and the SSTRSR register. Then, set the RE bit to 1.



(1) After reading the SSSR register and confirming that the TDRE bit is set to 1, write the transmit data to the SSTDR register. When the transmit data is written to the SSTDR register, the TDRE bit is automatically set to 0.

(2) Confirm that the RDRF bit is set to 1. If the RDRF bit is set to 1, read receive data in the SSRDR register. When the SSRDR register is read, the RDRF bit is automatically set to 0.

(3) Determine whether data transmission continues.

(4) When the data transmission is completed, the TEND bit in the SSSR register is set to 1.

(5) Set the TEND bit to 0, and bits RE and TE
(6) in the SSER register to 0 before ending transmit/receive mode.

Note:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 24.9 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode)

24.5 Operation in 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

The data input line and output line change according to the settings of the MSS bit in the SSCRH register and the BIDE bit in the SSMR2 register. For details, refer to **24.3.2.1 Association between Data I/O Pins and SS Shift Register**. In this mode, the clock polarity, phase, and data settings are performed by using bits CPOS and CPHS in the SSMR register. For details, refer to **24.3.1.1 Association between Transfer Clock Polarity, Phase, and Data**.

When this MCU is set as the master device, the chip select line controls output. When the synchronous serial communication unit is set as a slave device, the chip select line controls input. When it is set as the master device, the chip select line controls output of the $\overline{\text{SCS}}$ pin or controls output of a general port according to the setting of the CSS1 bit in the SSMR2 register. When the MCU is set as a slave device, the chip select line sets the $\overline{\text{SCS}}$ pin as input by setting bits CSS1 and CSS0 in the SSMR2 register to 01b.

In 4-wire bus communication mode, the MLS bit in the SSMR register is set to 0 and communication is performed MSB first.

24.5.1 Initialization in 4-Wire Bus Communication Mode

Figure 24.10 shows Initialization in 4-Wire Bus Communication Mode. Before the data transit/receive operation, set the TE bit in the SSER register to 0 (transmission disabled), the RE bit in the SSER register to 0 (reception disabled), and initialize the synchronous serial communication unit.

Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.

Setting the RE bit to 0 does not change the settings of flags RDRF and ORER or the contents of the SSRDR register.

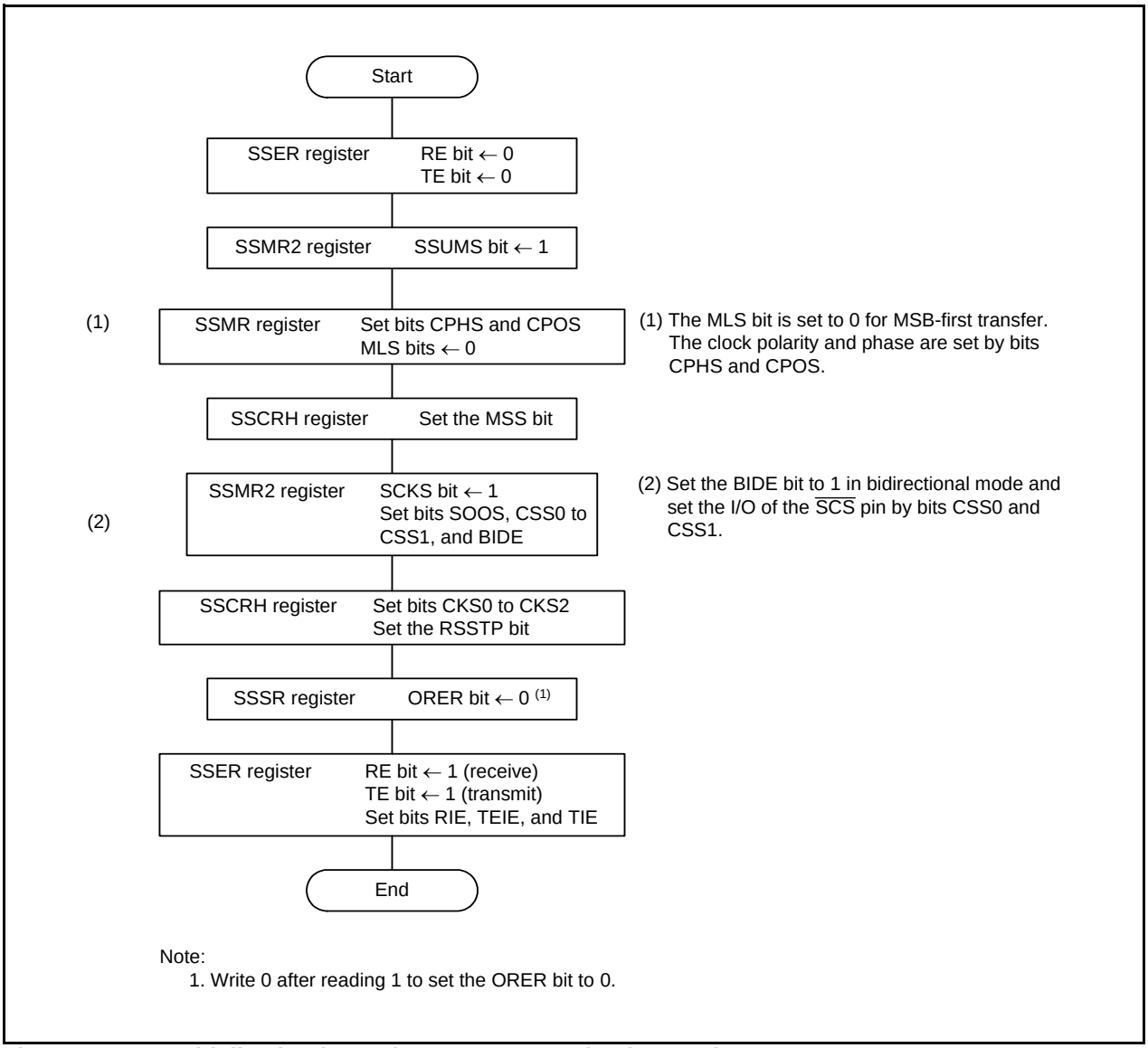

Start
SSER register RE bit ← 0
TE bit ← 0
SSMR2 register SSUMS bit ← 1
(1)
SSMR register Set bits CPHS and CPOS
MLS bits ← 0
(1) The MLS bit is set to 0 for MSB-first transfer. The clock polarity and phase are set by bits CPHS and CPOS.
SSCRH register Set the MSS bit
(2)
SSMR2 register SCKS bit ← 1
Set bits SOOS, CSS0 to CSS1, and BIDE
(2) Set the BIDE bit to 1 in bidirectional mode and set the I/O of the SCS pin by bits CSS0 and CSS1.
SSCRH register Set bits CKS0 to CKS2
Set the RSSTP bit
SSSR register ORER bit ← 0 (1)
SSER register RE bit ← 1 (receive)
TE bit ← 1 (transmit)
Set bits RIE, TEIE, and TIE
End
Note:
1. Write 0 after reading 1 to set the ORER bit to 0.

Figure 24.10 Initialization in 4-Wire Bus Communication Mode

24.5.2 Data Transmission

Figure 24.11 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During the data transmit operation, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data in synchronization with the input clock while the $\overline{SCS}$ pin is low-input state.

When the transmit data is written to the SSTDR register after setting the TE bit to 1 (transmission enabled), the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1 at this time, the TXI interrupt request is generated.

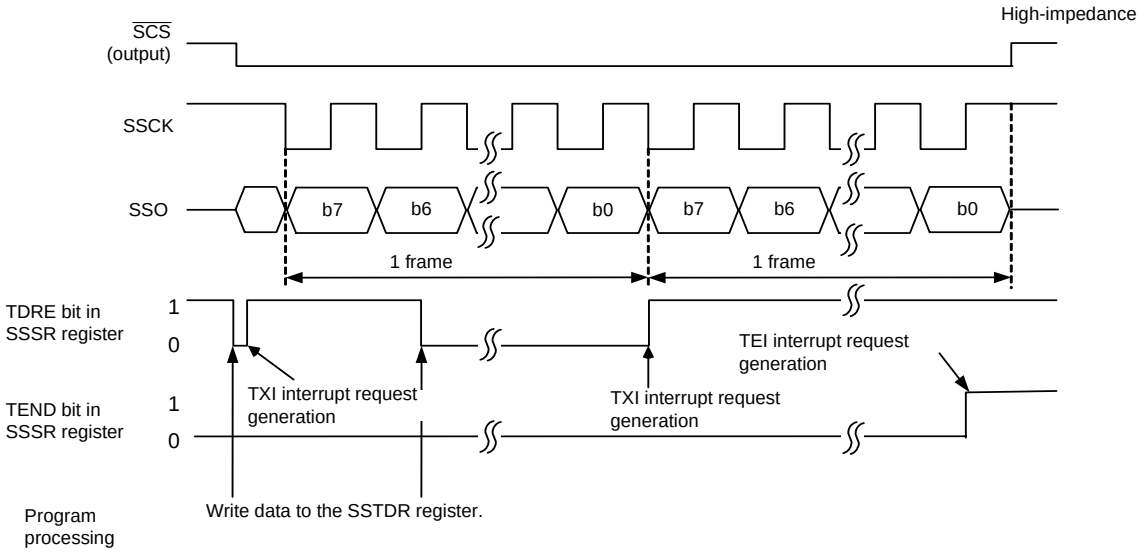
After one frame of data is transferred while the TDRE bit is set to 0, the data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while TDRE is set to 1, TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. When the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled) at this time, the TEI interrupt request is generated. The SSCK pin remains high after transmit-end and the $\overline{SCS}$ pin is held high. When transmitting continuously while the $\overline{SCS}$ pin is held low, write the next transmit data to the SSTDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

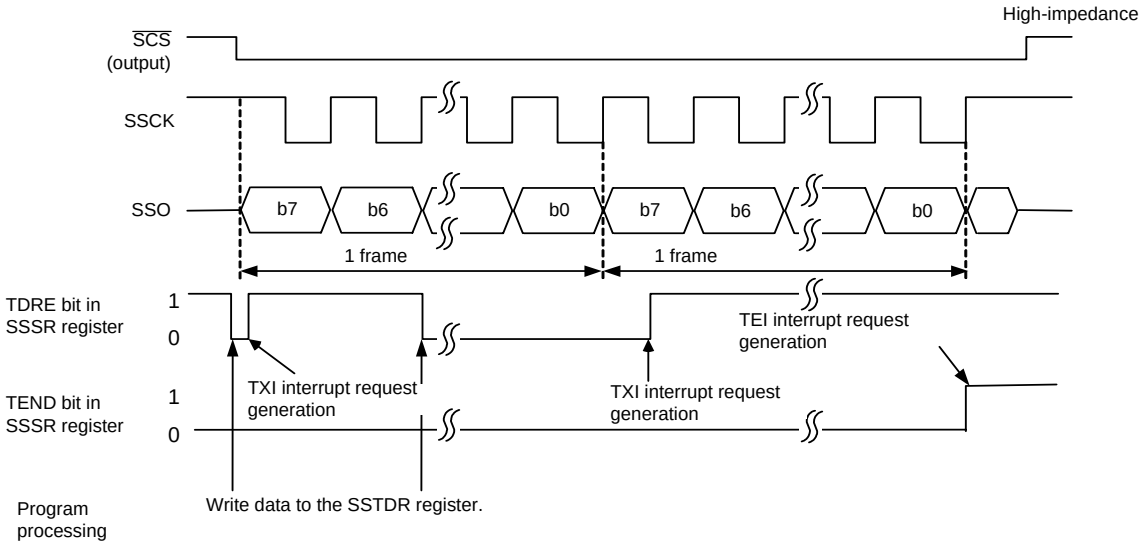
In contrast to the clock synchronous communication mode, the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as the master device. The SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is high-input state when operating as a slave device.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 24.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

• CPHS bit = 0 (data change at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data change at even edges). CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 24.11 Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

24.5.3 Data Reception

Figure 24.12 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin is low-input state.

When the MCU is set as the master device, it outputs a receive clock and starts receiving by performing a dummy read from the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled) at this time, an RXI interrupt request is generated. When the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (receive operation is completed after receiving 1-byte data). The synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (reception disabled) and the RSSTP bit to 0 (receive operation is continued after receiving 1-byte data) and read the receive data. When the SSRDR register is read while the RE bit is set to 1 (reception enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

The timing at which bits RDRF and ORER are set to 1 varies depending on the setting of the CPHS bit in the SSMR register. Figure 24.12 shows when bits RDRF and ORER are set to 1.

When the CPHS bit is set to 1 (data download at odd edges), bits RDRF and ORER are set to 1 at some point during the frame.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 24.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)**).

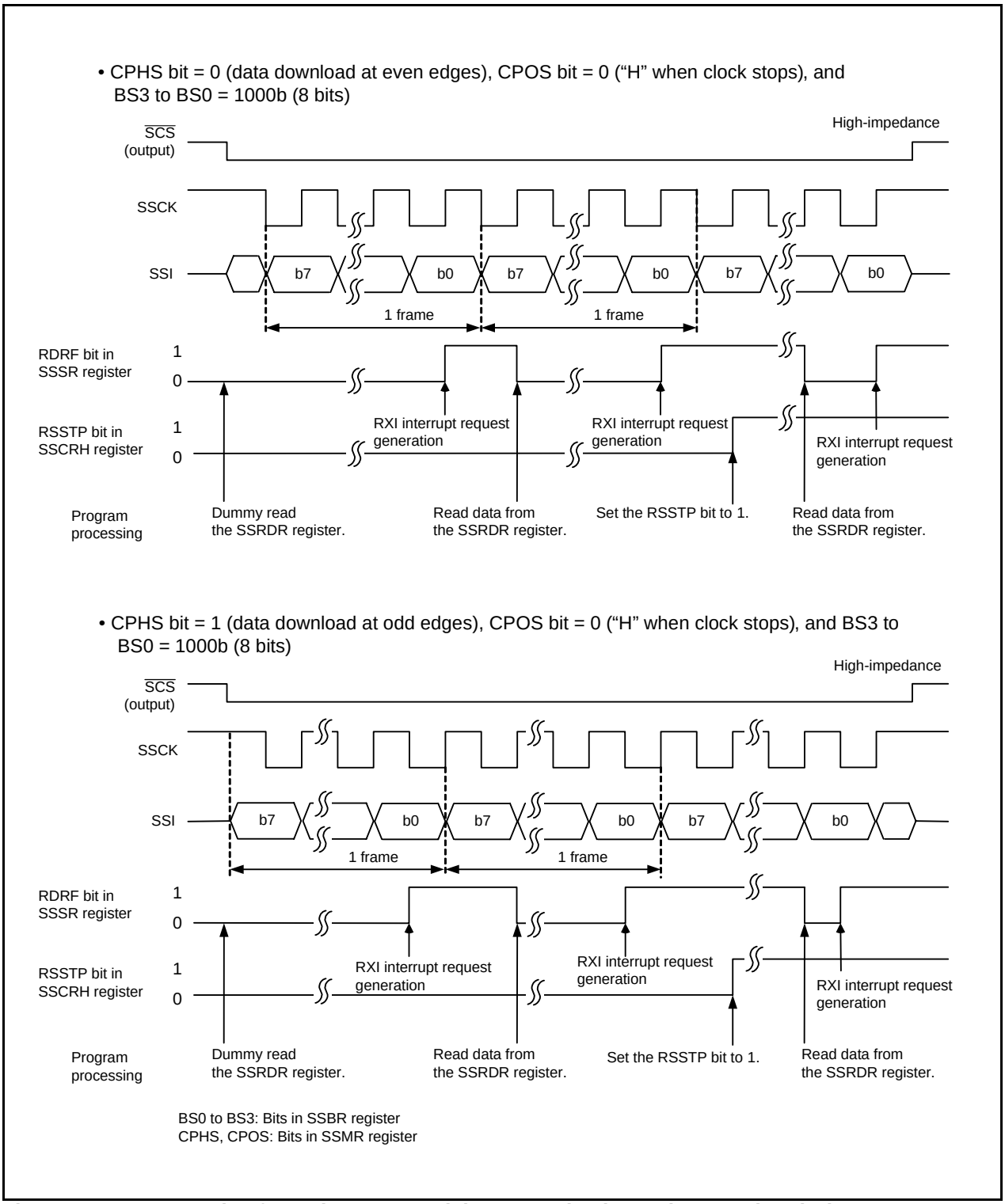

• CPHS bit = 0 (data download at even edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)
High-impedance
SCS (output)
SSCK
SSI
b7
b0
1 frame
RDRF bit in SSSR register
RSSTP bit in SSCRH register
RXI interrupt request generation
Program processing
Dummy read the SSRDR register.
Read data from the SSRDR register.
Set the RSSTP bit to 1.
• CPHS bit = 1 (data download at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)
BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 24.12 Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

24.5.4 $\overline{\text{SCS}}$ Pin Control and Arbitration

When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the CSS1 bit is set to 1 (function as the $\overline{\text{SCS}}$ output pin), set the MSS bit in the SSCRH register to 1 (operation as the master device) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If the synchronous serial communication unit detects that the synchronized internal $\overline{\text{SCS}}$ signal is held low in this period, the CE bit in the SSSR register is set to 1 (conflict error) and the MSS bit is automatically set to 0 (operation as a slave device).
Figure 24.13 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE bit is set to 1. Set the CE bit to 0 (no conflict error) before starting transmission.

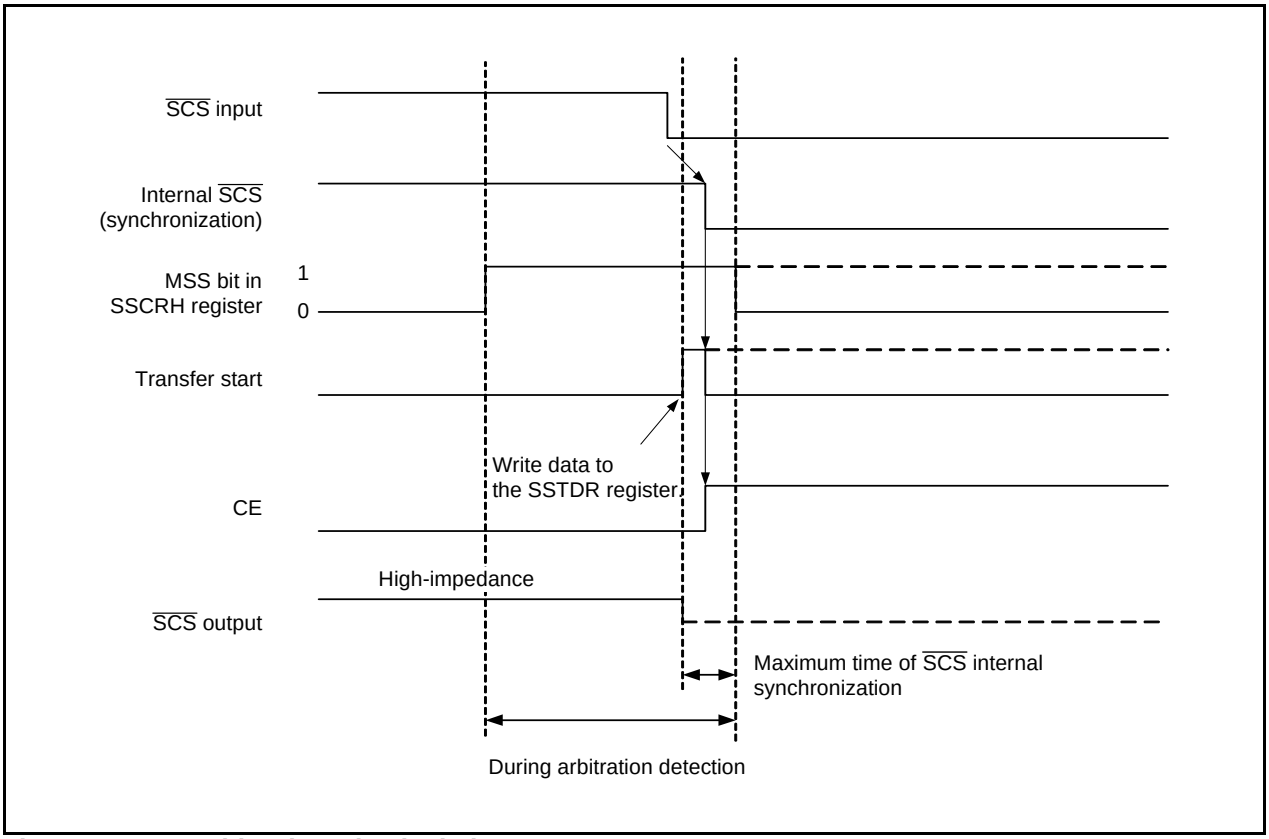


Figure 24.13 Arbitration Check Timing

24.6 Notes on Synchronous Serial Communication Unit (SSU)

To use the synchronous serial communication unit, set the IICSEL bit in the SSUIICSR register to 0 (SSU function selected).

25. I2C bus Interface

The I2C bus interface is the circuit that performs serial communication based on the data transfer format of the Philips I2C bus.

25.1 Introduction

Table 25.1 lists the I2C bus Interface Specifications. Figure 25.1 shows a Block Diagram of I2C bus interface, and Figure 25.2 shows the External Circuit Connection Example of Pins SCL and SDA. Table 25.2 lists the I2C bus Interface Pin Configuration.

* I2C bus is a trademark of Koninklijke Philips Electronics N. V.

Table 25.1 I2C bus Interface Specifications

Item	Specification
Communication formats	• I2C bus format - Selectable as master/slave device - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent) - Start/stop conditions are automatically generated in master mode. - Automatic loading of the acknowledge bit during transmission - Bit synchronization/wait function (In master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not possible yet, the SCL signal goes low and the interface stands by.) - Support for direct drive of pins SCL and SDA (N-channel open-drain output) • Clock synchronous serial format Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent)
I/O pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer clocks	• When the MST bit in the ICCR1 register is set to 0 • External clock (input from the SCL pin) • When the MST bit in the ICCR1 register is set to 1 • Internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and bits IICTCTWI and IICTCHALF in the PINSR register (output from the SCL pin)
Receive error detection	• Overrun error detection (clock synchronous serial format) • Indicates an overrun error during reception. When the last bit of the next unit of data is received while the RDRF bit in the ICSR register is set to 1 (data in the ICDRR register), the AL bit is set to 1.
Interrupt sources	• I2C bus format ..... 6 sources (1) • Transmit data empty (including when slave address matches), transmit end, receive data full (including when slave address matches), arbitration lost, NACK detection, and stop condition detection • Clock synchronous serial format ..... 4 sources (1) • Transmit data empty, transmit end, receive data full, and overrun error
Selectable functions	• I2C bus format Selectable output level for the acknowledge signal during reception • Clock synchronous serial format Selectable MSB first or LSB first as the data transfer direction • SDA digital delay Digital delay value for the SDA pin selectable by bits SDADLY0 to SDADLY1 in the PINSR register.

Note:
1. All sources use a single interrupt vector table for the I2C bus interface.

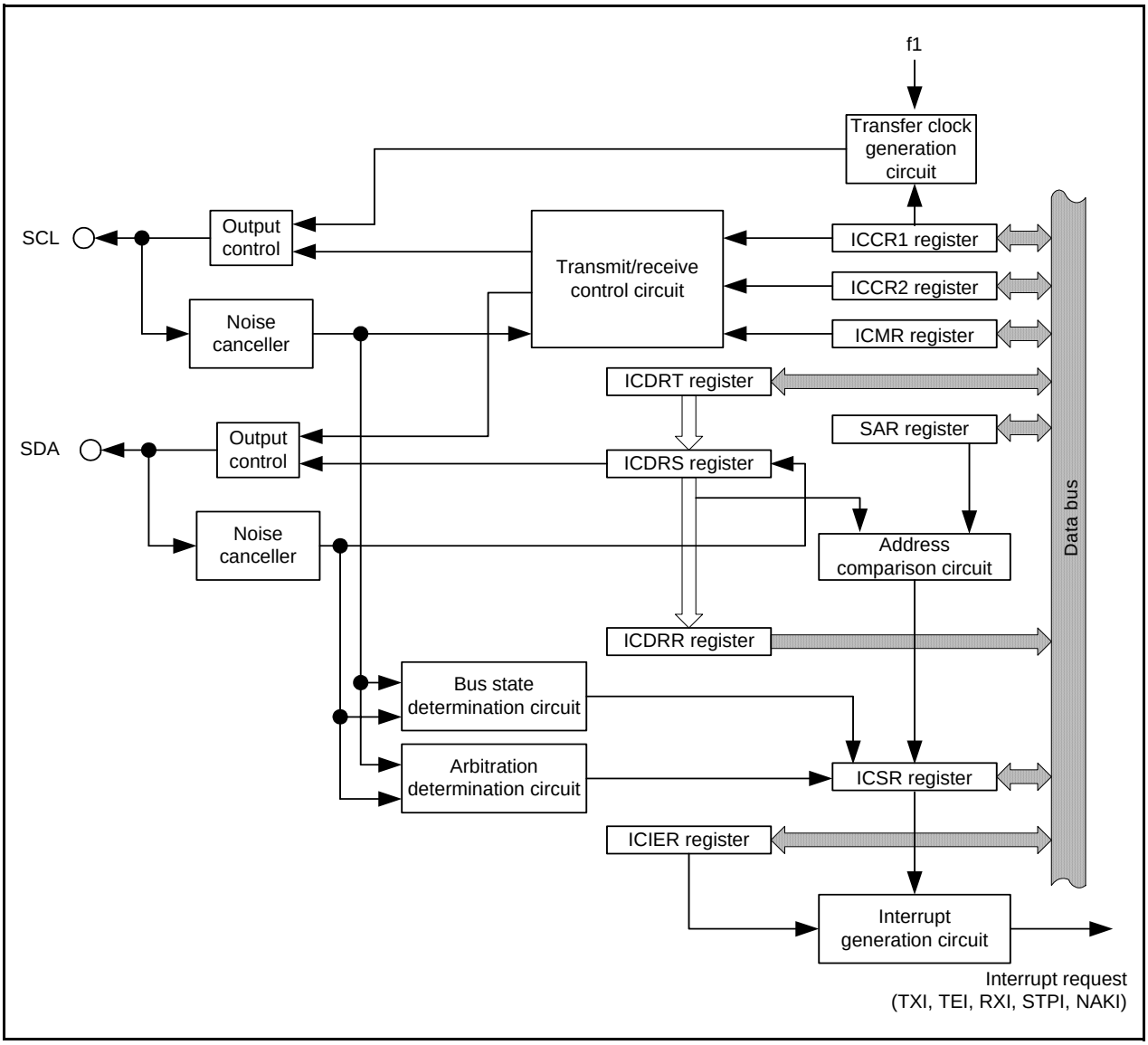


Figure 25.1 Block Diagram of I2C bus interface

Table 25.2 I2C bus Interface Pin Configuration

Pin Name	Assigned Pin	Function
SCL	P8_2, P6_3	Clock I/O
SDA	P8_3, P6_4	Data I/O

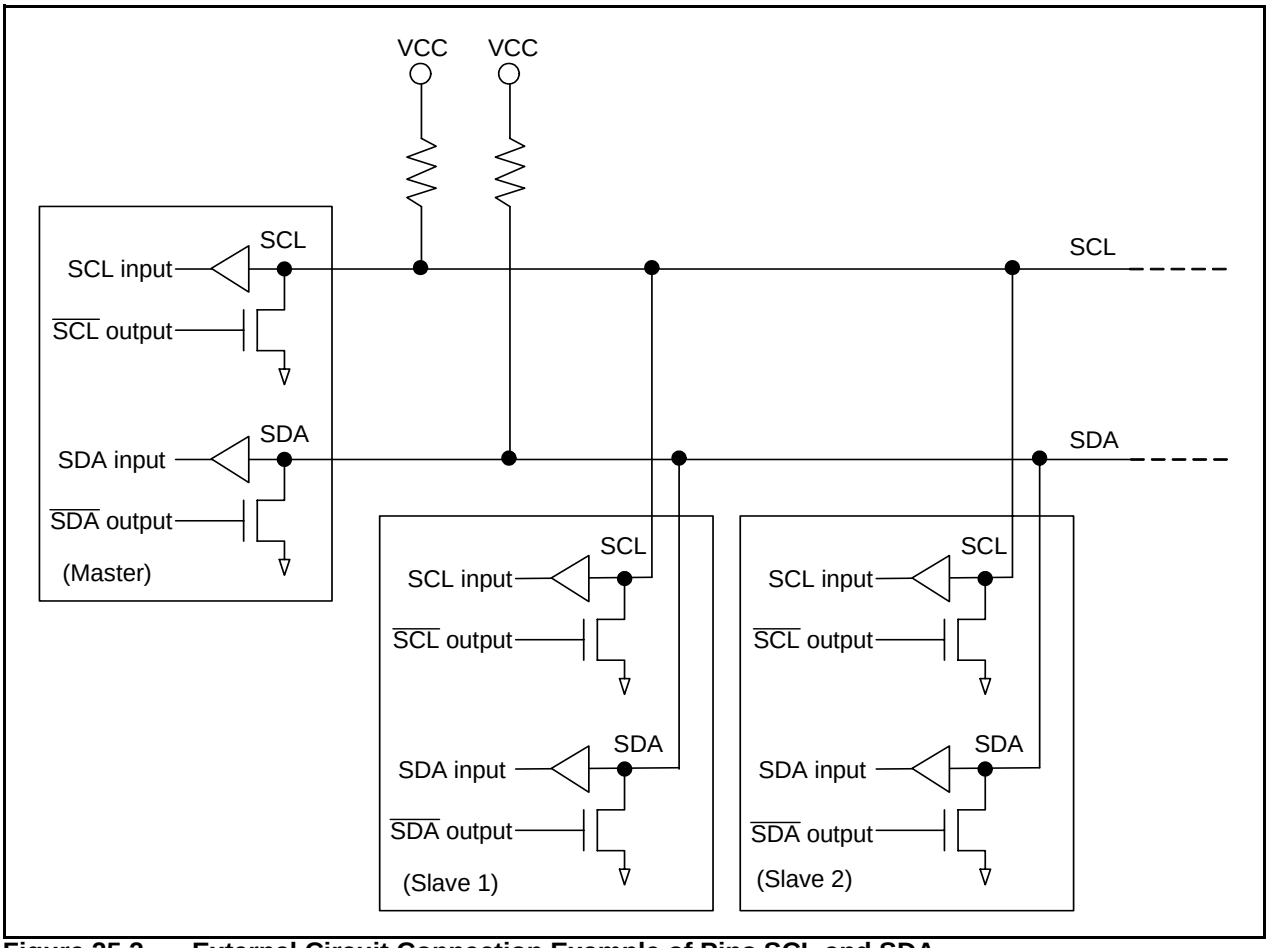


Figure 25.2 External Circuit Connection Example of Pins SCL and SDA

25.2 Registers

25.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	MSTURT2	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	UART0 standby bit	0: Active 1: Standby (1)	R/W
b2	MSTURT2	UART2 standby bit	0: Active 1: Standby (2)	R/W
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (3)	R/W
b4	MSTLCD	LCD standby bit	0: Active 1: Standby (4)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (5)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	A/D standby bit (6)	0: Active 1: Standby	R/W

Notes:
1. When the MSTURT0 bit is set to 1 (standby), any access to the UART0 associated registers (addresses 00A0h to 00A7h) is disabled.
2. When the MSTURT2 bit is set to 1 (standby), any access to the timer UART2 associated registers (addresses 00A8h to 00BFh) is disabled.
3. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
4. When the MSTLCD bit is set to 1 (standby), any access to the timer LCD associated registers (addresses 0200h to 0237h) is disabled.
5. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
6. When the MSTADC bit is set to 1 (standby), any access to the timer A/D associated registers (addresses 00C0h to 00D9h, 00DCh to 00DFh) is disabled.
   Set the MSTADC bit to 0 (active) when the temperature sensor is used.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

25.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SSOSEL0	SCSSEL0	SSCKSEL0	SSISEL0	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit	0: SSU function selected 1: I2C bus function selected	R/W
b1	—	Reserved bits	Set to 0.	—
b2	—			
b3	—			
b4	SSISEL0	SSI pin select bit	0: P8_1 assigned 1: P6_2 assigned	R/W
b5	SSCKSEL0	SSCK/SCL pin select bit	0: P8_2 assigned 1: P6_3 assigned	R/W
b6	SCSSEL0	SCS pin select bit	0: P8_0 assigned 1: P6_1 assigned	R/W
b7	SSOSEL0	SSO/SDA pin select bit	0: P8_3 assigned 1: P6_4 assigned	R/W

25.2.3 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0 to 9) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register.	R/W
b4	IICTCTWI	I2C double transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I2C half transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

25.2.4 IIC bus Transmit Data Register (ICDRT)

Address 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores transmit data. When the ICDRS register is detected as empty, the stored transmit data is transferred to the ICDRS register and transmission starts. When the next transmit data is written to the ICDRT register during the data transmission from the ICDRS register, continuous transmission is enabled. When the MLS bit in the ICMR register is set to 1 (data transfer with LSB first), the MSB-LSB inverted data is read after writing to the ICDRT register.	R/W

25.2.5 IIC bus Receive Data Register (ICDRR)

Address 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores receive data. When the ICDRS register receives 1 byte of data, the receive data is transferred to the ICDRR register and the next receive operation is enabled.	R

25.2.6 IIC bus Control Register 1 (ICCR1)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transmit clock select bit 3 to 0 (1)	b3 b2 b1 b0 0 0 0 0: f1/28 0 0 0 1: f1/40 0 0 1 0: f1/48 0 0 1 1: f1/64 0 1 0 0: f1/80 0 1 0 1: f1/100 0 1 1 0: f1/112 0 1 1 1: f1/128 1 0 0 0: f1/56 1 0 0 1: f1/80 1 0 1 0: f1/96 1 0 1 1: f1/128 1 1 0 0: f1/160 1 1 0 1: f1/200 1 1 1 0: f1/224 1 1 1 1: f1/256	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Transmission/reception select bit (2, 3, 6)	b5 b4 0 0: Slave Receive Mode (4) 0 1: Slave Transmit Mode 1 0: Master Receive Mode 1 1: Master Transmit Mode	R/W
b5	MST	Master/slave select bit (5, 6)		R/W
b6	RCVD	Reception disable bit	After reading the ICDRR register while the TRS bit is set to 0, 0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	I2C bus interface enable bit (7)	0: This module is halted (Pins SCL and SDA are set to the port function) 1: This module is enabled for transfer operations (Pins SCL and SDA are in the bus drive state)	R/W

Notes:

1. Set according to the necessary transfer rate in master mode. Refer to **Table 25.3 Transfer Rate Examples and Table 25.4 Transfer Rate Examples (2)** for the transfer rate. This bit is used for maintaining the setup time in transmit mode of slave mode. The time is 10Tcyc when the CKS3 bit is set to 0 and 20Tcyc when the CKS3 bit is set to 1. (1Tcyc = 1/f1(s))
2. Rewrite the TRS bit between transfer frames.
3. When the first 7 bits after the start condition in slave receive mode match the slave address set in the SAR register and the 8th bit is set to 1, the TRS bit is set to 1.
4. In master mode with the I2C bus format, if arbitration is lost, bits MST and TRS are set to 0 and the IIC enters slave receive mode.
5. When an overrun error occurs in master receive mode with the clock synchronous serial format, the MST bit is set to 0 and the I2C bus enters slave receive mode.
6. In multimaster operation, use the MOV instruction to set bits TRS and MST.
7. When writing 0 to the ICE bit or 1 to the IICRST bit in the ICCR2 register during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined. Refer to **25.9 Notes on I2C bus Interface**.

25.2.7 IIC bus Control Register 2 (ICCR2)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	IICRST	I2C bus control block reset bit (5)	When hang-up occurs due to communication failure during the I2C bus interface operation, writing 1 resets the control block of the I2C bus interface without setting ports or initializing registers.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	SCLO	SCL monitor flag	0: SCL pin is set to low 1: SCL pin is set to high	R
b4	SDAOP	SDAO write protect bit	When rewriting the SDAO bit, write 0 simultaneously (1). When read, the content is 1.	R/W
b5	SDAO	SDA output value control bit	When read 0: SDA pin output is held low 1: SDA pin output is held high When written (1, 2) 0: SDA pin output is changed to low 1: SDA pin output is changed to high-impedance (High-level output via an external pull-up resistor)	R/W
b6	SCP	Start/stop condition generation disable bit	When writing to the to BBSY bit, write 0 simultaneously (3). When read, the content is 1. Writing 1 is invalid.	R/W
b7	BBSY	Bus busy bit (4, 5)	When read: 0: Bus is released (SDA signal changes from low to high while SCL signal is held high) 1: Bus is occupied (SDA signal changes from high to low while SCL signal is held high) When written (3): 0: Stop condition generated 1: Start condition generated	R/W

Notes:
1. When rewriting the SDAO bit, write 0 to the SDAOP bit simultaneously using the MOV instruction.
2. Do not write to the SDAO bit during a transfer operation.
3. Enabled in master mode. When writing to the BBSY bit, write 0 to the SCP bit simultaneously using the MOV instruction. Execute the same way when a start condition is regenerated.
4. Disabled when the clock synchronous serial format is used.
5. When writing 0 to the ICE bit in the ICCR1 register or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit and the STOP bit in the ICSR register may become undefined. Refer to **25.9 Notes on I2C bus Interface**.

25.2.8 IIC bus Mode Register (ICMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counter 2 to 0	I2C bus format	R/W
b1	BC1		(Read: Number of remaining transfer bits;	R/W
b2	BC2		Write: Number of next transfer data bits). (1, 2) b2 b1 b0 0 0 0: 9 bits (3) 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits Clock synchronous serial format (Read: Number of remaining transfer bits; Write: Always 000b). b2 b1 b0 0 0 0: 8 bits 0 0 1: 1 bit 0 1 0: 2 bits 0 1 1: 3 bits 1 0 0: 4 bits 1 0 1: 5 bits 1 1 0: 6 bits 1 1 1: 7 bits	R/W
b3	BCWP	BC write protect bit	When rewriting bits BC0 to BC2, write 0 simultaneously. (2, 4) When read, the content is 1.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—	Reserved bit	Set to 0.	R/W
b6	WAIT	Wait insertion bit (5)	0: No wait states (Data and the acknowledge bit are transferred successively) 1: Wait state (After the clock of the last data bit falls, a low-level period is extended for two transfer clocks)	R/W
b7	MLS	MSB first/LSB first select bit	0: Data transfer with MSB first (6) 1: Data transfer with LSB first	R/W

Notes:
1. Rewrite between transfer frames. When writing values other than 000b, write when the SCL signal is low.
2. When writing to bits BC0 to BC2, write 0 to the BCWP bit simultaneously using the MOV instruction.
3. After data including the acknowledge bit is transferred, these bits are automatically set to 000b. When a start condition is detected, these bits are automatically set to 000b.
4. Do not rewrite when the clock synchronous serial format is used.
5. The setting value is valid in master mode with the I2C bus format. It is invalid in slave mode with the I2C bus format or when the clock synchronous serial format is used.
6. Set to 0 when the I2C bus format is used.

25.2.9 IIC bus Interrupt Enable Register (ICIER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ACKBT	Transmit acknowledge select bit	0: In receive mode, 0 is transmitted as the acknowledge bit. 1: In receive mode, 1 is transmitted as the acknowledge bit.	R/W
b1	ACKBR	Receive acknowledge bit	0: In transmit mode, the acknowledge bit received from the receive device is set to 0. 1: In transmit mode, the acknowledge bit received from the receive device is set to 1.	R
b2	ACKE	Acknowledge bit detection select bit	0: Content of the receive acknowledge bit is ignored and continuous transfer is performed. 1: When the receive acknowledge bit is set to 1, continuous transfer is halted.	R/W
b3	STIE	Stop condition detection interrupt enable bit	0: Stop condition detection interrupt request disabled 1: Stop condition detection interrupt request enabled (2)	R/W
b4	NAKIE	NACK receive interrupt enable bit	0: NACK receive interrupt request and arbitration lost/ overrun error interrupt request disabled 1: NACK receive interrupt request and arbitration lost/ overrun error interrupt request (1)	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt request disabled 1: Receive data full and overrun error interrupt request enabled (1)	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Notes:
1. An overrun error interrupt request is generated when the clock synchronous format is used.
2. Set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit in the ICSR register is set to 0.

25.2.10 IIC bus Status Register (ICSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	AL	AAS	ADZ
After Reset	0	0	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADZ	General call address recognition flag (1, 2)	This flag is set to 1 when a general call address is detected.	R/W
b1	AAS	Slave address recognition flag (1)	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SAR register in slave receive mode (slave address detection and general call address detection).	R/W
b2	AL	Arbitration lost flag/ overrun error flag (1)	I2C bus format: This flag indicates that arbitration has been lost in master mode. This flag is set to 1 (3) when: • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is held high at start condition detection in master transmit/receive mode Clock synchronous format: This flag indicates an overrun error. This flag is set to 1 when: • The last bit of the next unit of data is received while the RDRF bit is set to 1	R/W
b3	STOP	Stop condition detection flag (1, 7)	This flag is set to 1 when a stop condition is detected after the frame is transferred.	R/W
b4	NACKF	No acknowledge detection flag (1, 4)	This flag is set to 1 when no ACKnowledge is detected from the receive device after transmission.	R/W
b5	RDRF	Receive data register full flag (1, 5)	This flag is set to 1 when receive data is transferred from registers ICDRS to ICDRR.	R/W
b6	TEND	Transmit end flag (1, 6)	I2C bus format: This flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is set to 1. Clock synchronous format: This flag is set to 1 when the last bit of the transmit frame is transmitted.	R/W
b7	TDRE	Transmit data empty flag (1, 6)	This flag is set to 1 when: • Data is transferred from registers ICDRT to ICDRS and the CDRT register is empty • The TRS bit in the ICCR1 register is set to 1 (transmit mode) • A start condition is generated (including retransmission) • Slave receive mode is changed to slave transmit mode	R/W

Notes:
1. Each bit is set to 0 by reading 1 before writing 0.
2. This flag is enabled in slave receive mode with the I2C bus format.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I2C bus Interface monitors the SDA pin and the data which the I2C bus Interface transmits is different, the AL flag is set to 1 and the bus is occupied by another master.
4. The NACKF bit is enabled when the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted).
5. The RDRF bit is set to 0 when data is read from the ICDRR register.
6. Bits TEND and TDRE are set to 0 when data is written to the ICDRT register.
7. When writing 0 to the ICE bit in the ICCR1 register or 1 to the IICRST bit in the ICCR2 register during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit may become undefined. Refer to **25.9 Notes on I2C bus Interface**.

When accessing the ICSR register successively, insert one or more NOP instructions between the instructions used for access.

25.2.11 Slave Address Register (SAR)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FS	Format select bit	0: I2C bus format 1: Clock synchronous serial format	R/W
b1	SVA0	Slave address 6 to 0	Set an address different from that of the other slave devices connected to the I2C bus. When the 7 high-order bits of the first frame transmitted after the start condition match bits SVA0 to SVA6 in slave mode of the I2C bus format, the MCU operates as a slave device.	R/W
b2	SVA1			R/W
b3	SVA2			R/W
b4	SVA3			R/W
b5	SVA4			R/W
b6	SVA5			R/W
b7	SVA6			R/W

25.2.12 IIC bus Shift Register (ICDRS)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—

Bit	Function	R/W
b7 to b0	This register transmits and receives data. During transmission, data is transferred from registers ICRDT to ICDRS and transmitted from the SDA pin. During reception, data is transferred from registers ICDRS to the ICDRR after 1 byte of data is received.	—

25.3 Common Items for Multiple Modes

25.3.1 Transfer Clock

When the MST bit in the ICCR1 register is set to 0, the transfer clock is the external clock input from the SCL pin.
When the MST bit in the ICCR1 register is set to 1, the transfer clock is the internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and the transfer clock is output from the SCL pin.
Tables 25.3 and 25.4 list Transfer Rate Examples.

Table 25.3 Transfer Rate Examples(1)

PINSR Register		ICCR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	0	0	0	0	0	f1/28	179 kHz	286 kHz	357 kHz	571 kHz	714 kHz
					1	f1/40	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/48	104 kHz	167 kHz	208 kHz	333 kHz	417 kHz
					1	f1/64	78.1 kHz	125 kHz	156 kHz	250 kHz	313 kHz
			1	0	0	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/100	50.0 kHz	80.0 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz	179 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
		1	0	0	0	f1/56	89.3 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz	208 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
			1	0	0	f1/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz	125 kHz
					1	f1/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz	100 kHz
				1	0	f1/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz	89.3 kHz
					1	f1/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz	78.1 kHz

Table 25.4 Transfer Rate Examples (2)

PINSR Register		ICCR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	1	0	0	0	0	f1/28	358 kHz	572 kHz	714 kHz	1142 kHz	1428 kHz
					1	f1/40	250 kHz	400 kHz	500 kHz	800 kHz	1000 kHz
				1	0	f1/48	208 kHz	334 kHz	416 kHz	666 kHz	834 kHz
					1	f1/64	156 kHz	250 kHz	312 kHz	500 kHz	626 kHz
			1	0	0	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
					1	f1/100	100 kHz	160 kHz	200 kHz	320 kHz	400 kHz
				1	0	f1/112	89 kHz	143 kHz	179 kHz	286 kHz	358 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
		1	0	0	0	f1/56	179 kHz	286 kHz	358 kHz	572 kHz	714 kHz
					1	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/96	104 kHz	167 kHz	208 kHz	334 kHz	416 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
			1	0	0	f1/160	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/200	50 kHz	80 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/224	45 kHz	71 kHz	89 kHz	143 kHz	179 kHz
					1	f1/256	39 kHz	63 kHz	78 kHz	125 kHz	156 kHz
1	0	0	0	0	0	f1/28	90 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/40	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/48	52 kHz	84 kHz	104 kHz	167 kHz	209 kHz
					1	f1/64	39 kHz	63 kHz	78 kHz	125 kHz	157 kHz
			1	0	0	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
					1	f1/100	25 kHz	40 kHz	50 kHz	80 kHz	100 kHz
				1	0	f1/112	22 kHz	36 kHz	45 kHz	72 kHz	90 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
		1	0	0	0	f1/56	45 kHz	72 kHz	90 kHz	143 kHz	179 kHz
					1	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
				1	0	f1/96	26 kHz	42 kHz	52 kHz	84 kHz	104 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
			1	0	0	f1/160	16 kHz	25 kHz	31 kHz	50 kHz	63 kHz
					1	f1/200	13 kHz	20 kHz	25 kHz	40 kHz	50 kHz
				1	0	f1/224	11 kHz	18 kHz	22 kHz	36 kHz	45 kHz
					1	f1/256	10 kHz	16 kHz	20 kHz	31 kHz	39 kHz

25.3.2 SDA Pin Digital Delay Selection

The digital delay value for the SDA pin can be selected by bits SDADLY0 to SDADLY1 in the PINSR register. Figure 25.3 shows the Operating Example of Digital Delay for SDA Pin.

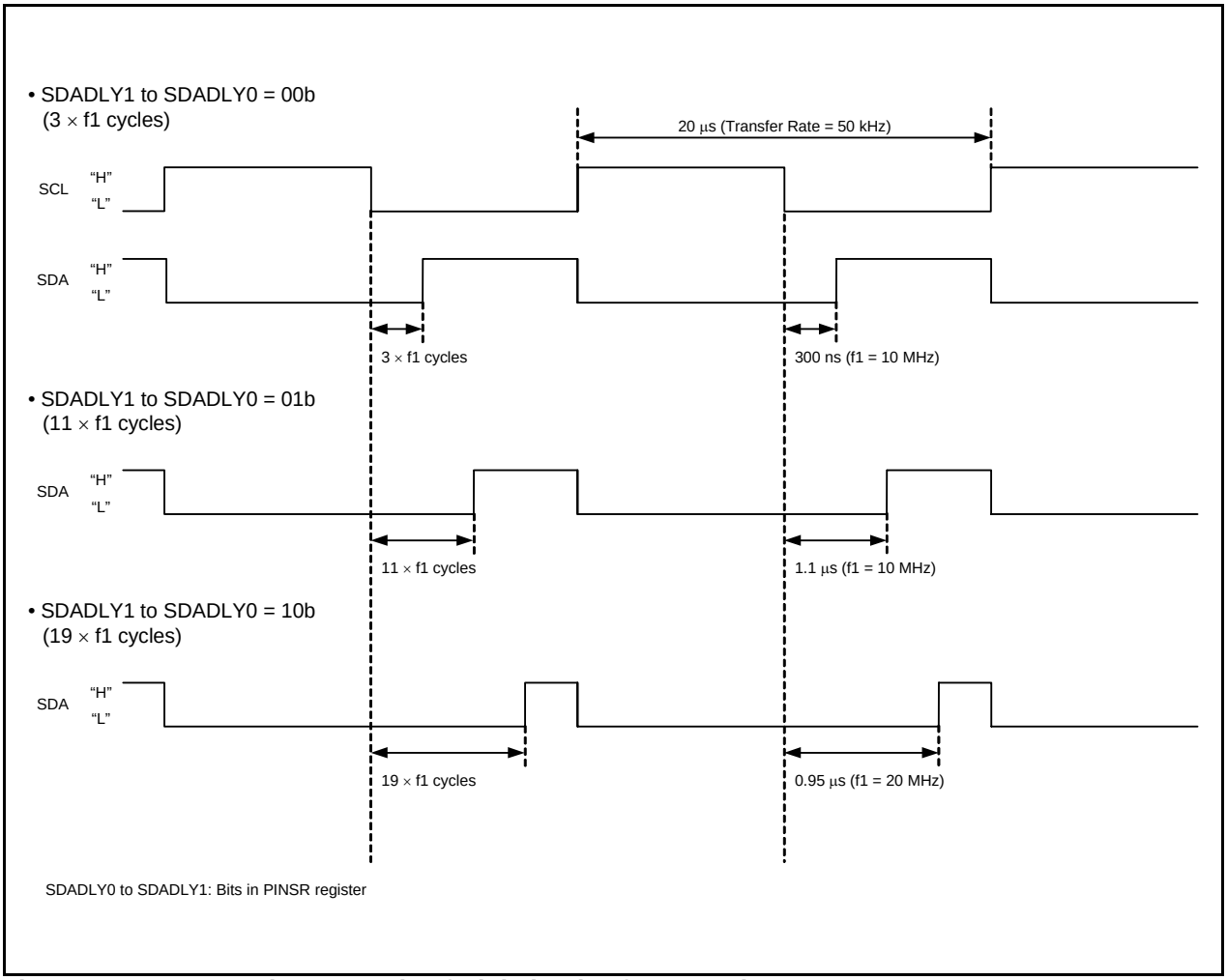


Figure 25.3 Operating Example of Digital Delay for SDA Pin

25.3.3 Interrupt Requests

The I2C bus interface has six interrupt requests when the I2C bus format is used and four interrupt requests when the clock synchronous serial format is used.

Table 25.5 lists the Interrupt Requests of I2C bus Interface.

Because these interrupt requests are allocated at the I2C bus interface interrupt vector table, the source must be determined bit by bit.

Table 25.5 Interrupt Requests of I2C bus Interface

Interrupt Request		Generation Condition	Format	
			I2C bus	Clock Synchronous Serial
Transmit data empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit end	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive data full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop condition detection	STPI	STIE = 1 and STOP = 1	Enabled	Disabled
NACK detection	NAKI	NAKIE = 1 and AL = 1 (or NAKIE = 1 and NACKF = 1)	Enabled	Disabled
Arbitration lost/overrun error			Enabled	Enabled

STIE, NAKIE, RIE, TEIE, TIE: Bits in ICIER register
AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in ICSR register

When generation conditions listed in Table 25.5 are met, an interrupt request of the I2C bus interface is generated. Set the interrupt generation conditions to 0 by the I2C bus interface interrupt routine.

However, bits TDRE and TEND are automatically set to 0 by writing transmit data to the ICDRT register and the RDRF bit is automatically set to 0 by reading the ICDRR register. In particular, the TDRE bit is set to 0 when transmit data is written to the ICDRT register and set to 1 when data is transferred from the ICDRT register to the ICDRS register. If the TDRE bit is further set to 0, additional 1 byte may be transmitted.
Also, set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit is set to 0.

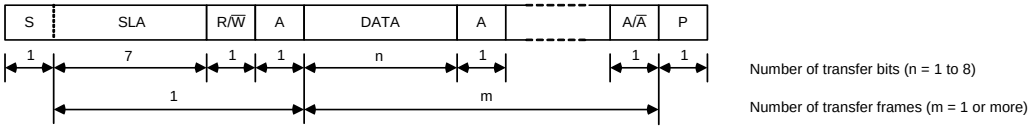
25.4 I2C bus Interface Mode

25.4.1 I2C bus Format

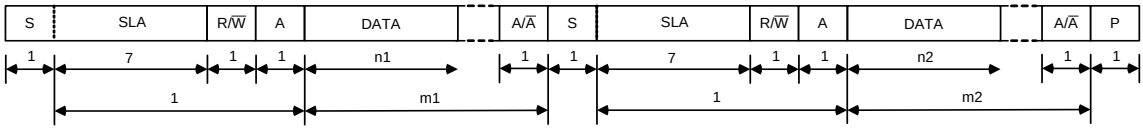
When the FS bit in the SAR register is set to 0, the I2C bus format is used for communication.
Figure 25.4 shows the I2C bus Format and Bus Timing. The first frame following the start condition consists of 8 bits.

(1) I2C bus format

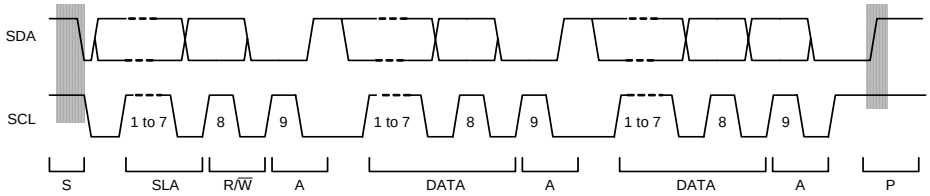
(a) I2C bus format (FS = 0)



(b) I2C bus format When Start Condition is Retransmitted (FS = 0)



(2) I2C bus timing



Legend:
S : Start condition
The master device changes the SDA signal from high to low while the SCL signal is held high.
SLA : Slave address
R/W : Indicates the direction of data transmission/reception
Data is transmitted when:
R/W value is 1: From the slave device to the master device
R/W value is 0: From the master device to the slave device
A : Acknowledge
The receive device sets the SDA signal to low.
DATA : Transmit/receive data
P : Stop condition
The master device changes the SDA signal from low to high while the SCL signal is held high.

Figure 25.4 I2C bus Format and Bus Timing

25.4.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 25.5 and 25.6 show the Operating Timing in Master Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in master transmit mode are as follows:

(1) Set the STOP bit in the ICSR register to 0 for initialization, and set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then, set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting).

(2) After confirming that the bus is released by reading the BBSY bit in the ICCR2 register, set bits TRS and MST in the ICCR1 register to master transmit mode. Then, write 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction (start condition generated). This will generate a start condition.

(3) After confirming that the TDRE bit in the ICSR register is set to 1 (data is transferred from registers ICDRT to ICDRS), write transmit data to the ICDRT register (data in which a slave address and R/$\overline{W}$ are indicated in the 1st byte). At this time, the TDRE bit is automatically set to 0. When data is transferred from registers ICDRT to ICDRS, the TDRE bit is set to 1 again.

(4) When 1 byte of data transmission is completed while the TDRE bit is set to 1, the TEND bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the transmit clock. After confirming that the slave device is selected by reading the ACKBR bit in the ICIER register, write the 2nd byte of data to the ICDRT register. Since the slave device is not acknowledged when the ACKBR bit is set to 1, generate a stop condition. Stop condition generation is enabled by writing 0 to the BBSY bit and 0 to the SCP bit with the MOV instruction. The SCL signal is fixed low until data is ready or a stop condition is generated.

(5) Write the transmit data after the 2nd byte to the ICDRT register every time the TDRE bit is set to 1.

(6) When the number of bytes to be transmitted is written to the ICDRT register, wait until the TEND bit is set to 1 while the TDRE bit is set to 1. Or wait for NACK (NACKF bit in ICSR register = 1) from the receive device while the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted). Then, generate a stop condition before setting the TEND bit or the NACKF bit to 0.

(7) When the STOP bit in the ICSR register is set to 1, return to slave receive mode.

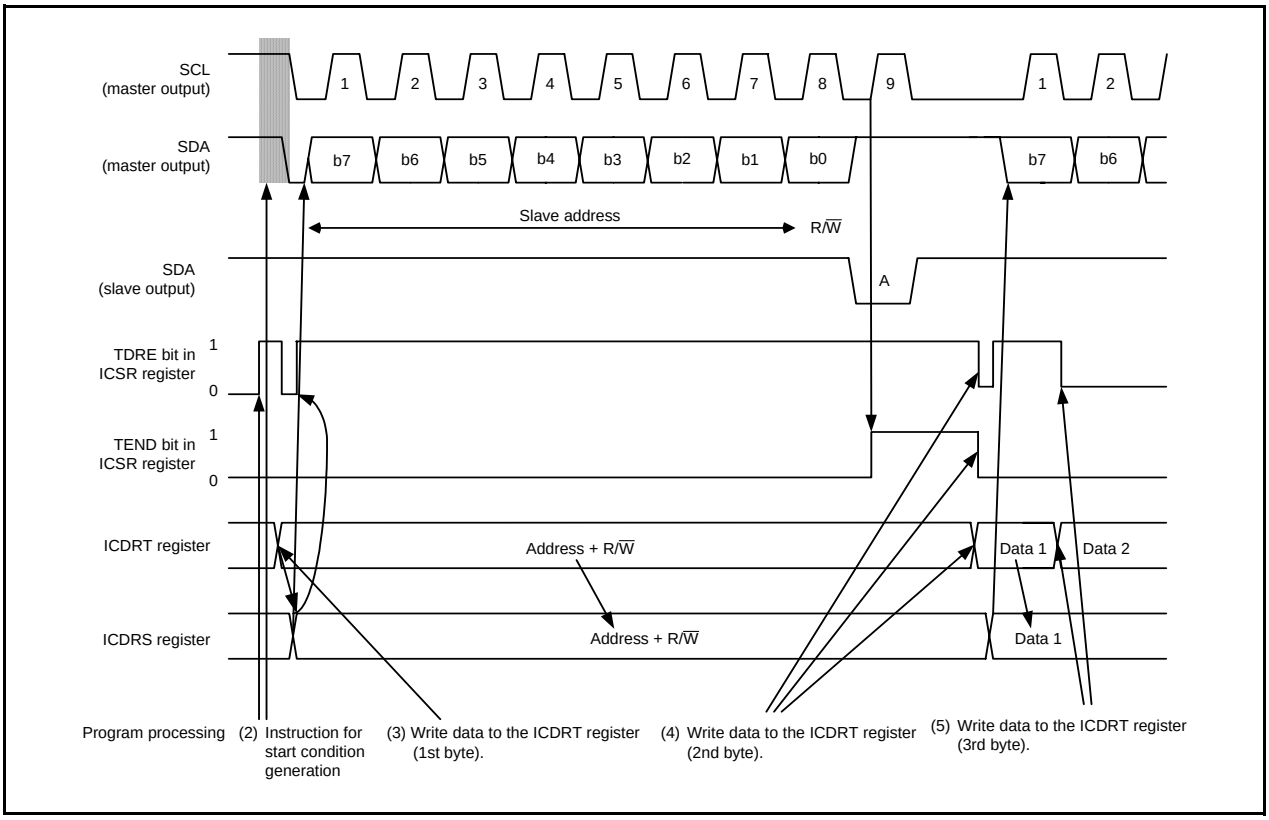


Figure 25.5 Operating Timing in Master Transmit Mode (I2C bus Interface Mode) (1)

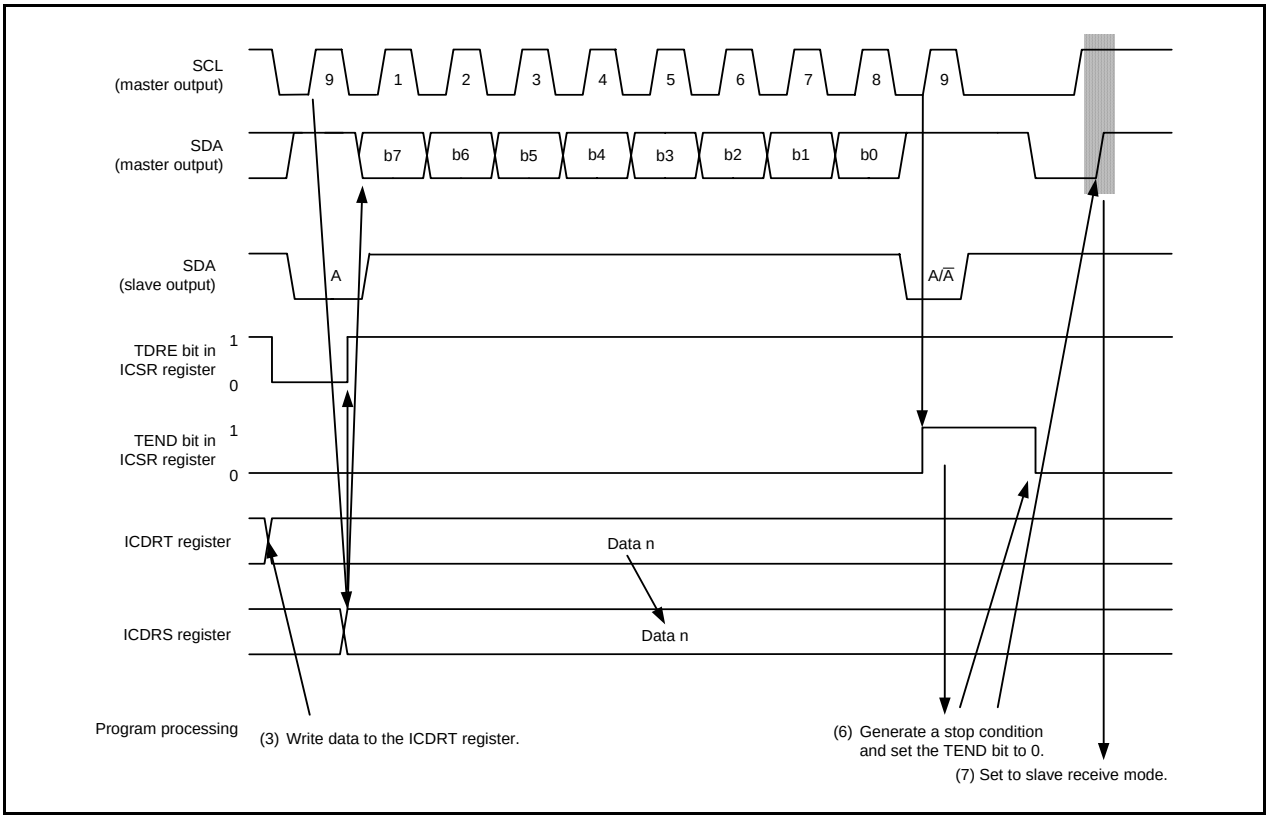


Figure 25.6 Operating Timing in Master Transmit Mode (I2C bus Interface Mode) (2)

25.4.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal. Figures 25.7 and 25.8 show the Operating Timing in Master Receive Mode (I2C bus Interface Mode).

The receive procedure and operation in master receive mode are as follows:

(1) After setting the TEND bit in the ICSR register to 0, set the TRS bit in the ICCR1 register to 0 to switch from master transmit mode to master receive mode. Then set the TDRE bit in the ICSR register to 0.
(2) Dummy reading the ICDRR register starts receive operation. The receive clock is output in synchronization with the internal clock and data is received. The master device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle of the receive clock.
(3) When one frame of data reception is completed, the RDRF bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the receive clock. If the ICDRR register is read at this time, the received data can be read and the RDRF bit is set to 0 simultaneously.
(4) Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If reading the ICDRR register is delayed by another process and the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed low until the ICDRR register is read.
(5) If the next frame is the last receive frame and the RCVD bit in the ICCR1 register is set to 1 (next receive operation disabled) before reading the ICDRR register, stop condition generation is enabled after the next receive operation.
(6) When the RDRF bit is set to 1 at the rising edge of the 9th clock cycle of the receive clock, generate a stop condition. When a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle. Refer to **25.9 Notes on I2C bus Interface**.
(7) When the STOP bit in the ICSR register is set to 1, read the ICDRR register and set the RCVD bit to 0 (next receive operation continues).
(8) Return to slave receive mode.

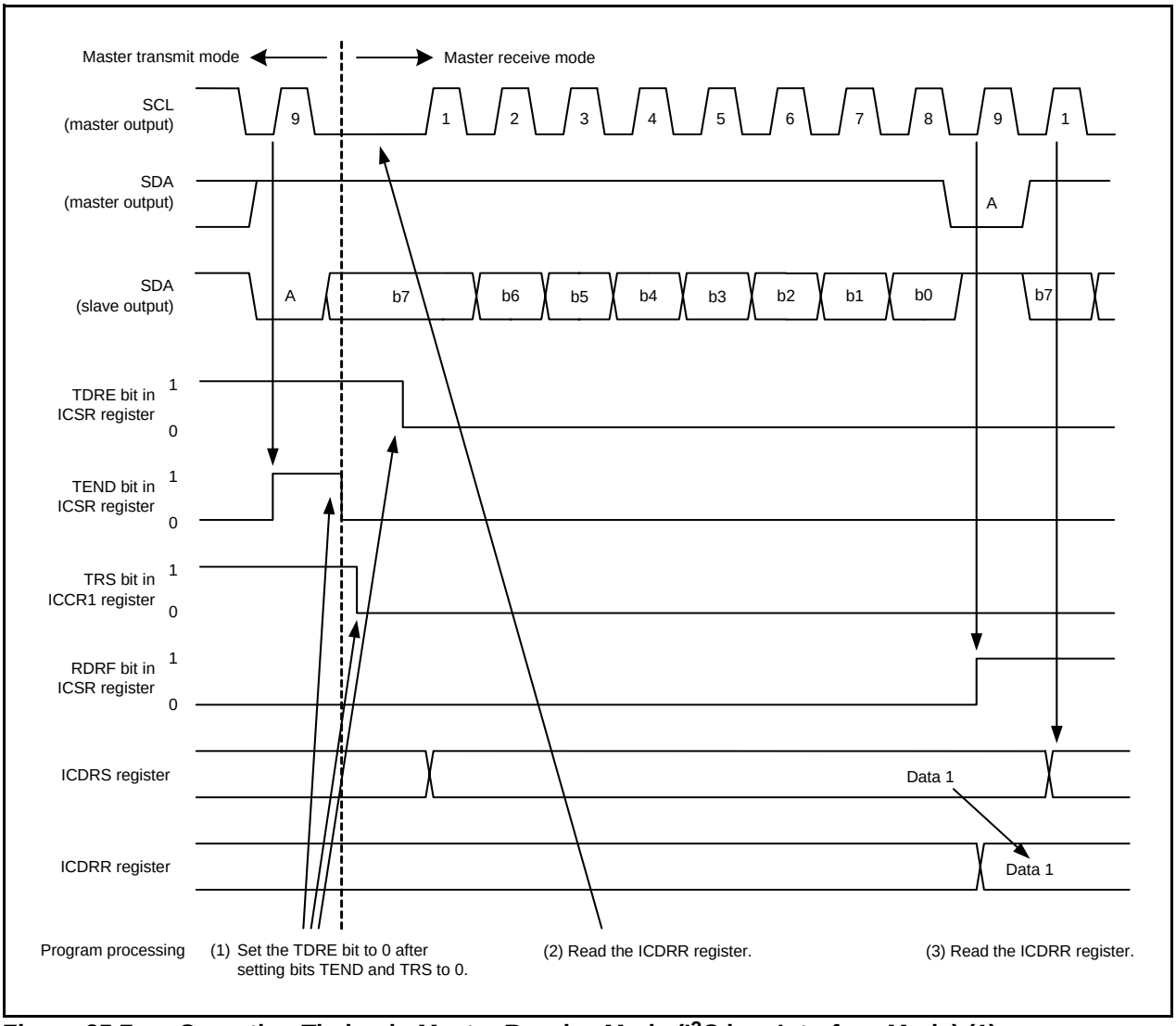


Figure 25.7 Operating Timing in Master Receive Mode (I2C bus Interface Mode) (1)

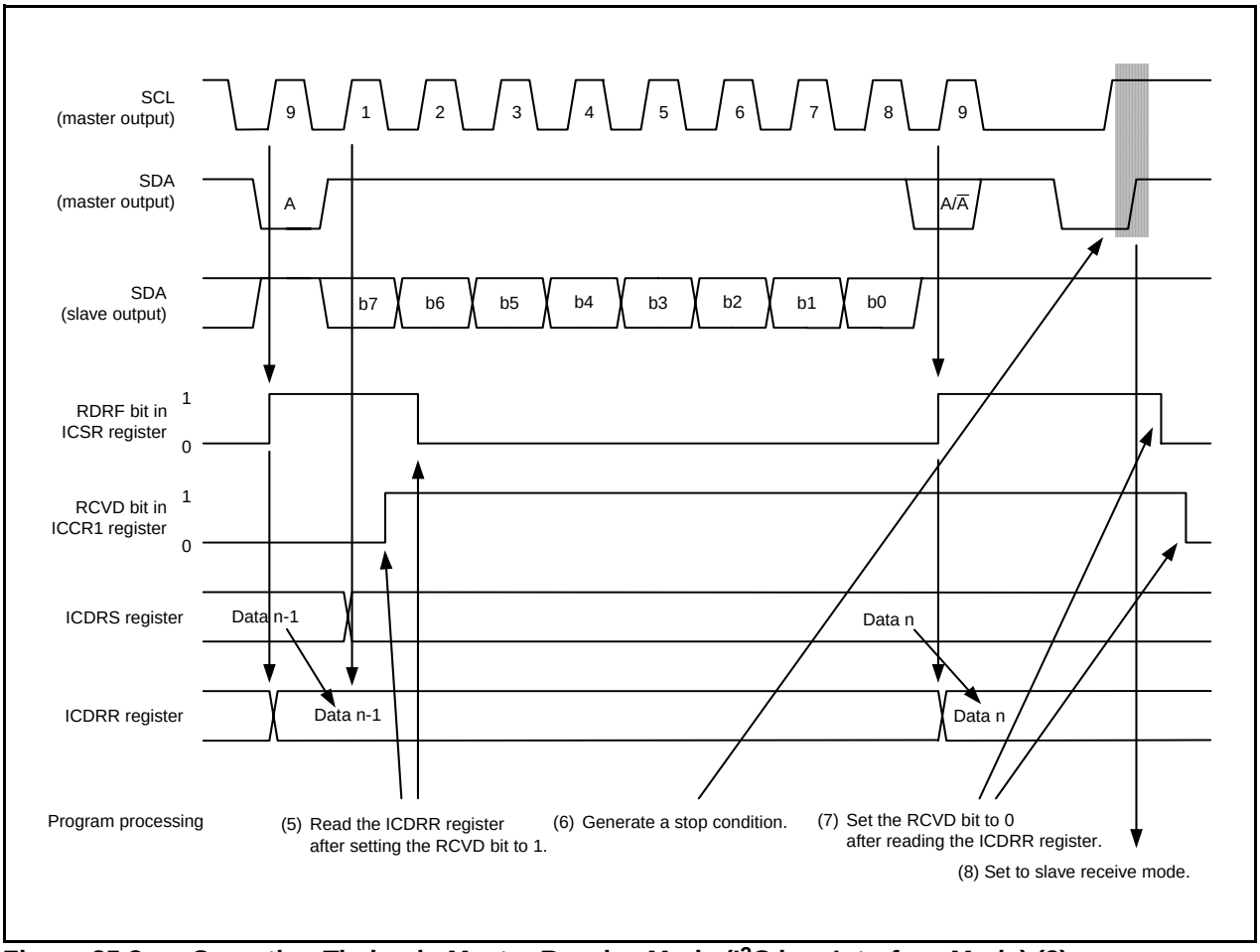


Figure 25.8 Operating Timing in Master Receive Mode (I2C bus Interface Mode) (2)

25.4.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal.

Figures 25.9 and 25.10 show the Operating Timing in Slave Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in slave transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. If the 8th bit of data (R/$\overline{W}$) is 1 at this time, bits TRS and TDRE in the ICSR register are set to 1, and the mode is switched to slave transmit mode automatically. Continuous transmission is enabled by writing transmit data to the ICDRT register every time the TDRE bit is set to 1.

(3) When the TDRE bit in the ICDRT register is set to 1 after the last transmit data is written to the ICDRT register, wait until the TEND bit in the ICSR register is set to 1 while the TDRE bit is set to 1. When the TEND bit is set to 1, set the TEND bit to 0.

(4) Set the TRS bit to 0 and dummy read the ICDRR register to end the process. This will release the SCL signal.

(5) Set the TDRE bit to 0.

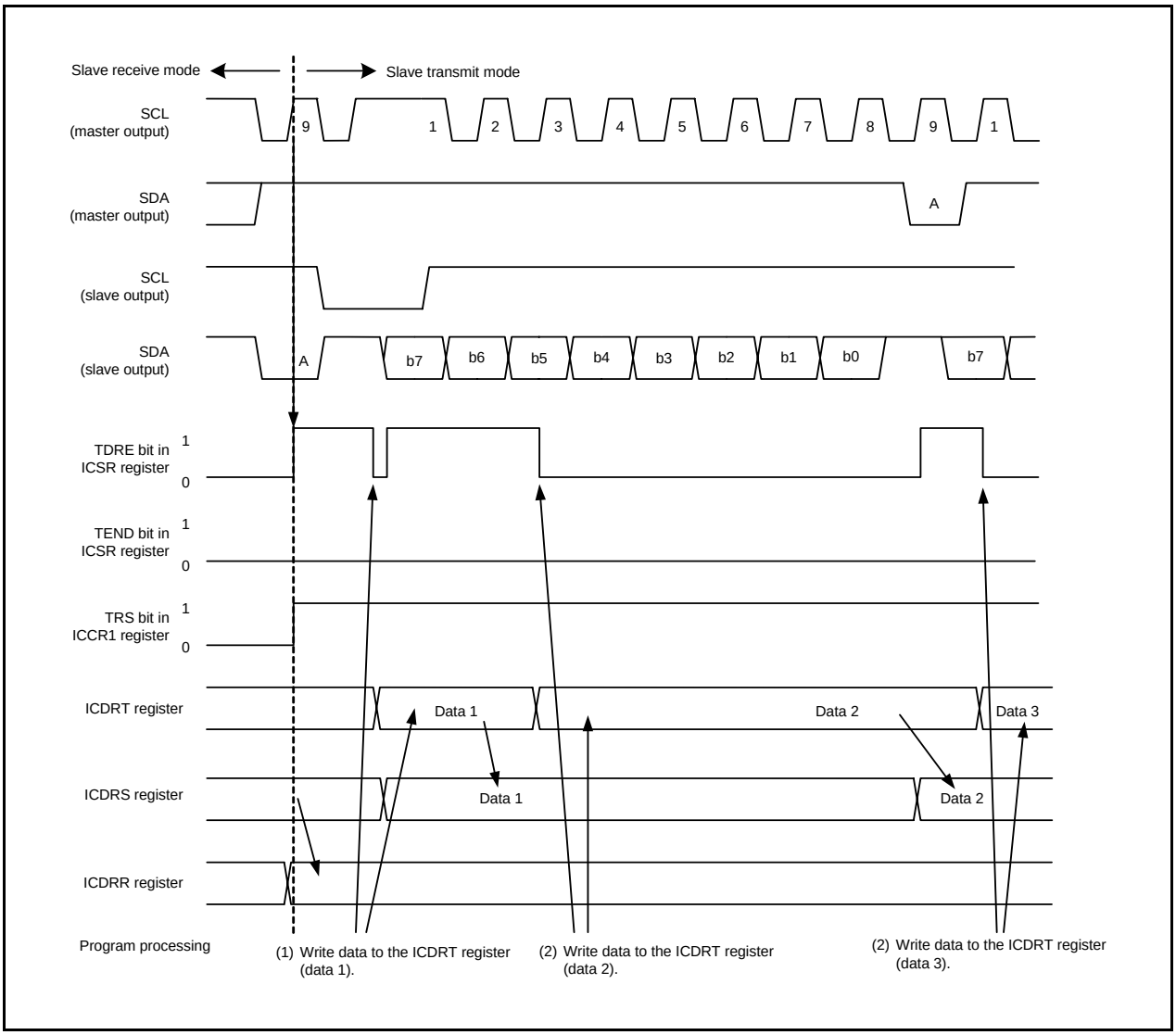


Figure 25.9 Operating Timing in Slave Transmit Mode (I2C bus Interface Mode) (1)

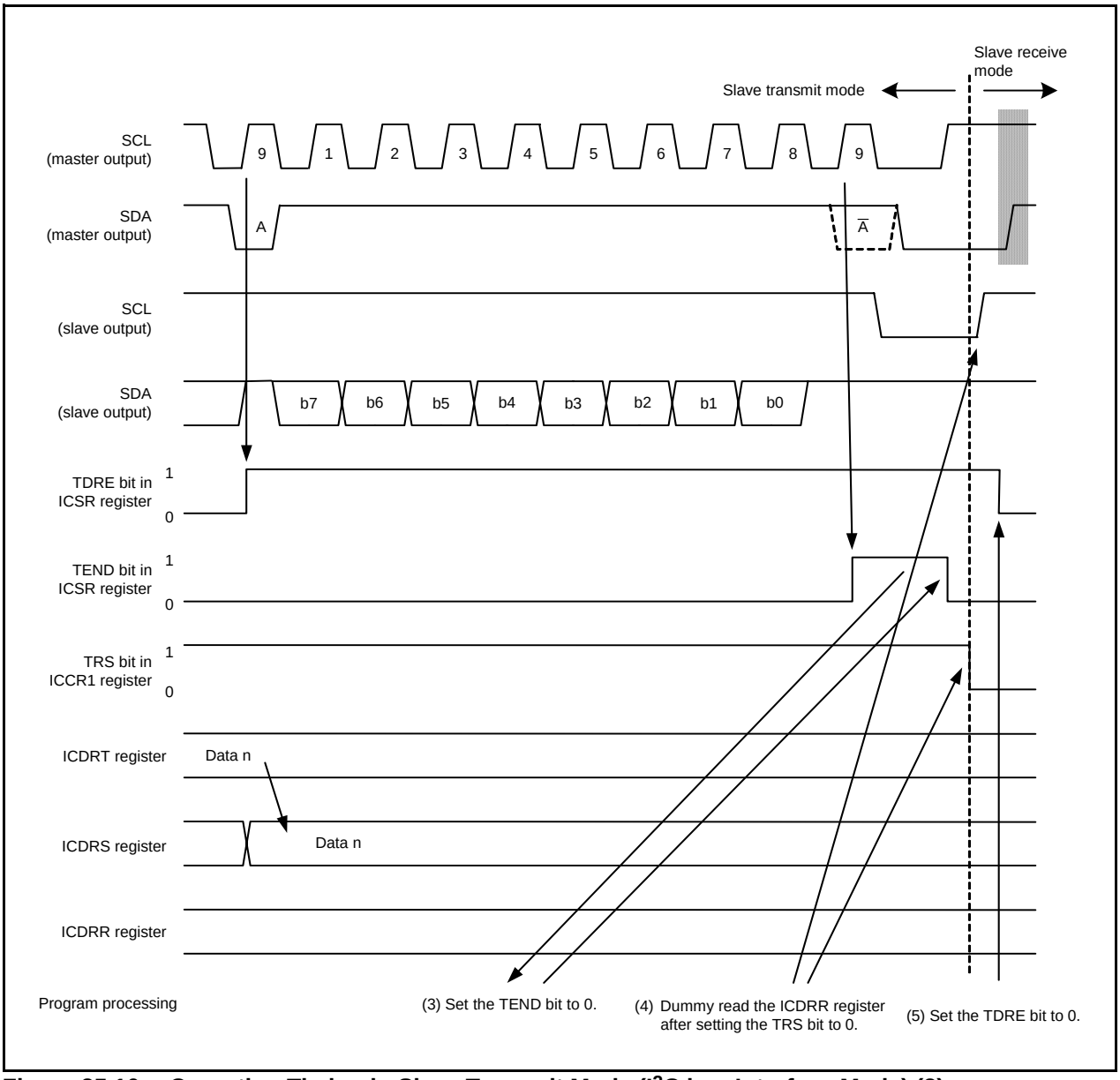


Figure 25.10 Operating Timing in Slave Transmit Mode (I2C bus Interface Mode) (2)

25.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 25.11 and 25.12 show the Operating Timing in Slave Receive Mode (I2C bus Interface Mode).

The receive procedure and operation in slave receive mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. Since the RDRF bit in the ICSR register is set to 1 simultaneously, dummy read the ICDRR register (the read data is unnecessary because it indicates the slave address and R/W).

(3) Read the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed low until the ICDRR register is read. The setting change of the acknowledge signal returned to the master device before reading the ICDRR register takes affect from the following transfer frame.

(4) Reading the last byte is also performed by reading the ICDRR register.

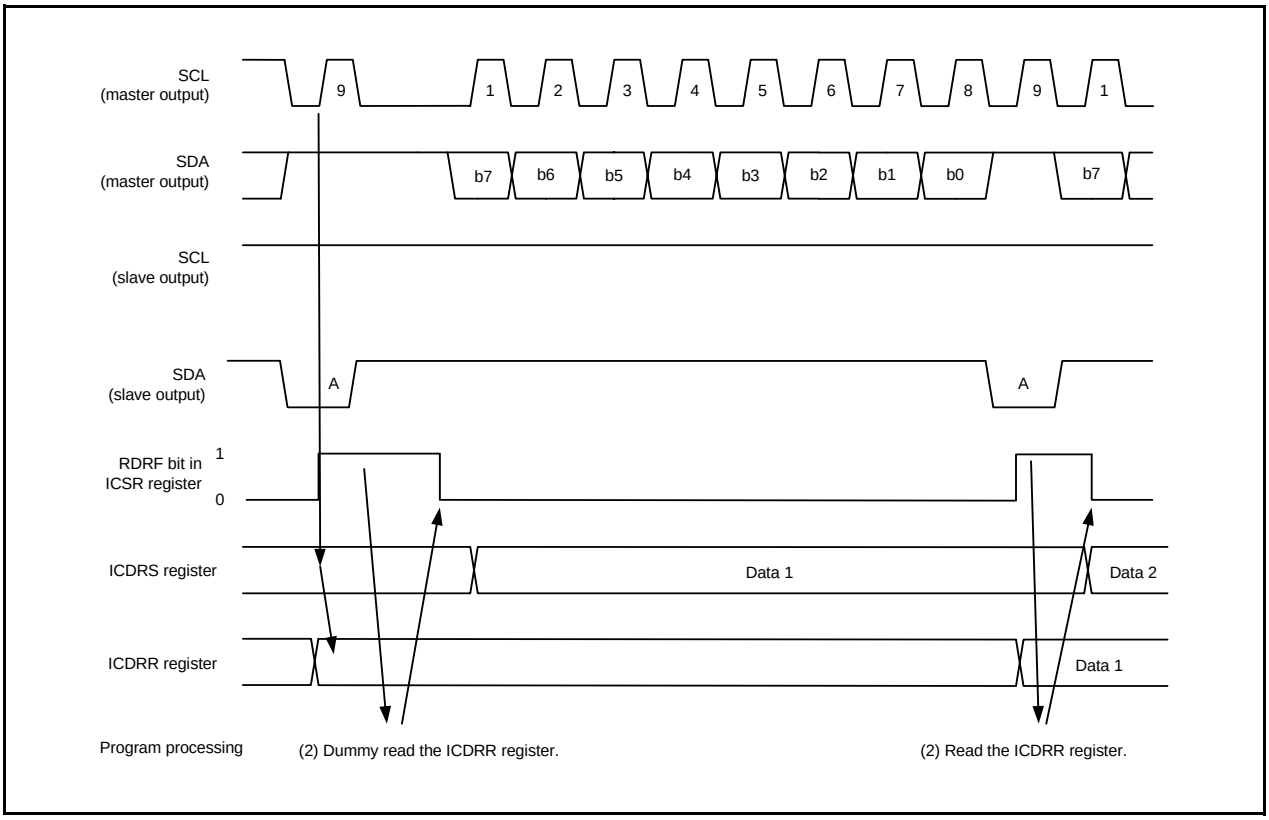


Figure 25.11 Operating Timing in Slave Receive Mode (I2C bus Interface Mode) (1)

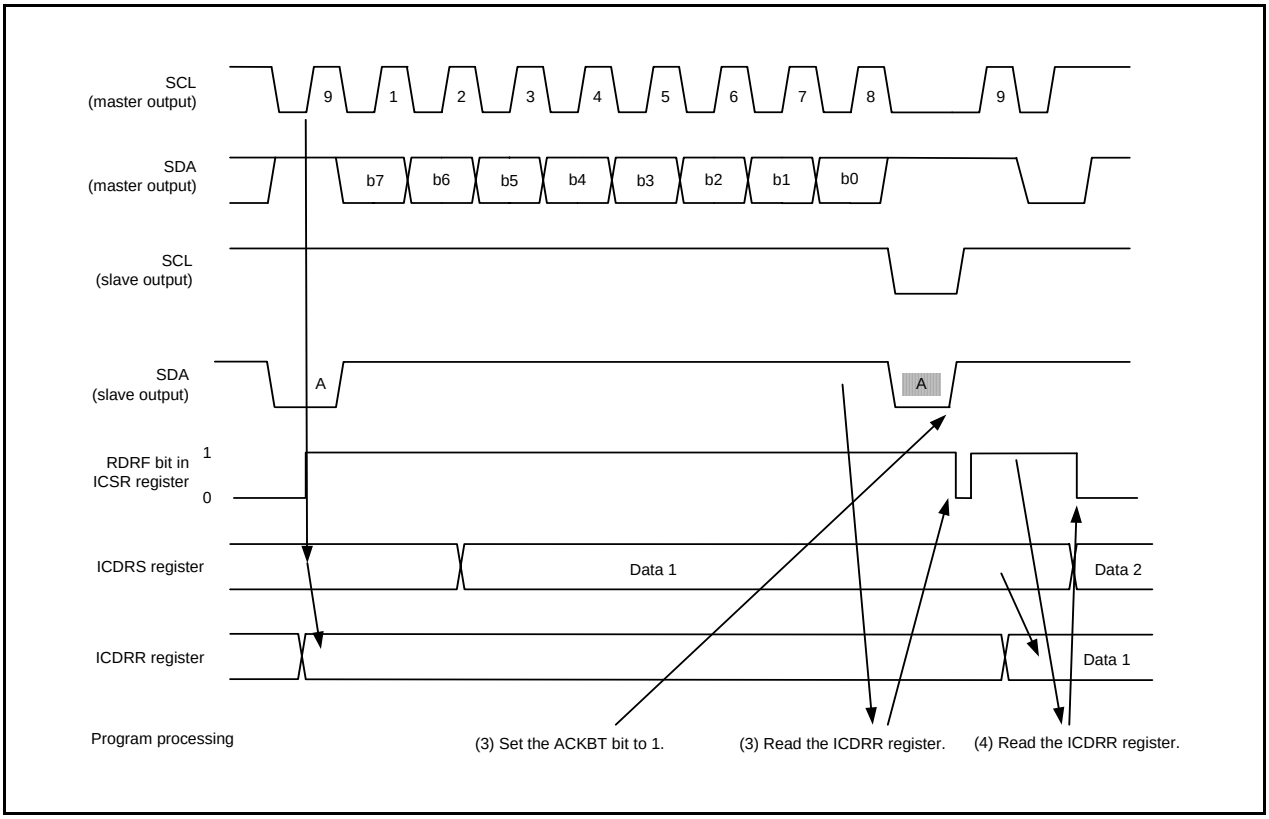


Figure 25.12 Operating Timing in Slave Receive Mode (I2C bus Interface Mode) (2)

25.5 Clock Synchronous Serial Mode

25.5.1 Clock Synchronous Serial Format

When the FS bit in the SAR register is set to 1, the clock synchronous serial format is used for communication. Figure 25.13 shows the Transfer Format of Clock Synchronous Serial Format.

When the MST bit in the ICCR1 register is set to 1, the transfer clock is output from the SCL pin. When the MST bit is set to 0, the external clock is input.

The transfer data is output between successive falling edges of the SCL clock, and data is determined at the rising edge of the SCL clock. MSB first or LSB first can be selected as the order of the data transfer by setting the MLS bit in the ICMR register. The SDA output level can be changed by the SDAO bit in the ICCR2 register during transfer standby.

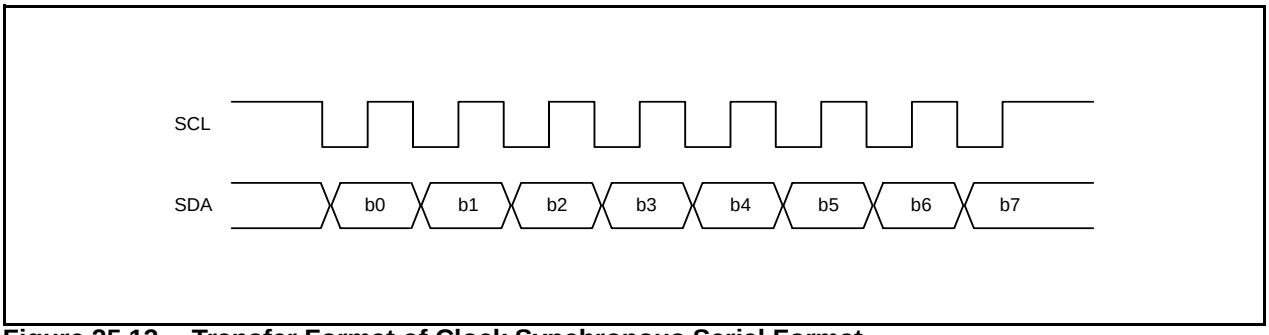


Figure 25.13 Transfer Format of Clock Synchronous Serial Format

25.5.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin in synchronization with the falling edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 25.14 shows the Operating Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the TRS bit in the ICCR1 register to 1 to select transmit mode. This will set the TDRE bit in the ICSR register is to 1.
(3) After confirming that the TDRE bit is set to 1, write transmit data to the ICDRT register. Data is transferred from registers ICDRT to ICDRS and the TDRE bit is automatically set to 1. Continuous transmission is enabled by writing data to the ICDRT register every time the TDRE bit is set to 1. To switch from transmit to receive mode, set the TRS bit to 0 while the TDRE bit is set to 1.

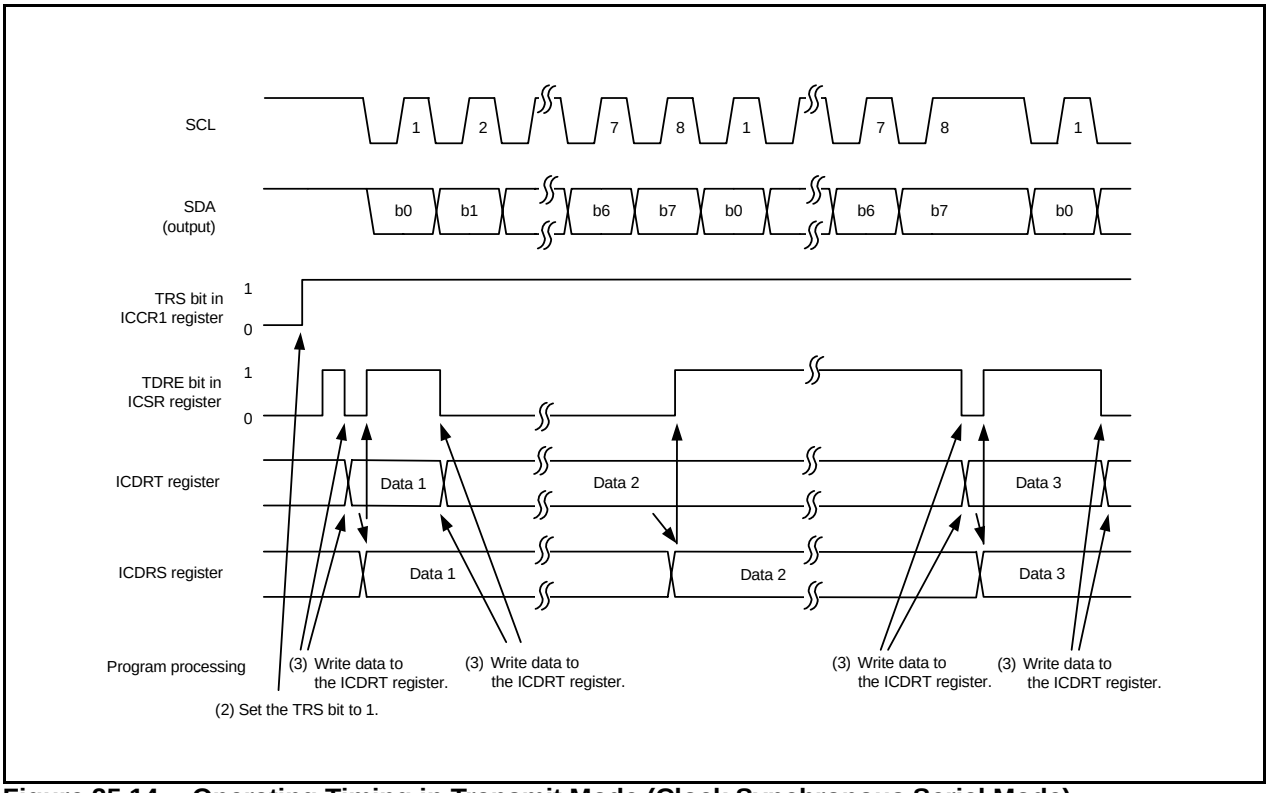


Figure 25.14 Operating Timing in Transmit Mode (Clock Synchronous Serial Mode)

25.5.3 Receive Operation

In receive mode, data is latched at the rising edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 25.15 shows the Operating Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are as follows:

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the MST bit to 1 while the transfer clock is being output. This will start the output of the receive clock.
(3) When the receive operation is completed, data is transferred from registers ICDRS to ICDRR and the RDRF bit in the ICSR register is set to 1. When the MST bit is set to 1, the clock is output continuously since the next byte of data is enabled for reception. Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, an overrun is detected and the AL bit in the ICSR register is set to 1. At this time, the last receive data is retained in the ICDRR register.
(4) When the MST bit is set to 1, set the RCVD bit in the ICCR1 register to 1 (next receive operation disabled) and read the ICDRR register. The SCL signal is fixed high after the following byte of data reception is completed.

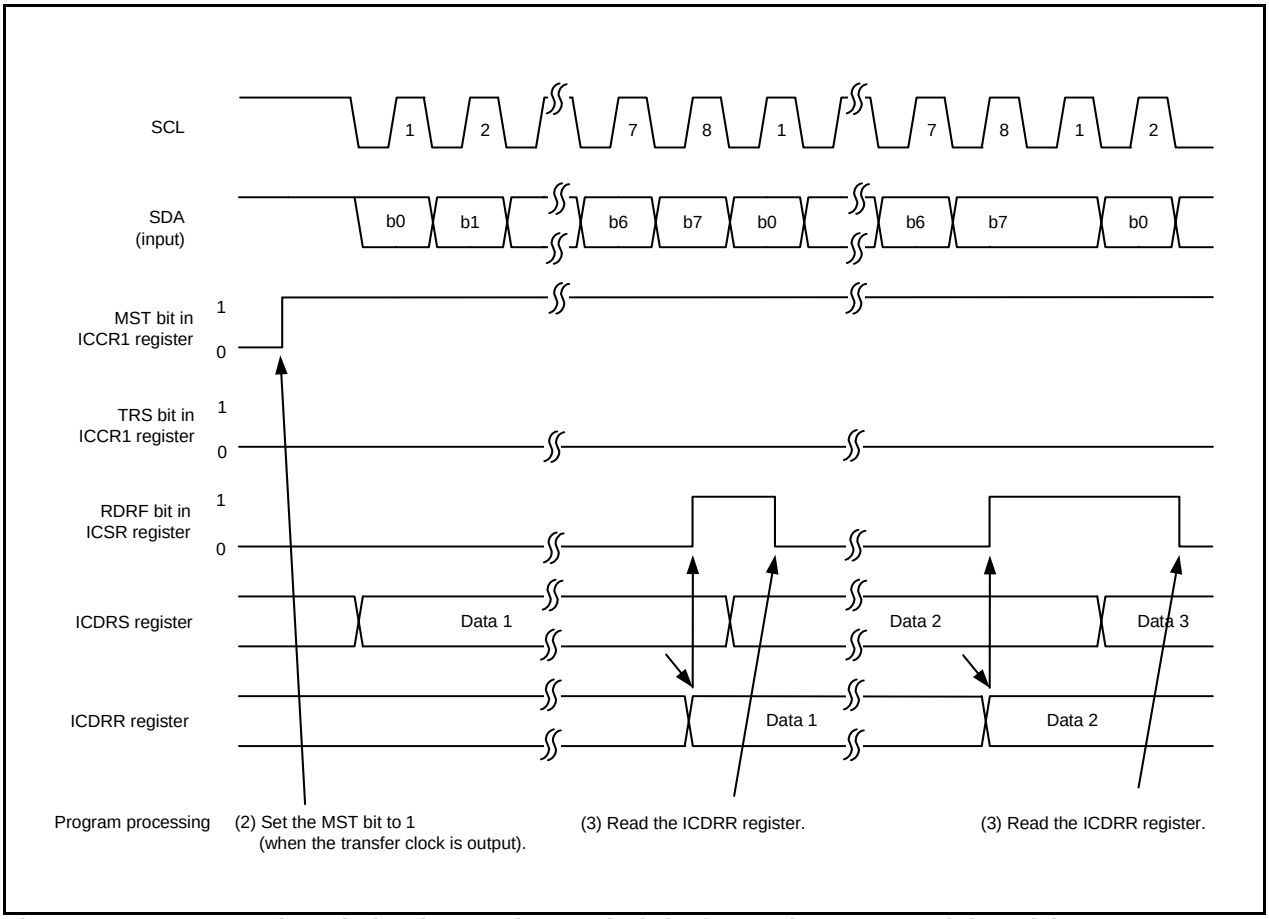


Figure 25.15 Operating Timing in Receive Mode (Clock Synchronous Serial Mode)

25.6 Register Setting Examples

Figures 25.16 to 25.19 show Register Setting Examples when using I2C bus interface.

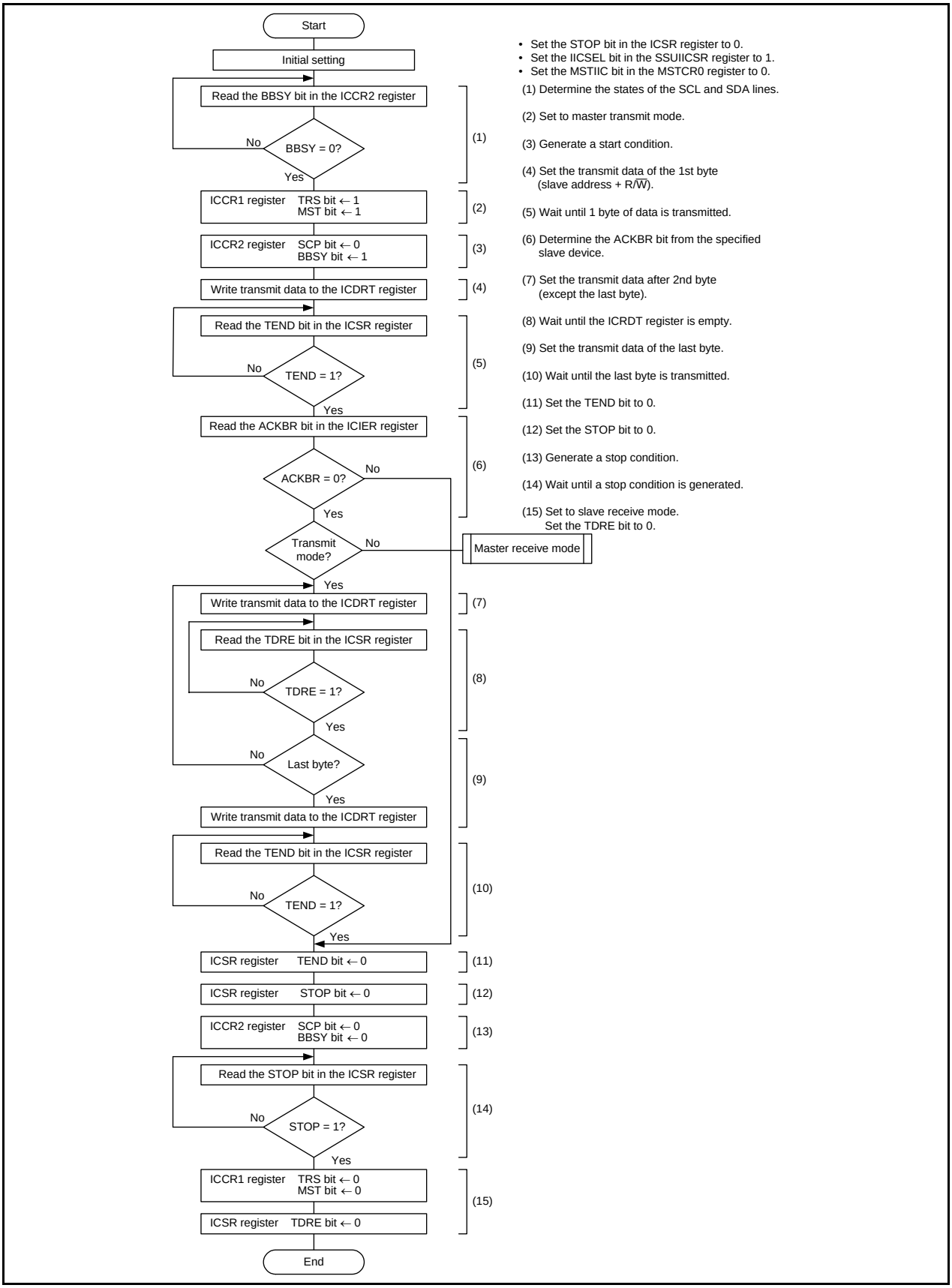
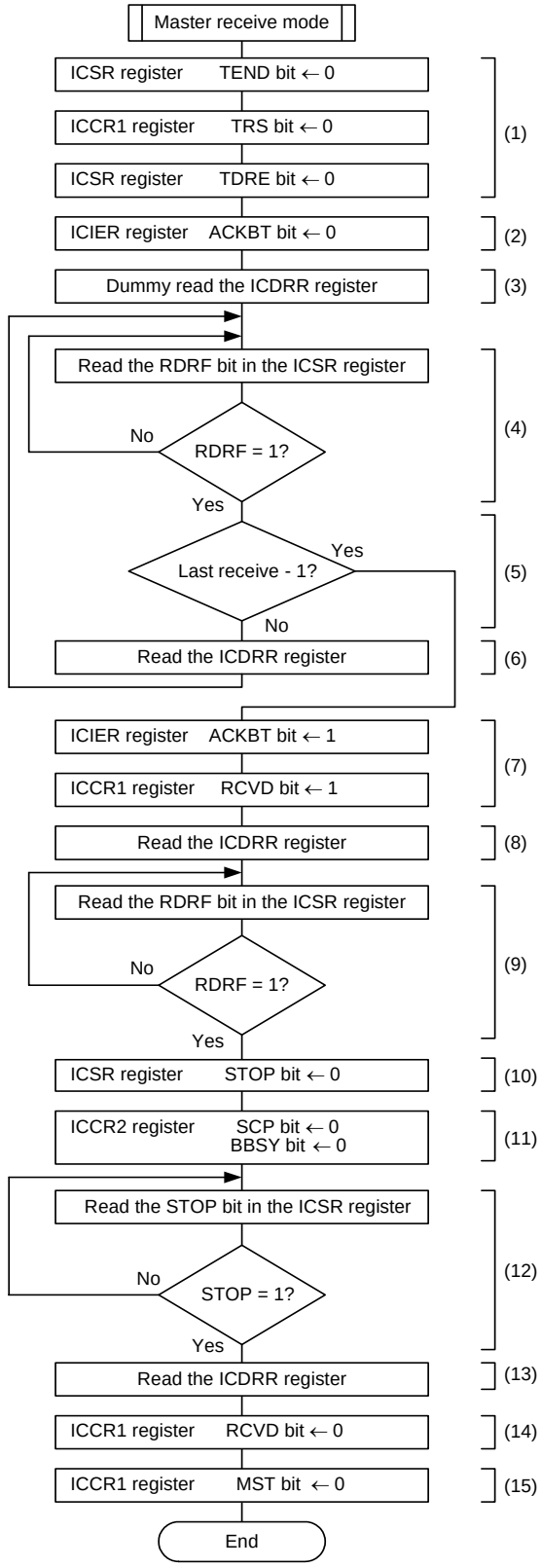

Start
Initial setting
Read the BBSY bit in the ICCR2 register
No
BBSY = 0?
Yes
ICCR1 register TRS bit ← 1 MST bit ← 1
ICCR2 register SCP bit ← 0 BBSY bit ← 1
Write transmit data to the ICDRT register
Read the TEND bit in the ICSR register
No
TEND = 1?
Yes
Read the ACKBR bit in the ICIER register
ACKBR = 0?
No
Yes
Transmit mode?
No
Master receive mode
Yes
Write transmit data to the ICDRT register
Read the TDRE bit in the ICSR register
No
TDRE = 1?
Yes
No
Last byte?
Yes
Write transmit data to the ICDRT register
Read the TEND bit in the ICSR register
No
TEND = 1?
Yes
ICSR register TEND bit ← 0
ICSR register STOP bit ← 0
ICCR2 register SCP bit ← 0 BBSY bit ← 0
Read the STOP bit in the ICSR register
No
STOP = 1?
Yes
ICCR1 register TRS bit ← 0 MST bit ← 0
ICSR register TDRE bit ← 0
End
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
(14)
(15)
• Set the STOP bit in the ICSR register to 0.
• Set the IICSEL bit in the SSUIICSR register to 1.
• Set the MSTIIC bit in the MSTCR0 register to 0.
(1) Determine the states of the SCL and SDA lines.
(2) Set to master transmit mode.
(3) Generate a start condition.
(4) Set the transmit data of the 1st byte (slave address + R/W).
(5) Wait until 1 byte of data is transmitted.
(6) Determine the ACKBR bit from the specified slave device.
(7) Set the transmit data after 2nd byte (except the last byte).
(8) Wait until the ICRDT register is empty.
(9) Set the transmit data of the last byte.
(10) Wait until the last byte is transmitted.
(11) Set the TEND bit to 0.
(12) Set the STOP bit to 0.
(13) Generate a stop condition.
(14) Wait until a stop condition is generated.
(15) Set to slave receive mode. Set the TDRE bit to 0.

Figure 25.16 Register Setting Example in Master Transmit Mode (I2C bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Set the TDRE bit to 0. (1,2)

(2) Set the ACKBT bit to the transmit device. (1)

(3) Dummy read the ICDRR register. (1)

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte and set continuous receive operation to disable (RCVD = 1). (2)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Set the STOP bit to 0.

(11) Generate a stop condition.

(12) Wait until a stop condition is generated.

(13) Read the receive data of the last byte.

(14) Set the RCVD bit to 0.

(15) Set to slave receive mode.

Notes:
1. Do not generate interrupts while processing steps (1) to (3).
2. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read from the ICDRR register.

Figure 25.17 Register Setting Example in Master Receive Mode (I2C bus Interface Mode)

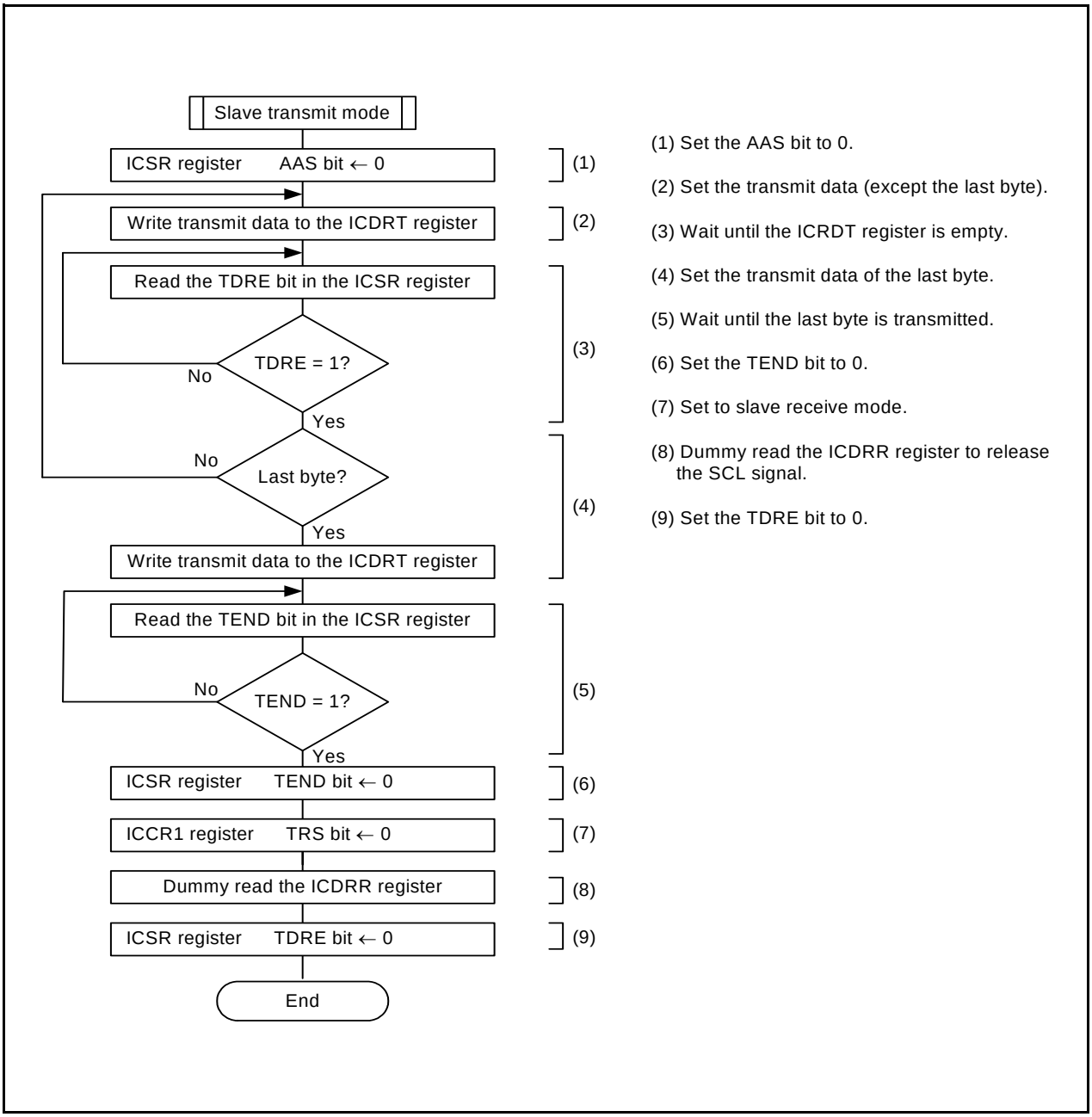
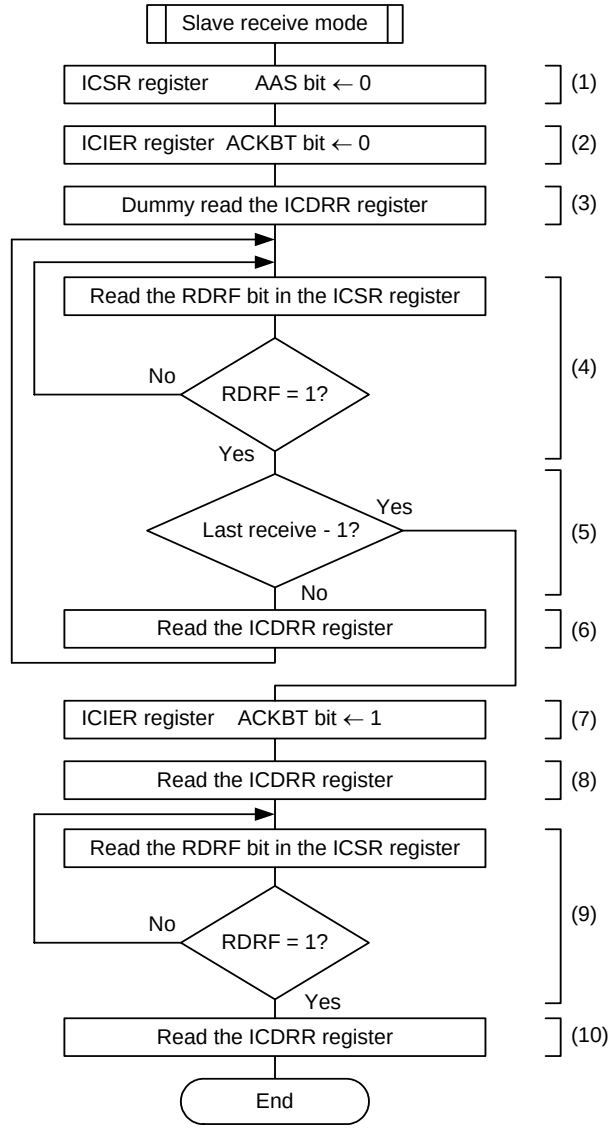

Slave transmit mode
ICSR register AAS bit ← 0
Write transmit data to the ICDRT register
Read the TDRE bit in the ICSR register
TDRE = 1?
No
Yes
Last byte?
No
Yes
Write transmit data to the ICDRT register
Read the TEND bit in the ICSR register
TEND = 1?
No
Yes
ICSR register TEND bit ← 0
ICCR1 register TRS bit ← 0
Dummy read the ICDRR register
ICSR register TDRE bit ← 0
End
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(1) Set the AAS bit to 0.
(2) Set the transmit data (except the last byte).
(3) Wait until the ICRDT register is empty.
(4) Set the transmit data of the last byte.
(5) Wait until the last byte is transmitted.
(6) Set the TEND bit to 0.
(7) Set to slave receive mode.
(8) Dummy read the ICDRR register to release the SCL signal.
(9) Set the TDRE bit to 0.

Figure 25.18 Register Setting Example in Slave Transmit Mode (I2C bus Interface Mode)



(1) Set the AAS bit to 0. (1)

(2) Set the ACKBT bit to the transmit device.

(3) Dummy read the ICDRR register.

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte. (1)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Read the receive data of the last byte.

Note:
1. For 1 byte of data reception, skip steps (2) to (6) after (1) and jump to process step (7). Process step (8) is a dummy read from the ICDRR register.

Figure 25.19 Register Setting Example in Slave Receive Mode (I2C bus Interface Mode)

25.7 Noise Canceller

The states of pins SCL and SDA are routed through the noise canceller before being latched internally.
Figure 25.20 shows a Block Diagram of Noise Canceller.
The noise canceller consists of two cascaded latch and match detector circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and two latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

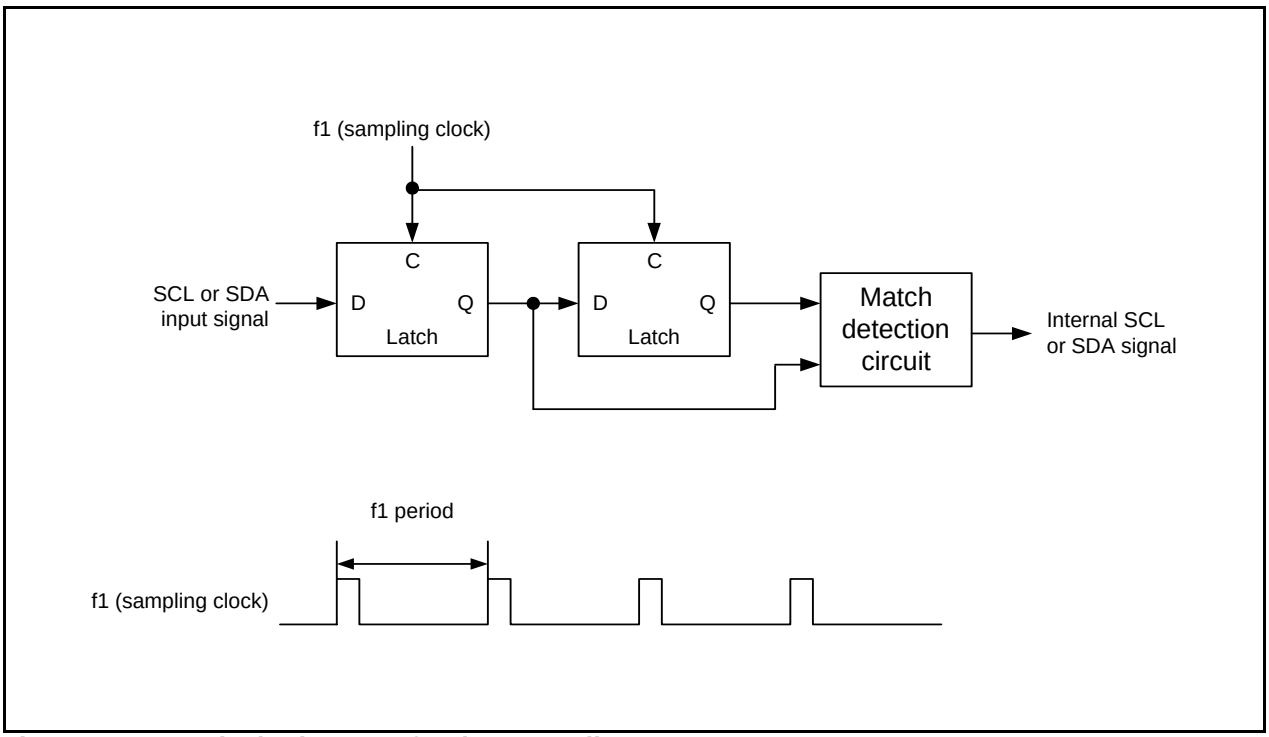


Figure 25.20 Block Diagram of Noise Canceller

25.8 Bit Synchronization Circuit

When the I2C bus interface is set to master mode, the high-level period may become shorter if:

- The SCL signal is held low by a slave device.
- The rise speed of the SCL signal is reduced by a load (load capacity or pull-up resistor) on the SCL line.

Therefore, the SCL signal is monitored and communication is synchronized bit by bit.

Figure 25.21 shows the Bit Synchronization Circuit Timing and Table 25.6 lists the Time between Changing SCL Signal from Low-Level Output to High-Impedance and Monitoring SCL Signal.

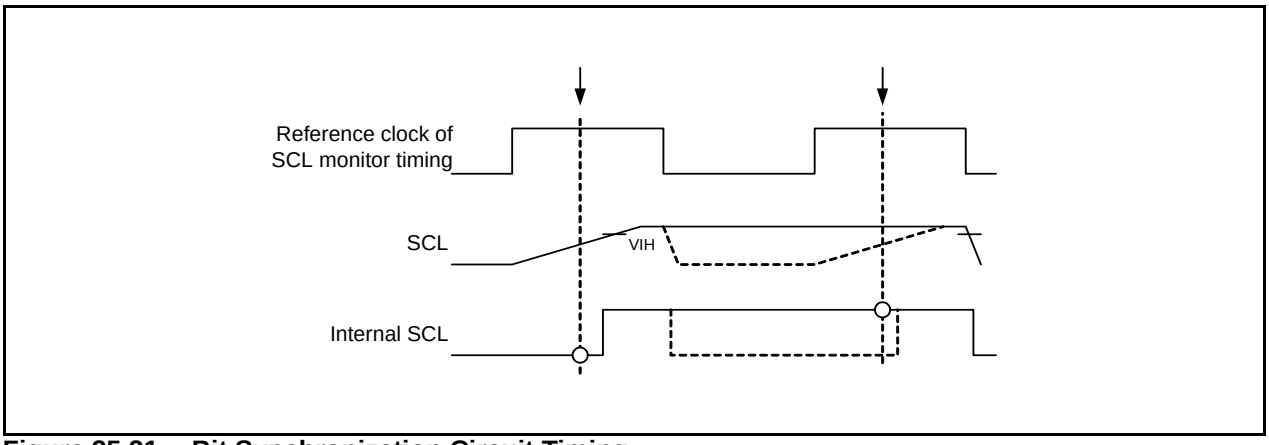


Figure 25.21 Bit Synchronization Circuit Timing

Table 25.6 Time between Changing SCL Signal from Low-Level Output to High-Impedance and Monitoring SCL Signal

ICCR1 Register		SCL Monitoring Time
CKS3	CKS2	
0	0	7.5Tcyc
	1	19.5Tcyc
1	0	17.5Tcyc
	1	41.5Tcyc

1Tcyc = 1/f1(s)

25.9 Notes on I2C bus Interface

To use the I2C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I2C bus interface function selected).

25.9.1 Master Receive Mode

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

25.9.1.1 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.
Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

25.9.2 The ICE Bit in the ICCR1 Register and the IICRST Bit in the ICCR2 Register

When writing 0 to the ICE bit or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

25.9.2.1 Conditions When Bits Become Undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

25.9.2.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

25.9.2.3 Additional Descriptions Regarding the IICRST Bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.

26. A/D Converter

Note

The description offered in this chapter is based on the R8C/LA8A Group.
For other groups, refer to 1.1.2 Differences between Groups.

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog input shares pins P0_0, P6, and P7_4 to P7_6.
As an extended function, the output voltage from the temperature sensor can be A/D converted.
For details of the temperature sensor, refer to **26.9 Temperature Sensor**.

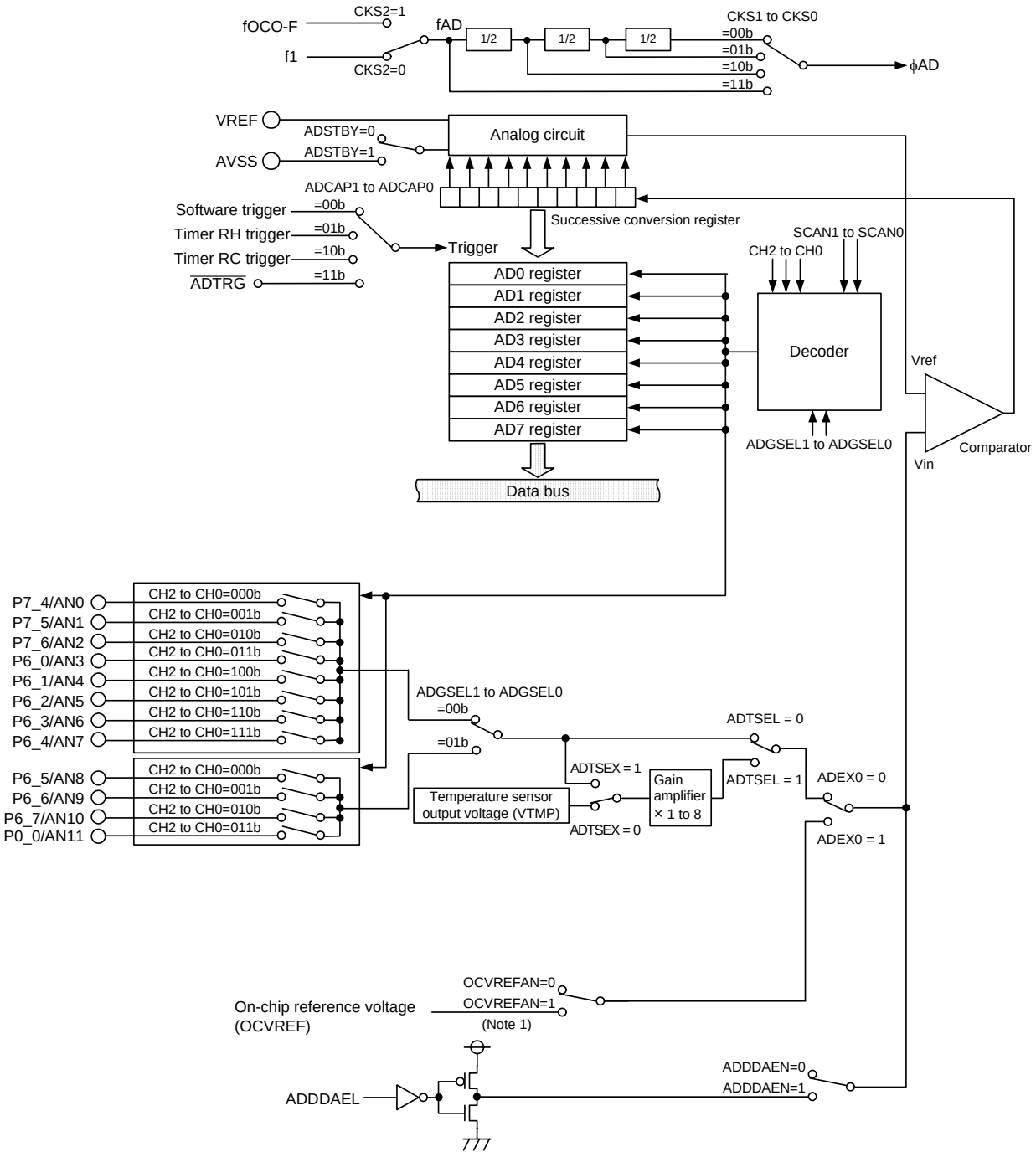
26.1 Introduction

Table 26.1 lists the A/D Converter Performance. Figure 26.1 shows the A/D Converter Block Diagram.

Table 26.1 A/D Converter Performance

Item	Performance
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage (1)	0 V to AVCC
Gain amplifier selection (4)	Gain 1, 2, 4, 6, or 8 can be selected
Operating clock ϕAD (2)	fAD, fAD divided by 2, fAD divided by 4, fAD divided by 8 (fAD = f1 or fOCO-F)
Resolution	8 bits or 10 bits selectable
Absolute accuracy	AVCC = Vref = 5 V, ϕAD = 20 MHz • 8-bit resolution±2 LSB • 10-bit resolution±3 LSB AVCC = Vref = 3.0 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
Operating modes	One-shot mode, repeat mode 0, repeat mode 1, single sweep mode, and repeat sweep mode
Analog input pins	12 pins (AN0 to AN11)
A/D conversion start conditions	• Software trigger • Timer RH • Timer RC • External trigger • (Refer to **26.3.3 A/D Conversion Start Conditions**.)
Conversion rate per pin (3) (ϕAD = fAD)	Minimum 44 ϕAD cycles

Notes:
1. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.
2. Refer to **Table 30.3 A/D Converter Characteristics** for the operating clock ϕAD.
3. The conversion rate per pin is minimum 44 ϕAD cycles for 8-bit and 10-bit resolution.
4. Due to the characteristics of the gain amplifier, the A/D conversion result at around VSS to VSS + 0.2 V and VCC to VCC - 0.4 V will be undefined. The gain amplifier has an offset. This offset increases with the multiplication factor of the gain.



CKS0 to CKS2, ADCAP0, ADCAP1: Bits in ADMOD register
CH0 to CH2, SCAN0, SCAN1, ADGSEL0, ADGSEL1: Bits in ADINSEL register
ADEX0, ADSTBY, ADDDAEN, ADDDAEL: Bits in ADCON1 register
ADTSEX, ADTSEL: Bits in ADCON2 register
OCVREFAN: Bit in OCVREFCR register

Note:
1. When the on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
When the on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (on-chip reference voltage not selected).

Figure 26.1 A/D Converter Block Diagram

26.2 Registers

26.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	MSTURT2	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	UART0 standby bit	0: Active 1: Standby (1)	R/W
b2	MSTURT2	UART2 standby bit	0: Active 1: Standby (2)	R/W
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (3)	R/W
b4	MSTLCD	LCD standby bit	0: Active 1: Standby (4)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (5)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	A/D standby bit (6)	0: Active 1: Standby	R/W

Notes:
1. When the MSTURT0 bit is set to 1 (standby), any access to the UART0 associated registers (addresses 00A0h to 00A7h) is disabled.
2. When the MSTURT2 bit is set to 1 (standby), any access to the timer UART2 associated registers (addresses 00A8h to 00BFh) is disabled.
3. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
4. When the MSTLCD bit is set to 1 (standby), any access to the timer LCD associated registers (addresses 0200h to 0237h) is disabled.
5. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
6. When the MSTADC bit is set to 1 (standby), any access to the timer A/D associated registers (addresses 00C0h to 00D9h, 00DCh to 00DFh) is disabled.
   Set the MSTADC bit to 0 (active) when the temperature sensor is used.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

26.2.2 On-Chip Reference Voltage Control Register (OCVREFCR)

Address 0026h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	OCVREFAN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCVREFAN	On-chip reference voltage to analog input connect bit (1)	0: On-chip reference voltage and analog input are cut off 1: On-chip reference voltage and analog input are connected	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:

1. When the on-chip reference voltage is used as analog input, first set the ADEX0 bit in the ADCON1 register to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
   When the on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input not selected).
   Set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) when the temperature sensor is used.

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the OCVREFCR register.
   If the content of the OCVREFCR register is rewritten during A/D conversion, the conversion result is undefined.

26.2.3 A/D Register i (ADi) (i = 0 to 7)

Address 00C1h to 00C0h (AD0), 00C3h to 00C2h (AD1), 00C5h to 00C4h (AD2), 00C7h to 00C6h (AD3), 00C9h to 00C8h (AD4), 00CBh to 00CAh (AD5), 00CDh to 00CCh (AD6), 00CFh to 00CEh (AD7)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	X	X

Bit	Function		R/W
	10-bit mode (BITS bit in ADCON1 register = 1)	8-bit mode (BITS bit in ADCON1 register = 0)	
b0	8 low-order bits in A/D conversion result	A/D conversion result	R
b1			
b2			
b3			
b4			
b5			
b6			
b7			
b8	2 high-order bits in A/D conversion result	When read, the content is 0.	R
b9			
b10	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b11			
b12			
b13			
b14			
b15	Reserved bit	When read, the content is undefined.	R

If the contents of the ADCON1, ADMOD, ADINSEL, or OCVREFCR register are written during A/D conversion, the conversion result is undefined.

When using the A/D converter in 10-bit mode, repeat mode 0, repeat mode 1, or repeat sweep mode, access the ADi register in 16-bit units. Do not access it in 8-bit units.

Wait for one cycle or more to read the conversion result after A/D conversion is completed.

26.2.4 A/D Mode Register (ADMOD)

Address 00D4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	MD2	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0 0 0: fAD divided by 8 0 1: fAD divided by 4 1 0: fAD divided by 2 1 1: fAD divided by 1 (no division)	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit (1)	0: f1 selected 1: fOCO-F selected	R/W
b3	MD0	A/D operating mode select bit (2)	b5 b4 b3 0 0 0: One-shot mode 0 0 1: Do not set. 0 1 0: Repeat mode 0 0 1 1: Repeat mode 1 1 0 0: Single sweep mode 1 0 1: Do not set. 1 1 0: Repeat sweep mode 1 1 1: Do not set.	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6 0 0: A/D conversion starts by software trigger (ADST bit in ADCON0 register) 0 1: A/D conversion starts by conversion trigger from timer RH 1 0: A/D conversion starts by conversion trigger from timer RC 1 1: A/D conversion starts by external trigger ($\overline{\text{ADTRG}}$)	R/W
b7	ADCAP1			R/W

Notes:
1. When the CKS2 bit is changed, wait for three ϕAD cycles or more before starting A/D conversion.
2. Use the temperature sensor only in one-shot mode, repeat mode 0, or repeat mode 1.
   Do not select single sweep mode and repeat sweep mode.

If the content of the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

26.2.5 A/D Input Select Register (ADINSEL)

Address 00D5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADGSEL1	ADGSEL0	SCAN1	SCAN0	—	CH2	CH1	CH0
After Reset	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Analog input pin select bit	Refer to **Table 26.2 Analog Input Pin Selection**	R/W
b1	CH1			R/W
b2	CH2			R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	SCAN0	A/D sweep pin count select bit	b5 b4 0 0: 2 pins 0 1: 4 pins 1 0: 6 pins 1 1: 8 pins	R/W
b5	SCAN1			R/W
b6	ADGSEL0	A/D input group select bit	b7 b6 0 0: AN0 to AN7 selected 0 1: AN8 to AN11 selected 1 0: Do not set. 1 1: Do not set.	R/W
b7	ADGSEL1			R/W

If the content of the ADINSEL register is rewritten during A/D conversion, the conversion result is undefined.

Table 26.2 Analog Input Pin Selection

Bits CH2 to CH0	Bits ADGSEL1 to ADGSEL0 = 00b	Bits ADGSEL1 to ADGSEL0 = 01b
000b	AN0	AN8
001b	AN1	AN9
010b	AN2	AN10
011b	AN3	AN11
100b	AN4	Do not set.
101b	AN5	
110b	AN6	
111b	AN7	

26.2.6 A/D Control Register 0 (ADCON0)

Address 00D6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	0: A/D conversion stops 1: A/D conversion starts	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

ADST Bit (A/D Conversion Start Flag)

[Conditions for setting to 1] When A/D conversion starts and while A/D conversion is in progress.
[Condition for setting to 0] When A/D conversion stops.

26.2.7 A/D Control Register 1 (ADCON1)

Address 00D7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADDDAEL	ADDDAEN	ADSTBY	BITS	—	—	—	ADEX0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	On-chip reference voltage select bit (1)	0: On-chip reference voltage not selected 1: On-chip reference voltage selected (2, 5, 6)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	BITS	8-/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit (3)	0: A/D operation stops (standby) 1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit (4, 6)	0: Disabled 1: Enabled	R/W
b7	ADDDAEL	A/D open-circuit detection assist method select bit (4)	0: Discharge before conversion 1: Precharge before conversion	R/W

Notes:

1. When the on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit in the OCVREFCR register to 1 (on-chip reference voltage and analog input are connected).
   When the on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (on-chip reference voltage not selected).
   Set the ADEX0 bit to 0 (on-chip reference voltage not selected) when the temperature sensor is used.
2. Do not set in single sweep mode or repeat sweep mode.
3. When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for one ϕAD cycle or more before starting A/D conversion.
4. To enable the A/D open-circuit detection assist function, select the conversion start state with the ADDDAEL bit after setting the ADDDAEN bit to 1 (enabled).
   The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed according to the system before using this function.
5. When on-chip reference voltage is used (ADEX0 = 1), set bits CH2 to CH0 in the ADINSEL register to 000b.
6. When on-chip reference voltage is used (ADEX0 = 1), set the ADDDAEN bit to 0 (A/D open-circuit detection assist function disabled).

If the content of the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

26.2.8 A/D Control Register 2 (ADCON2)

Address 00DDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTSEL	ADTSEN	—	—	ADTSEX	ADTSG2	ADTSG1	ADTSG0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTSG0	Gain select bit (5)	b2 b1 b0 0 0 0: Gain 1 0 0 1: Gain 2 0 1 0: Gain 4 0 1 1: Gain 6 1 0 0: Gain 8 1 0 1: Do not select. 1 1 0: Do not select. 1 1 1: Do not select.	R/W
b1	ADTSG1			R/W
b2	ADTSG2			R/W
b3	ADTSEX	Gain amplifier input switch bit	0: Internal temperature sensor (3) 1: Analog input pin	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	ADTSEN	Gain amplifier operation start bit (1, 2, 3)	0: Operation stops 1: Operation starts	R/W
b7	ADTSEL	Analog input switch bit (4)	0: Analog input pin 1: Gain amplifier output	R/W

Notes:
1. When the gain amplifier is not used, set the ADTSEN bit to 0 to reduce current consumption.
2. When the ADTSEN bit is set to 1 (operation starts), the gain amplifier starts operation. The voltage will stabilize maximum 200 μs after the setting to start operation. Wait until the voltage stabilizes before starting A/D conversion.
3. When the ADTSEX bit is set to 0 (internal temperature sensor) and the ADTSEN bit is set to 1 (operation starts), the temperature sensor starts operation. After the setting to start operation, wait until the voltage stabilizes a maximum of 200 μs before starting A/D conversion.
4. Set the ADTSEL bit to 1 (gain amplifier output) when the temperature sensor is used.
5. Ensure the amplified value does not exceed VCC.

If the content of the ADCON2 register is rewritten during A/D conversion, the conversion result is undefined. Due to the characteristics of the gain amplifier, the A/D conversion result at around VSS to VSS + 0.2 V and VCC to VCC – 0.4 V will be undefined. The gain amplifier has an offset. This offset increases with the multiplication factor of the gain.

26.3 Common Items for Multiple Modes

26.3.1 Input/Output Pins

The analog input shares pins P0_0, P6, and P7_4 to P7_6 in AN0 to AN11.
To use the ANi (i = 0 to 11) pin as input, set the corresponding port direction bit to 0 (input mode).
After changing the A/D operating mode, select an analog input pin again.

26.3.2 A/D Conversion Cycles

Figure 26.2 shows the Timing Diagram of A/D Conversion. Figure 26.3 shows the A/D Conversion Cycles (ϕAD = fAD).

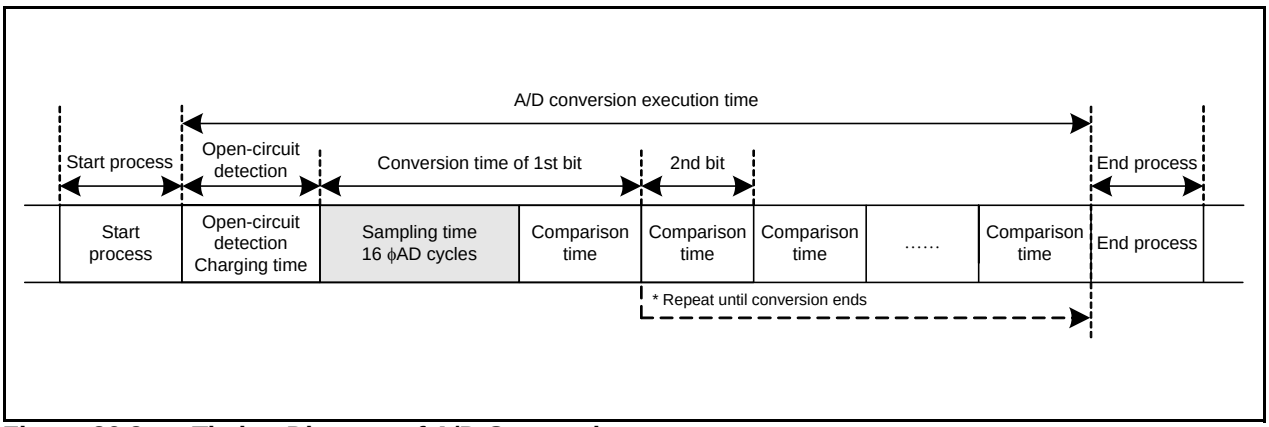
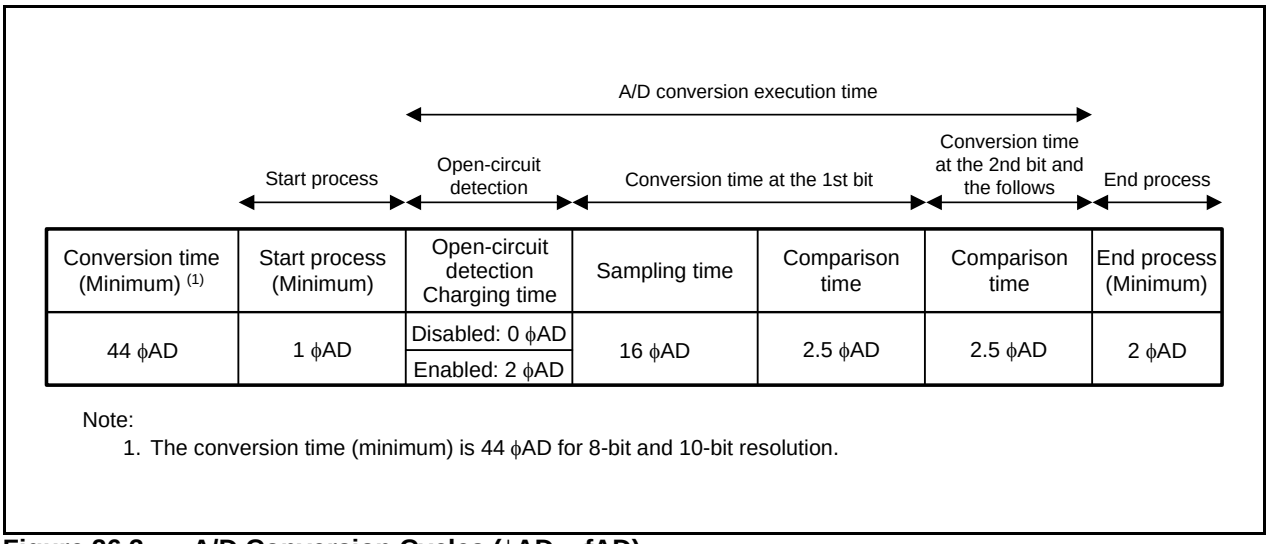


Figure 26.2 Timing Diagram of A/D Conversion


A/D conversion execution time
Start process
Open-circuit detection
Conversion time at the 1st bit
Conversion time at the 2nd bit and the follows
End process

Conversion time (Minimum) (1)	Start process (Minimum)	Open-circuit detection Charging time	Sampling time	Comparison time	Comparison time	End process (Minimum)
44 ϕAD	1 ϕAD	Disabled: 0 ϕAD Enabled: 2 ϕAD	16 ϕAD	2.5 ϕAD	2.5 ϕAD	2 ϕAD

Note:
1. The conversion time (minimum) is 44 ϕAD for 8-bit and 10-bit resolution.

Figure 26.3 A/D Conversion Cycles (ϕAD = fAD)

Table 26.3 shows the Number of Cycles for A/D Conversion Items. The A/D conversion time is defined as follows:
The start process time varies depending on which ϕAD is selected.
When 1 (A/D conversion starts) is written to the ADST bit in the ADCON0 register, an A/D conversion starts after the start process time has elapsed. Reading the ADST bit before the A/D conversion returns 0 (A/D conversion stops).
In the modes where an A/D conversion is performed on multiple pins or multiple times, the between-execution process time is inserted between the A/D conversion execution time for one pin and the next A/D conversion time.
In one-shot mode and single sweep mode, the ADST bit is set to 0 during the end process time and the last A/D conversion result is stored in the ADi register.

- In on-shot mode
  Start process time + A/D conversion execution time + end process time

- When two pins are selected in single sweep mode
  Start process time + (A/D conversion execution time + between-execution process time + A/D conversion execution time) + end process time

Table 26.3 Number of Cycles for A/D Conversion Items

A/D Conversion Item		Number of Cycles
Start process time	ϕAD = fAD	1 or 2 fAD cycles
	ϕAD = fAD divided by 2	2 or 3 fAD cycles
	ϕAD = fAD divided by 4	3 or 4 fAD cycles
	ϕAD = fAD divided by 8	5 or 6 fAD cycles
A/D conversion execution time	Open-circuit detection disabled	40 ϕAD cycles + 1 to 3 fAD cycles
	Open-circuit detection enabled	42 ϕAD cycles + 1 to 3 fAD cycles
Between-execution process time		1 ϕAD cycle
End process time		2 or 3 fAD cycles

26.3.3 A/D Conversion Start Conditions

A software trigger, trigger from timer RH interrupt request, trigger from timer RC, and external trigger are used as A/D conversion start triggers.
Figure 26.4 shows the Block Diagram of A/D Conversion Start Control Unit.

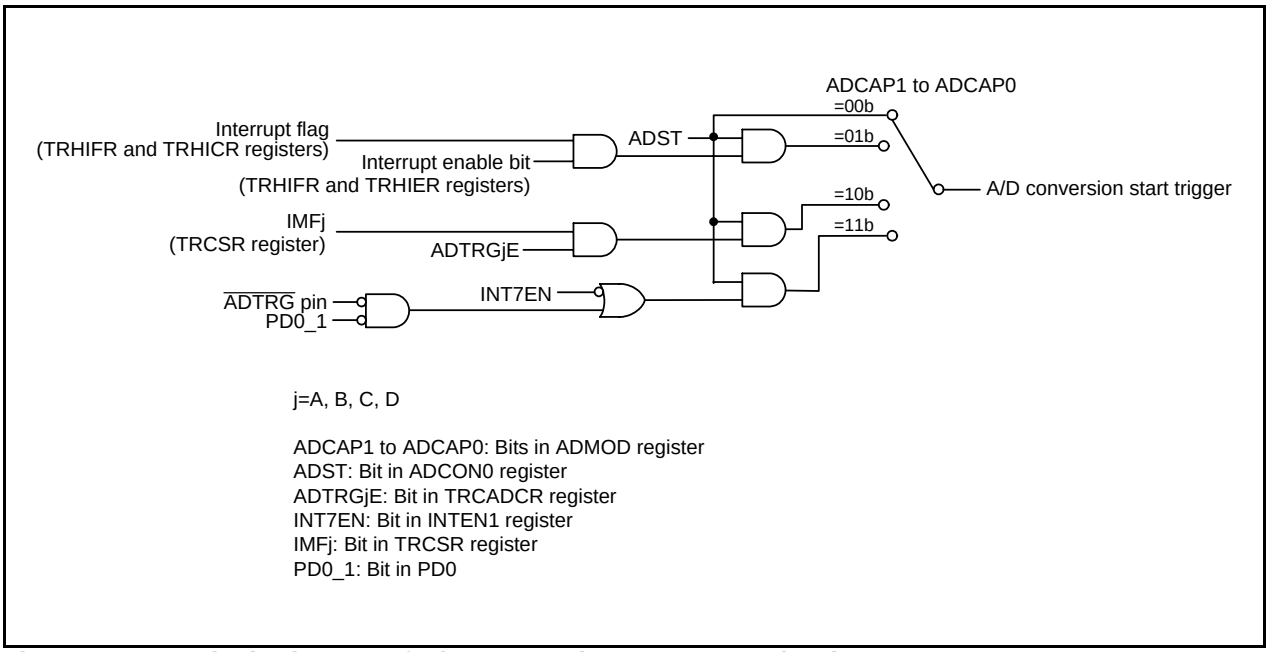


Figure 26.4 Block Diagram of A/D Conversion Start Control Unit

26.3.3.1 Software Trigger

A software trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger).
The A/D conversion starts when the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

26.3.3.2 Trigger from Timer RH

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 01b (timer RH).
To use this function, make sure the following conditions are met:

- Bits ILVL0 to ILVL2 in the TRHIC register are set to 000b (interrupt disabled).
- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 01b (timer RH).
- Timer RH is used.
- The corresponding interrupt enable bit in the TRHIER register is set to 1.
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the corresponding interrupt flag in the TRHIFR or TRHICR register is changed from 0 to 1 under the above conditions, A/D conversion starts.
Refer to **12. Interrupts** and **19. Timer RH** for details of timer RH interrupt request.

26.3.3.3 Trigger from Timer RC

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
To use this function, make sure the following conditions are met:

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
- Timer RC is used in the output compare function (timer mode, PWM mode, and PWM2 mode).
- The ADTRGjE bit (j = A, B, C, D) in the TRCADCR register is set to 1 (A/D trigger occurs at compare match with TRCGRj register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMFj bit in the TRCSR register is changed from 0 to 1 under the above conditions, A/D conversion starts.
Refer to **18. Timer RC**, **18.5 Timer Mode (Output Compare Function)**, **18.6 PWM Mode**, **18.7 PWM2 Mode** for the details of timer RC and the output compare function (timer mode, PWM mode, and PWM2 mode).

26.3.3.4 External Trigger

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ($\overline{\text{ADTRG}}$)).
To use this function, make sure the following conditions are met:

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ($\overline{\text{ADTRG}}$)).
- The INT7EN bit in the INTEN1 register is set to 1 (($\overline{\text{INT7}}$ input enabled)).
- The port direction register is set to input:
  When the INT7SEL0 bit in the INTSR register is 0, the PD0_1 bit in the PD0 register is set to 0 (input mode).
  When the INT7SEL0 bit in the INTSR register is 1, the PD3_7 bit in the PD3 register is set to 0 (input mode).
- Select the $\overline{\text{INT7}}$ digital filter by bits INT7F1 to INT7F0 in the INTF1 register.
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

The IR bit in the INT7IC register is set to 1 (interrupt requested) in accordance with the setting of the POL bit in the INT7IC register and the INT7PL bit in the INTEN1 register and a change in the $\overline{\text{ADTRG}}$ pin input (refer to **12.8 Notes on Interrupts**).
Refer to **12. Interrupts** for details of interrupts.

When the $\overline{\text{ADTRG}}$ pin input is changed from high to low under the above conditions, A/D conversion starts.

26.3.4 A/D Conversion Result

The A/D conversion result is stored in the ADi register (i = 0 to 7). Wait for one cycle or more to read the conversion result after A/D conversion is completed. The register where the result is stored varies depending on the A/D operating mode used. The contents of the ADi register are undefined after reset. Values cannot be written to the ADi register.

In repeat mode 0, no interrupt request is generated. After the first AD conversion is completed, determine if the A/D conversion time has elapsed by a program.
In one-shot mode, repeat mode 1, single sweep mode, and repeat sweep mode, an interrupt request is generated at certain times, such as when an A/D conversion completes (the IR bit in the ADIC register is set to 1).
However, in repeat mode 1 and repeat sweep mode, A/D conversion continues after an interrupt request is generated. Read the ADi register before the next A/D conversion is completed, since at completion the ADi register is rewritten with the new value.

In one-shot mode and single sweep mode, when bits ADCAP1 to ADCAP0 in the ADMOD register is set to 00b (software trigger), the ADST bit in the ADCON0 register is used to determine whether the A/D conversion or sweep has completed.

During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

26.3.5 Low-Current-Consumption Function

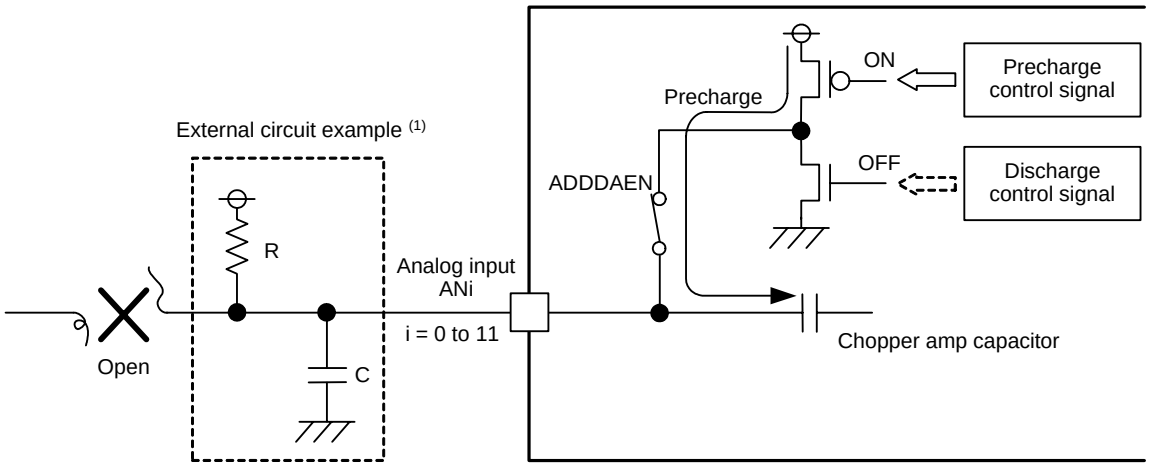
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for one ϕAD cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion starts). Do not write 1 to bits ADST and ADSTBY at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stops (standby)) during the A/D conversion.

26.3.6 On-Chip Reference Voltage (OCVREF)

In one-shot mode, repeat mode 0, and repeat mode 1, the on-chip reference voltage (OCVREF) can be used as analog input.
Any variation in VREF can be confirmed using the on-chip reference voltage. Use the ADEX0 bit in the ADCON1 register and the OCVREFAN bit in the OCVREFCR register to select the on-chip reference voltage.
The A/D conversion result of the on-chip reference voltage in one-shot mode or in repeat mode 0 is stored in the AD0 register.

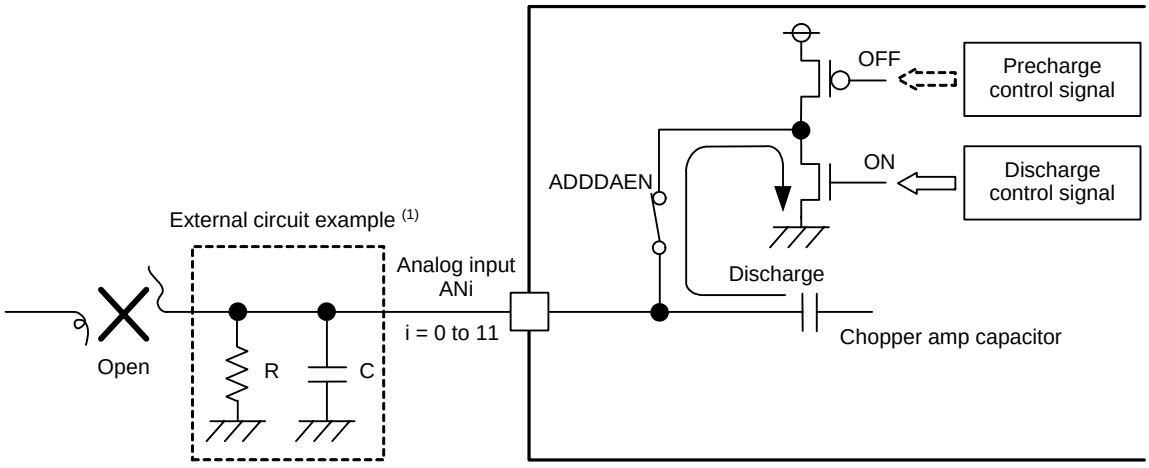
26.3.7 A/D Open-Circuit Detection Assist Function

To suppress influences of the analog input voltage leakage from the previously converted channel during A/D conversion operation, a function is incorporated to fix the electric charge on the chopper amp capacitor to the predetermined state (AVCC or GND) before starting conversion.
This function enables more reliable detection of an open circuit in the wiring connected to the analog input pins.
Figure 26.5 shows the A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected) and Figure 26.6 shows the A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected).



Note:
1. The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed before using this function.

Figure 26.5 A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected)



Note:
1. The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed before using this function.

Figure 26.6 A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected)

26.4 One-Shot Mode

In one-shot mode, the input voltage to one pin selected from among AN0 to AN11, OCVREF, or the temperature sensor output voltage (VTMP) is A/D converted once.
Table 26.4 lists the One-Shot Mode Specifications.

Table 26.4 One-Shot Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register, bits ADTSEX and ADTSEL in the ADCON2 register, or the ADEX0 bit in the ADCON1 register is A/D converted once.
Resolution	8 bits or 10 bits
A/D conversion start conditions	• Software trigger • Timer RH • Timer RC • External trigger (Refer to **26.3.3 A/D Conversion Start Conditions)**
A/D conversion stop conditions	• A/D conversion completes (when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger), the ADST bit in the ADCON0 register is set to 0.) • Set the ADST bit to 0.
Interrupt request generation timing	When A/D conversion completes.
Analog input pin	One pin is selectable from among AN0 to AN11, OCVREF, or VTMP.
Storage resisters for A/D conversion result	AD0 register: AN0, AN8, OCVREF, VTMP (1) AD1 register: AN1, AN9, VTMP (1) AD2 register: AN2, AN10, VTMP (1) AD3 register: AN3, AN11, VTMP (1) AD4 register: AN4, VTMP (1) AD5 register: AN5, VTMP (1) AD6 register: AN6, VTMP (1) AD7 register: AN7, VTMP (1)
Reading of A/D conversion result	Read the register among AD0 to AD7 corresponding to the selected pin.

Note:
1. The A/D conversion result of the temperature sensor output voltage is stored in registers AD0 to AD7 corresponding to the pin selected by bits CH0 to CH2 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register.

26.5 Repeat Mode 0

In repeat mode 0, the input voltage to one pin selected from among AN0 to AN11, OCVREF, or the temperature sensor output voltage (VTMP) is A/D converted repeatedly.
Table 26.5 lists the Repeat Mode 0 Specifications.

Table 26.5 Repeat Mode 0 Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register, bits ADTSEX and ADTSEL in the ADCON2 register, or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start conditions	• Software trigger • Timer RH • Timer RC • External trigger (Refer to **26.3.3 A/D Conversion Start Conditions)**
A/D conversion stop conditions	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	Not generated
Analog input pin	One pin is selectable from among AN0 to AN11, OCVREF, or VTMP.
Storage resisters for A/D conversion result	AD0 register: AN0, AN8, OCVREF, VTMP (1) AD1 register: AN1, AN9, VTMP (1) AD2 register: AN2, AN10, VTMP (1) AD3 register: AN3, AN11, VTMP (1) AD4 register: AN4, VTMP (1) AD5 register: AN5, VTMP (1) AD6 register: AN6, VTMP (1) AD7 register: AN7, VTMP (1)
Reading of A/D conversion result	Read the register among AD0 to AD7 corresponding to the selected pin.

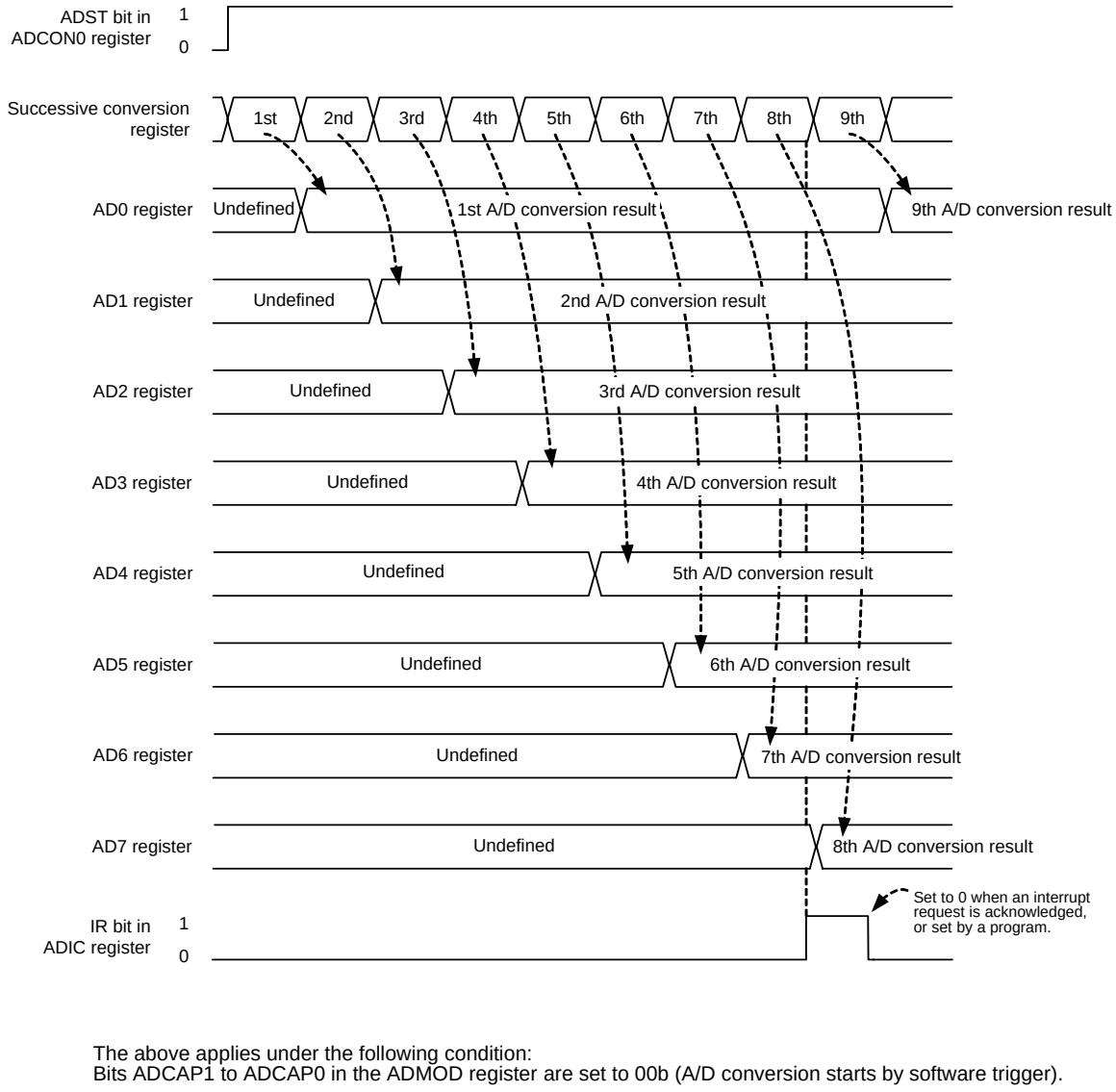
Note:
1. The A/D conversion result of the temperature sensor output voltage is stored in registers AD0 to AD7 corresponding to the pin selected by bits CH0 to CH2 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register.

26.6 Repeat Mode 1

In repeat mode 1, the input voltage to one pin selected from among AN0 to AN11, OCVREF, or the temperature sensor output voltage (VTMP) is A/D converted repeatedly.
Table 26.6 lists the Repeat Mode 1 Specifications. Figure 26.7 shows an Operating Example in Repeat Mode 1.

Table 26.6 Repeat Mode 1 Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register, bits ADTSEX and ADTSEL in the ADCON2 register, or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start conditions	• Software trigger • Timer RH • Timer RC • External trigger (Refer to **26.3.3 A/D Conversion Start Conditions)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0.
Interrupt request generation timing	When the A/D conversion result is stored in the AD7 register.
Analog input pin	One pin is selectable from among AN0 to AN11, OCVREF, or VTMP.
Storage resisters for A/D conversion result	AD0 register: 1st A/D conversion result, 9th A/D conversion result... AD1 register: 2nd A/D conversion result, 10th A/D conversion result... AD2 register: 3rd A/D conversion result, 11th A/D conversion result... AD3 register: 4th A/D conversion result, 12th A/D conversion result... AD4 register: 5th A/D conversion result, 13th A/D conversion result... AD5 register: 6th A/D conversion result, 14th A/D conversion result... AD6 register: 7th A/D conversion result, 15th A/D conversion result... AD7 register: 8th A/D conversion result, 16th A/D conversion result...
Reading of A/D conversion result	Read registers AD0 to AD7.



The above applies under the following condition:
Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (A/D conversion starts by software trigger).

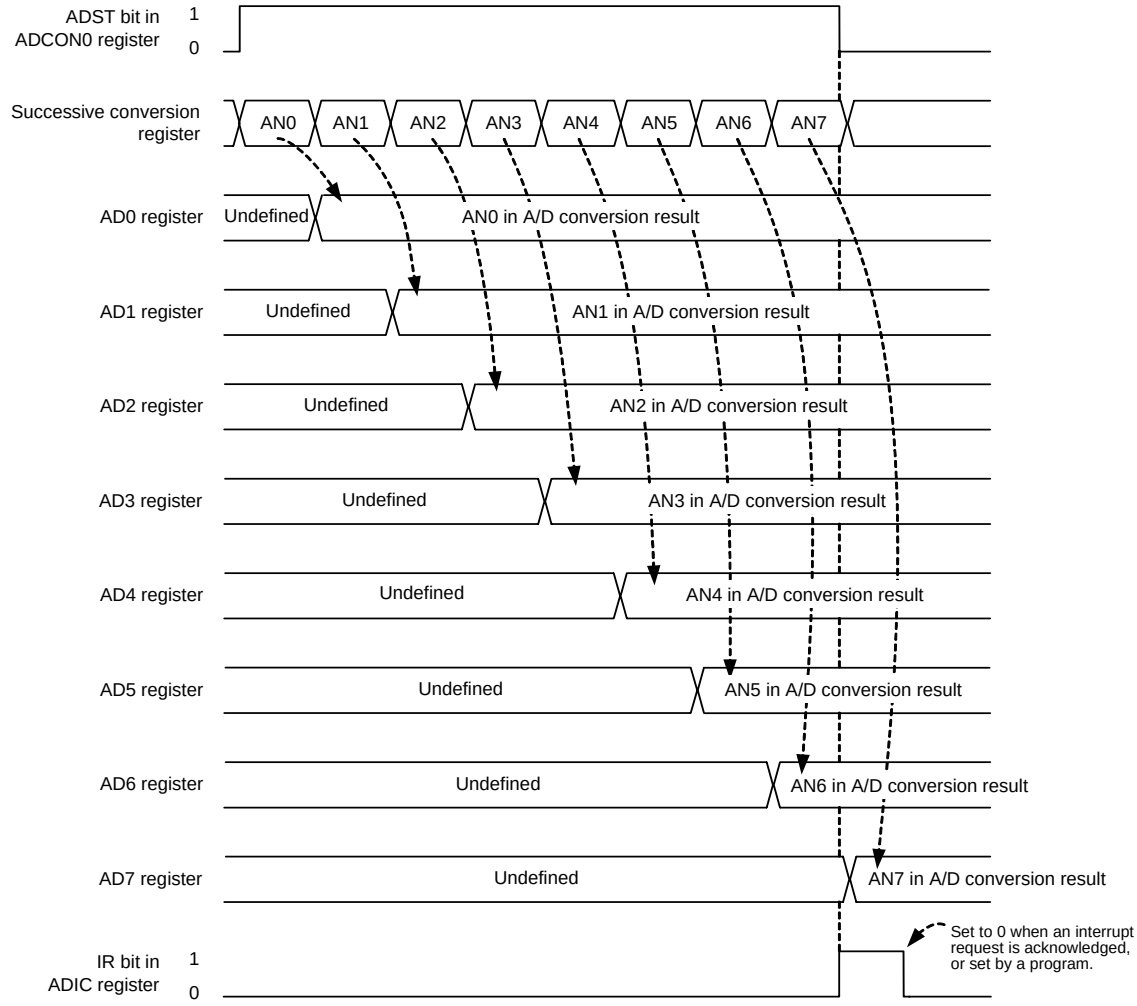
Figure 26.7 Operating Example in Repeat Mode 1

26.7 Single Sweep Mode

In single sweep mode, the input voltage to two, four, six, or eight pins selected from among AN0 to AN11 are A/D converted one-by-one.
Table 26.7 lists the Single Sweep Mode Specifications. Figure 26.8 shows an Operating Example in Single Sweep Mode.

Table 26.7 Single Sweep Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits ADGSEL1 to ADGSEL0 and bits SCAN1 to SCAN0 in the ADINSEL register is A/D converted one-by-one.
Resolution	8 bits or 10 bits
A/D conversion start conditions	• Software trigger • Timer RH • Timer RC • External trigger (Refer to **26.3.3 A/D Conversion Start Conditions)**
A/D conversion stop conditions	• If 2 pins are selected, when A/D conversion of the 2 selected pins completes. (The ADST bit in the ADCON0 register is set to 0.) • If 4 pins are selected, when A/D conversion of the 4 selected pins completes. (The ADST bit is set to 0.) • If 6 pins are selected, when A/D conversion of the 6 selected pins completes. (The ADST bit is set to 0.) • If 8 pins are selected, when A/D conversion of the 8 selected pins completes. (The ADST bit is set to 0.) • Set the ADST bit to 0.
Interrupt request generation timing	• If 2 pins are selected, when A/D conversion of the 2 selected pins completes. • If 4 pins are selected, when A/D conversion of the 4 selected pins completes. • If 6 pins are selected, when A/D conversion of the 6 selected pins completes. • If 8 pins are selected, when A/D conversion of the 8 selected pins completes.
Analog input pins	AN0 and AN1 (2 pins), AN8 and AN9 (2 pins) AN0 to AN3 (4 pins), AN8 to AN11 (4 pins) AN0 to AN5 (6 pins) AN0 to AN7 (8 pins) (Selectable by bits SCAN1 to SCAN0 and bits ADGSEL1 to ADGSEL0.)
Storage resisters for A/D conversion result	AD0 register: AN0, AN8 AD1 register: AN1, AN9 AD2 register: AN2, AN10 AD3 register: AN3, AN11 AD4 register: AN4 AD5 register: AN5 AD6 register: AN6 AD7 register: AN7
Reading of A/D conversion result	Read the register among AD0 to AD7 corresponding to the selected pin.



The above applies under the following conditions:
- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (A/D conversion starts by software trigger).
- Bits SCAN1 to SCAN0 in the ADINSEL register are set to 11b (8 pins), bits ADGSEL1 to ADGSEL0 are set to 00b (AN0, AN1, AN2, AN3, AN4, AN5, AN6, and AN7).

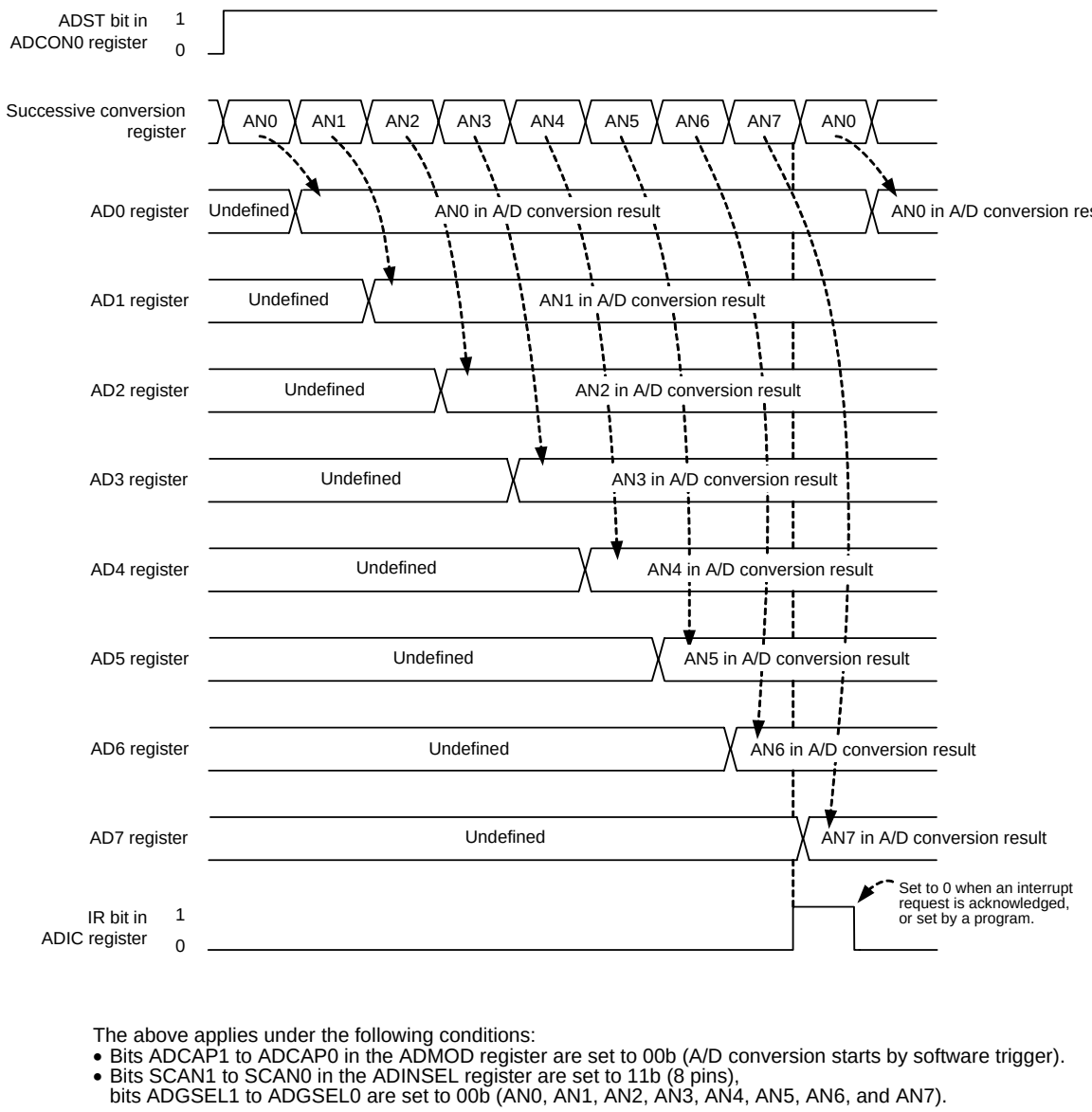
Figure 26.8 Operating Example in Single Sweep Mode

26.8 Repeat Sweep Mode

In repeat sweep mode, the input voltage to two, four, six, or eight pins selected from among AN0 to AN11 are A/D converted repeatedly.
Table 26.8 lists the Repeat Sweep Mode Specifications. Figure 26.9 shows an Operating Example in Repeat Sweep Mode.

Table 26.8 Repeat Sweep Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits ADGSEL1 to ADGSEL0 and bits SCAN1 to SCAN0 in the ADINSEL register is A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start conditions	• Software trigger • Timer RH • Timer RC • External trigger (Refer to **26.3.3 A/D Conversion Start Conditions)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	• If 2 pins are selected, when A/D conversion of the 2 selected pins completes. • If 4 pins are selected, when A/D conversion of the 4 selected pins completes. • If 6 pins are selected, when A/D conversion of the 6 selected pins completes. • If 8 pins are selected, when A/D conversion of the 8 selected pins completes.
Analog input pins	AN0 and AN1 (2 pins), AN8 and AN9 (2 pins) AN0 to AN3 (4 pins), AN8 to AN11 (4 pins) AN0 to AN5 (6 pins) AN0 to AN7 (8 pins) (Selectable by bits SCAN1 to SCAN0 and bits ADGSEL1 to ADGSEL0.)
Storage resisters for A/D conversion result	AD0 register: AN0, AN8 AD1 register: AN1, AN9 AD2 register: AN2, AN10 AD3 register: AN3, AN11 AD4 register: AN4 AD5 register: AN5 AD6 register: AN6 AD7 register: AN7
Reading of A/D conversion result	Read the register among AD0 to AD7 corresponding to the selected pin.



The above applies under the following conditions:
- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (A/D conversion starts by software trigger).
- Bits SCAN1 to SCAN0 in the ADINSEL register are set to 11b (8 pins), bits ADGSEL1 to ADGSEL0 are set to 00b (AN0, AN1, AN2, AN3, AN4, AN5, AN6, and AN7).

Figure 26.9 Operating Example in Repeat Sweep Mode

26.9 Temperature Sensor

A temperature sensor circuit is provided to generate a voltage (typical temperature-coefficient value: –2.1 mV/°C) which decreases in proportion to temperature. The temperature sensor output voltage can be A/D converted through the gain amplifier.
Table 26.9 lists the Temperature Sensor Performance, and Figure 26.10 shows the Temperature Characteristics of Temperature Sensor Output Voltage (Typical Characteristics).

Table 26.9 Temperature Sensor Performance

Item	Performance
Guaranteed temperature range	–20 to 85 °C
Temperature coefficient of temperature sensor output voltage	Typical value: –2.1 mV/°C
Normal temperature characteristics of temperature sensor output voltage	Typical value: 600 mV (Topr = 27 °C)
Gain amplifier selection	Gain 1, 2, 4, 6, or 8 can be selected (1)
A/D conversion voltage/frequency conditions	1.8 V ≤ Vref = AVCC ≤ 5.5 V ϕAD: 1 MHz to 5 MHz
Start-up time	Max. 200 μs
Resolution	8 bits or 10 bits selectable
Absolute accuracy	Refer to **Table 30.3 A/D Converter Characteristics**.
Operating modes	One-shot mode, repeat mode 0, and repeat mode 1
A/D conversion start conditions	Refer to **Table 26.1 A/D Converter Performance**.
A/D conversion result	Refer to **26.3.4 A/D Conversion Result**.

Note:
1. Ensure the amplified value does not exceed VCC.

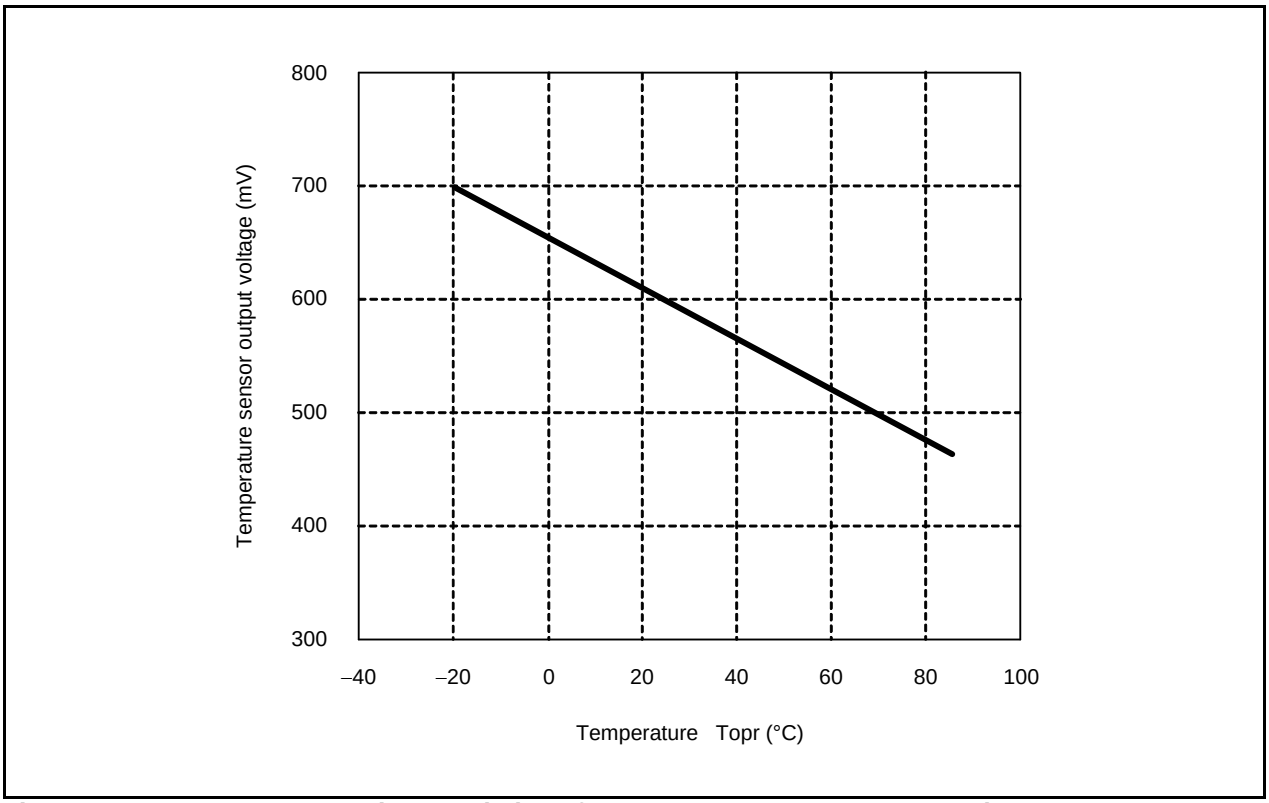
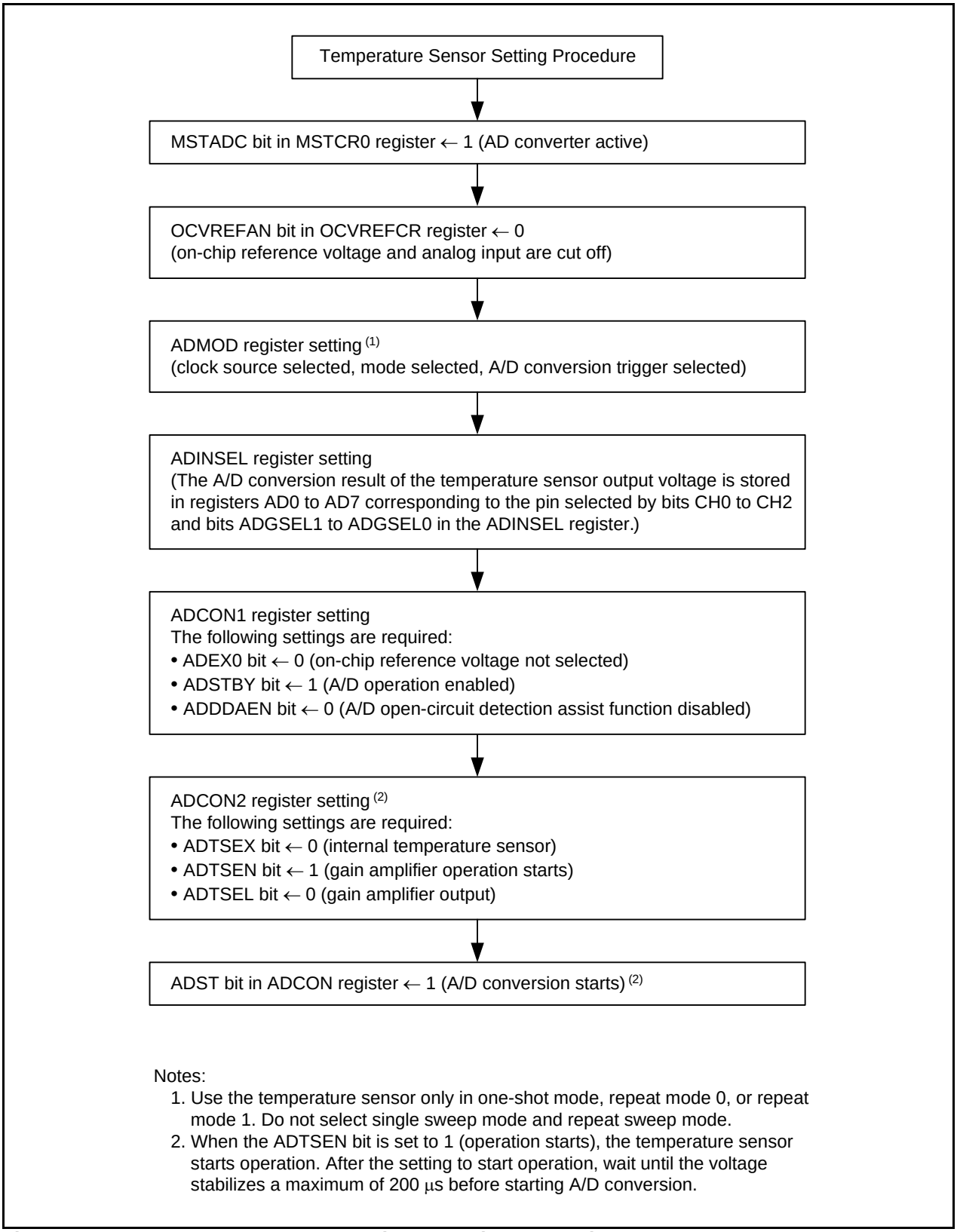


Figure 26.10 Temperature Characteristics of Temperature Sensor Output Voltage (Typical Characteristics)

26.9.1 Temperature Sensor Setting Procedure

Figure 26.11 shows the Temperature Sensor Setting Procedure Example before A/D conversion starts.


Temperature Sensor Setting Procedure
MSTADC bit in MSTCR0 register ← 1 (AD converter active)
OCVREFAN bit in OCVREFCR register ← 0
(on-chip reference voltage and analog input are cut off)
ADMOD register setting (1)
(clock source selected, mode selected, A/D conversion trigger selected)
ADINSEL register setting
(The A/D conversion result of the temperature sensor output voltage is stored in registers AD0 to AD7 corresponding to the pin selected by bits CH0 to CH2 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register.)
ADCON1 register setting
The following settings are required:
• ADEX0 bit ← 0 (on-chip reference voltage not selected)
• ADSTBY bit ← 1 (A/D operation enabled)
• ADDDAEN bit ← 0 (A/D open-circuit detection assist function disabled)
ADCON2 register setting (2)
The following settings are required:
• ADTSEX bit ← 0 (internal temperature sensor)
• ADTSEN bit ← 1 (gain amplifier operation starts)
• ADTSEL bit ← 0 (gain amplifier output)
ADST bit in ADCON register ← 1 (A/D conversion starts) (2)

Notes:
1. Use the temperature sensor only in one-shot mode, repeat mode 0, or repeat mode 1. Do not select single sweep mode and repeat sweep mode.
2. When the ADTSEN bit is set to 1 (operation starts), the temperature sensor starts operation. After the setting to start operation, wait until the voltage stabilizes a maximum of 200 μs before starting A/D conversion.

Figure 26.11 Temperature Sensor Setting Procedure Example

26.10 Output Impedance of Sensor under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 26.12 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, internal resistance of microcomputer be R, precision (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

VC is generally $VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$

And when t = T, $VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

Hence, $R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$

Figure 26.12 shows the Analog Input Pin and External Sensor Equivalent Circuit. When the difference between VIN and VC becomes 0.1LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN-(0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB.
T = 0.75 µs when ϕAD = 20 MHz. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.75 µs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.75 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \approx 3.5 \times 10^{3}$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1LSB or less, is approximately 3.5 kΩ maximum.

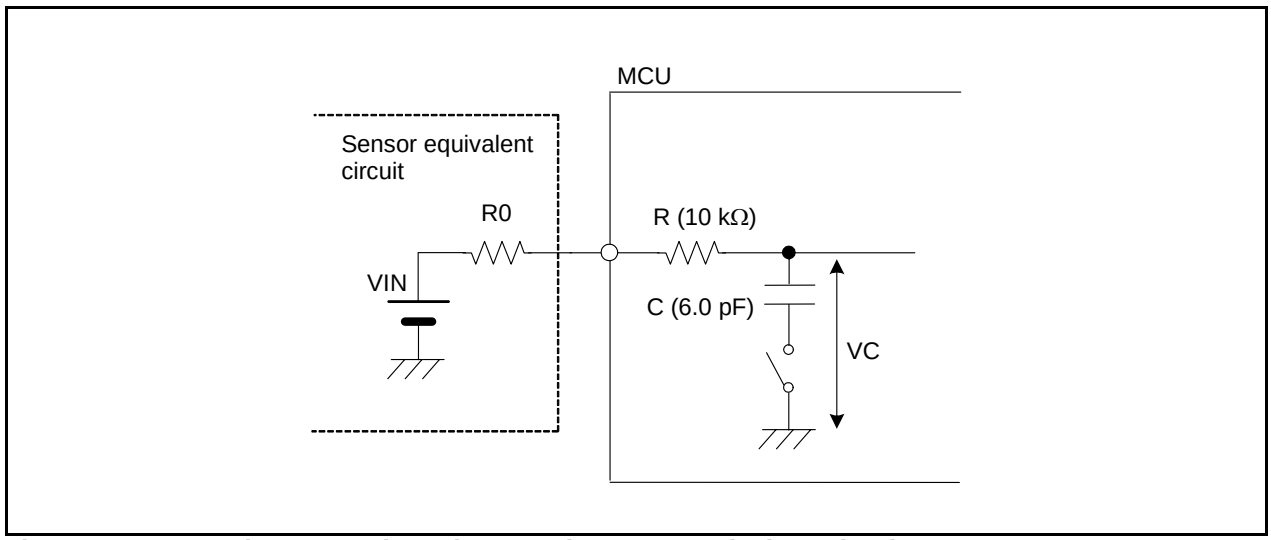


Figure 26.12 Analog Input Pin and External Sensor Equivalent Circuit

26.11 Notes on A/D Converter

26.11.1 A/D Converter

- Write to the ADMOD, ADINSEL, ADCON0 (other than the ADST bit), ADCON1, or OCVREFCR register must be performed while A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select fOCO-F as ϕAD.
- Connect 0.1 μF capacitor between pins VREF and AVSS.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) or the FMR27 bit to 1 (low-current-consumption read mode enabled) during A/D conversion. Otherwise, the A/D conversion result will be undefined.
- Do not change the CKS2 bit in the ADMOD register while fOCO-F is stopped.
- During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

26.11.2 Temperature Sensor

- When the ADTSEN bit is set to 1 (operation starts), the temperature sensor starts operation. After the setting to start operation, wait until the voltage stabilizes a maximum of 200 μs before starting A/D conversion.
- The A/D conversion result of the temperature sensor output voltage will include fluctuations in the output voltage and errors in the A/D converter absolute accuracy. This may cause discrepancies in the Temperature Sensor Performance (refer to Table 26.9) or the Temperature Characteristics (Typical Characteristics) of Temperature Sensor Output Voltage (refer to Figure 26.10).
- Depending on the environment surrounding the MCU, the thermal conductivity from the measured object to the temperature sensor circuit varies, affecting the response time and accuracy of the temperature sensor output voltage. Careful evaluation should be performed for the system before use.
- If the temperature sensor output voltage amplified by the gain amplifier exceeds the reference voltage, A/D conversion cannot be performed correctly.
- The temperature sensor output voltage cannot be output from the pins.

27. Comparator B

Comparator B compares a reference input voltage and an analog input voltage. Comparator B1 and comparator B3 are independent of each other.

27.1 Introduction

The comparison result of the reference input voltage and analog input voltage can be read by software. An input to the IVREFi (i = 1 or 3) pin can be used as the reference input voltage.
Table 27.1 lists the Comparator B Specifications, Figure 27.1 shows the Comparator B Block Diagram, and Table 27.2 lists the I/O Pins.

Table 27.1 Comparator B Specifications

Item	Specification
Analog input voltage	Input voltage to the IVCMPi pin
Reference input voltage	Input voltage to the IVREFi pin
Comparison result	Read from the INTiCOUT bit in the INTCMP register
Interrupt request generation timing	When the comparison result changes.
Selectable function	• Digital filter function Whether the digital filter is applied or not and the sampling frequency can be selected.

i = 1 or 3

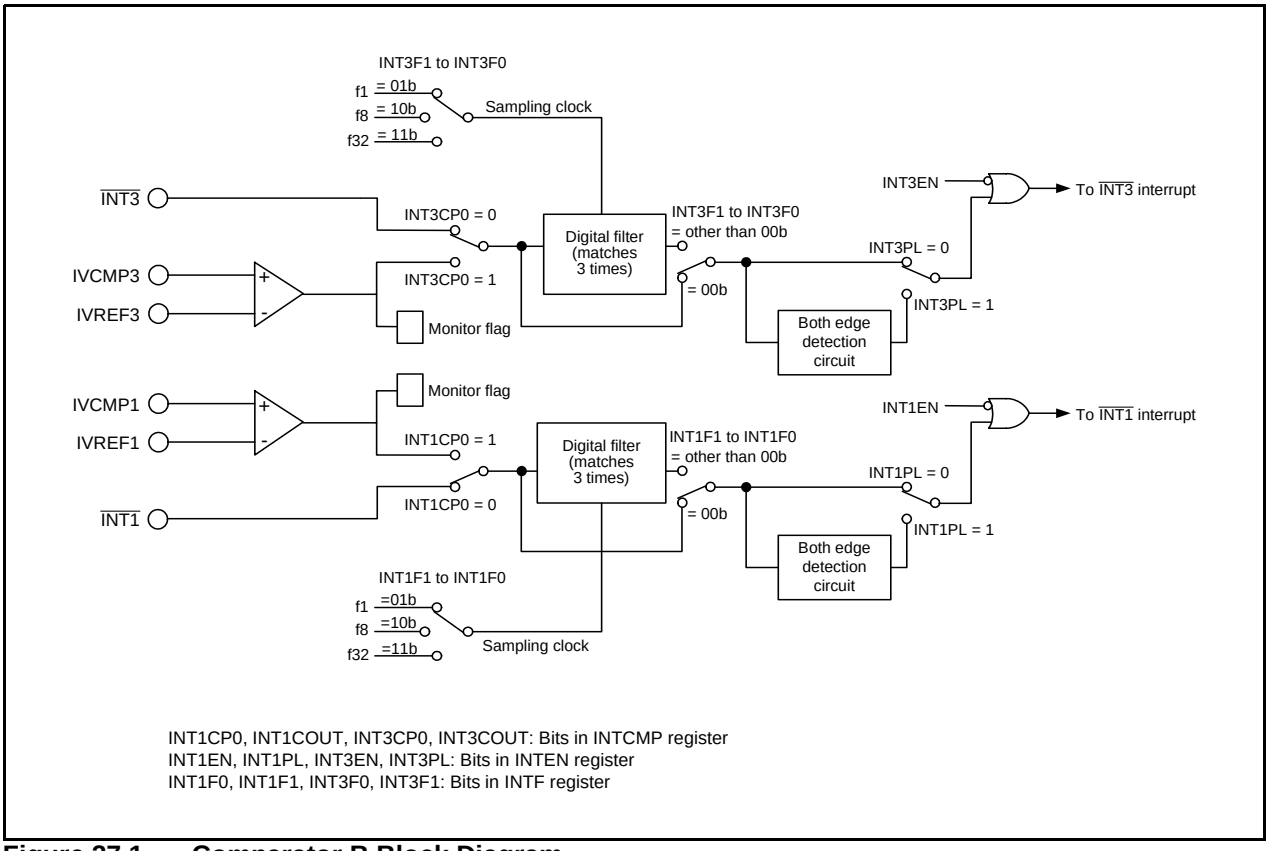


Figure 27.1 Comparator B Block Diagram

Table 27.2 I/O Pins

Pin Name	I/O	Function
IVCMP1	Input	Comparator B1 analog pin
IVREF1	Input	Comparator B1 reference voltage pin
IVCMP3	Input	Comparator B3 analog pin
IVREF3	Input	Comparator B3 reference voltage pin

27.2 Registers

27.2.1 Comparator B Control Register 0 (INTCMP)

Address 01F8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3COUT	—	—	INT3CP0	INT1COUT	—	—	INT1CP0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT1CP0	Comparator B1 operation enable bit	0: Comparator B1 operation disabled 1: Comparator B1 operation enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	INT1COUT	Comparator B1 monitor flag	0: IVCMP1 < IVREF1 or comparator B1 operation disabled 1: IVCMP1 > IVREF1	R
b4	INT3CP0	Comparator B3 operation enable bit	0: Comparator B3 operation disabled 1: Comparator B3 operation enabled	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	INT3COUT	Comparator B3 monitor flag	0: IVCMP3 < IVREF3 or comparator B3 operation disabled 1: IVCMP3 > IVREF3	R

27.2.2 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

27.2.3 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

27.3 Functional Description

Comparator B1 and comparator B3 operate independently. Their operations are the same.
Table 27.3 lists the Procedure for Setting Registers Associated with Comparator B.

Table 27.3 Procedure for Setting Registers Associated with Comparator B

Step	Register	Bit	Setting Value
1	Select the function of pins IVCMPi and IVREFi. Refer to **7.6 Port Settings**. However, set registers and bits other than listed in step 2 and the following steps.		
2	INTF	Select whether to enable or disable the filter. Select the sampling clock.	
3	INTCMP	INTiCP0	1 (operation enabled)
4	Wait for comparator stability time (100 μs max.)		
5	INTEN	INTiEN	When using an interrupt: 1 (interrupt enabled)
		INTiPL	When using an interrupt: Select the input polarity.
6	INTiIC	ILVL0 to ILVL2	When using an interrupt: Select the interrupt priority level.
		IR	When using an interrupt: 0 (no interrupt requested: initialization)

i = 1 or 3

Figure 27.2 shows an Operating Example of Comparator Bi (i = 1 or 3).
If the analog input voltage is higher than the reference input voltage, the INTiCOUT bit in the INTCMP register is set to 1. If the analog input voltage is lower than the reference input voltage, the INTiCOUT bit is set to 0. To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bi interrupt request is generated. Refer to **27.4 Comparator B1 and Comparator B3 Interrupts** for details of interrupts.

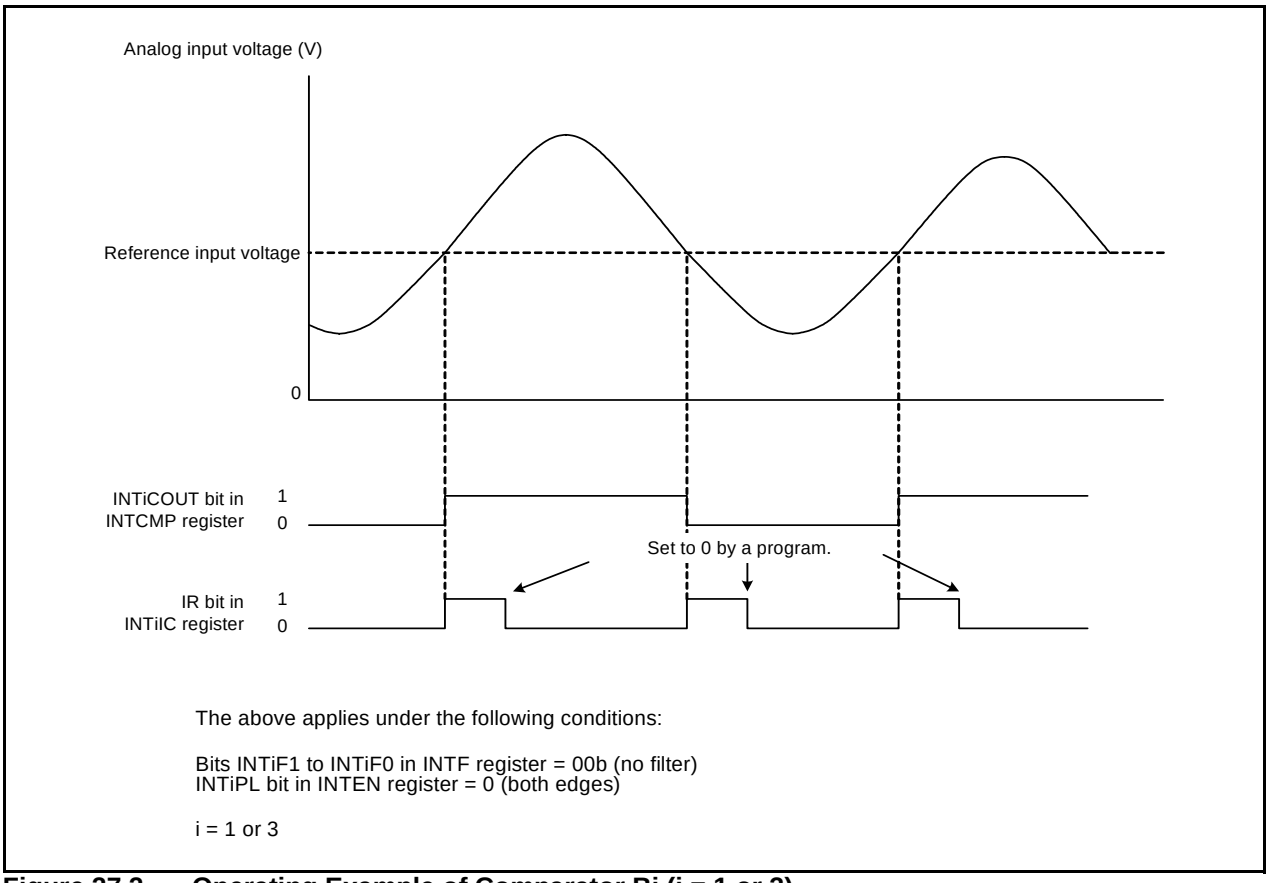

Analog input voltage (V)
Reference input voltage
0
INTiCOUT bit in INTCMP register
1
0
Set to 0 by a program.
IR bit in INTiIC register
1
0
The above applies under the following conditions:
Bits INTiF1 to INTiF0 in INTF register = 00b (no filter)
INTiPL bit in INTEN register = 0 (both edges)
i = 1 or 3

Figure 27.2 Operating Example of Comparator Bi (i = 1 or 3)

27.3.1 Comparator Bi Digital Filter (i = 1 or 3)

Comparator Bi can use the same digital filter as the $\overline{\text{INTi}}$ input. The sampling clock can be selected by bits INTiF0 and INTiF1 in the INTF register. The INTiCOUT signal output from comparator Bi is sampled every sampling clock. When the level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).

Figure 27.3 shows the Configuration of Comparator Bi Digital Filter, and Figure 27.4 shows an Operating Example of Comparator Bi Digital Filter.

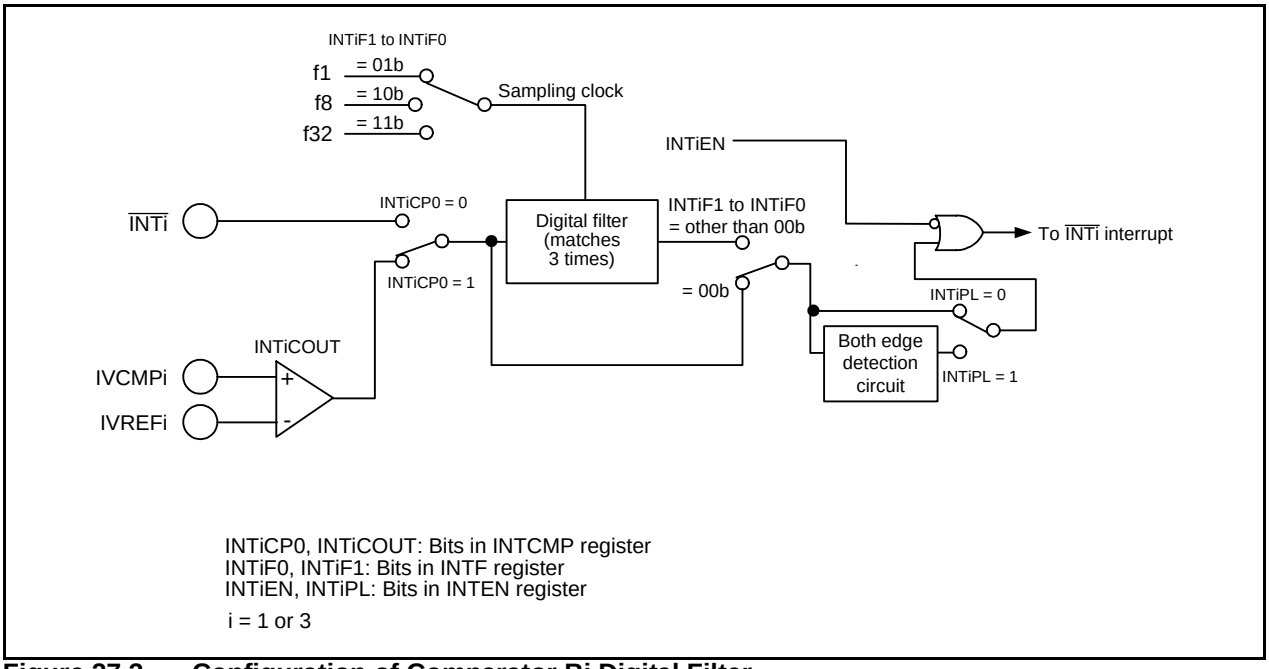


Figure 27.3 Configuration of Comparator Bi Digital Filter

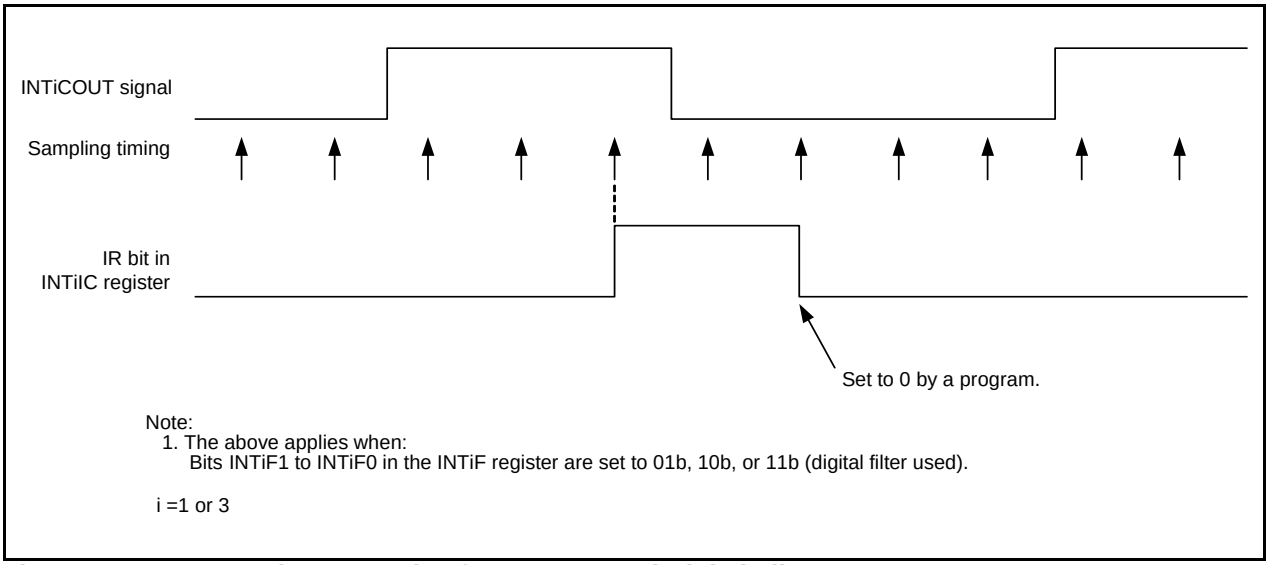

INTiCOUT signal
Sampling timing
IR bit in
INTiIC register
Set to 0 by a program.
Note:
1. The above applies when:
Bits INTiF1 to INTiF0 in the INTiF register are set to 01b, 10b, or 11b (digital filter used).
i =1 or 3

Figure 27.4 Operating Example of Comparator Bi Digital Filter

27.4 Comparator B1 and Comparator B3 Interrupts

Comparator B generates an interrupt request from two sources, comparator B1 and comparator B3. The comparator Bi (i = 1 or 3) interrupt uses the same INTiIC register (bits IR and ILVL0 to ILVL2) as the INTi (i = 1 or 3) and a single vector.

To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). In addition, the polarity can be selected by the INTiPL bit in the INTEN register and the POL bit in the INTiIC register.

Inputs can also be passed through the digital filter with three different sampling clocks.

28. LCD Drive Control Circuit

Note

The description offered in this chapter is based on the R8C/LA8A Group.
For other groups, refer to 1.1.2 Differences between Groups.

28.1 Introduction

This circuit is a drive control circuit for a liquid crystal display (LCD).
A maximum of 40 pins can be used for segment output and 4 pins for common output. Up to 160 pixels of an LCD display can be controlled.
Segment output pins, common output pins, and the LCD power supply input pins are shared with the I/O port functions.
When the LCD display function is not used, these pins are used as I/O ports.
The number of these LCD display function pins varies for each group. Table 28.1 lists the LCD Display Function Pins Provided for Each Group.
The following description applies to the R8C/LA8A Group, which have the maximum number of LCD display function pins. For other groups, note that only the pins listed in Table 28.1 are provided.

Table 28.1 LCD Display Function Pins Provided for Each Group

Shared I/O Port	R8C/LA6A Group Common output: Max. 4 Segment output: Max. 32								R8C/LA8A Group Common output: Max. 4 Segment output: Max. 40							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	—	—	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	—	—	—	—	—	—	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	—	$VL3^{(2)}$	$VL2^{(2)}$	$VL1^{(2)}$	COM 0	COM 1	COM 2	COM 3	—	$VL3^{(2)}$	$VL2^{(2)}$	$VL1^{(2)}$	COM 0	COM 1	COM 2	COM 3

Notes:
1. The symbol "–" indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE0 to LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

Table 28.2 lists the Specification Overview of LCD Drive Control Circuit. Figure 28.1 shows a Block Diagram of LCD Drive Control Circuit.

Table 28.2 Specification Overview of LCD Drive Control Circuit (1)

<table>
<tr><th>Item</th><th>Specification</th></tr>
<tr><td>Segment output</td><td>Max. 40 pins (SEG0 to SEG39)
Pins can be individually controlled for use as an I/O port or a segment output pin by setting bits LSE00 to LSE39 in registers LSE0 to LSE4.</td></tr>
<tr><td>Common output</td><td>Max. 4 pins (COM0 to COM3)
The common output pins can be selected by setting bits LDTY0 and LDTY1 in the LCR0 register.
Pins can be controlled for use as an I/O port or a common output pin by setting bits LCOM0 to LCOM3 in the LSE5 register.</td></tr>
<tr><td>LCD power supply input pins</td><td>Pins can be controlled for use as an I/O port or LCD power supply input pin by setting bits LVLP1 to LVLP3 in the LSE5 register. However, make the settings of pins VL1 to VL3 at the same time.</td></tr>
<tr><td>Maximum number of display pixels</td><td>
<table>
<tr><th rowspan="2">Duty</th><th colspan="2">LCR0 Register</th><th rowspan="2">Common Pin</th><th rowspan="2">Maximum Number of Display Pixels</th></tr>
<tr><th>LDTY1</th><th>LDTY0</th></tr>
<tr><td>Static</td><td>0</td><td>0</td><td>COM0</td><td>40 dots or 8-segment LCD 5 digits</td></tr>
<tr><td>1/2</td><td>0</td><td>1</td><td>COM0 to COM1</td><td>80 dots or 8-segment LCD 10 digits</td></tr>
<tr><td>1/3</td><td>1</td><td>0</td><td>COM0 to COM2</td><td>120 dots or 8-segment LCD 15 digits</td></tr>
<tr><td>1/4</td><td>1</td><td>1</td><td>COM0 to COM3</td><td>160 dots or 8-segment LCD 20 digits</td></tr>
</table>
</td></tr>
<tr><td>LCD drive timing</td><td>The frequency of the internal signal LCDCK for determining the LCD drive timing:
$f(LCDCK) = \frac{\text{Frequency of LCD clock source}}{n \times \text{division ratio}}$
Notes:
n = 32 when f32 is selected
n = 4 when fC-LCD is selected
The frequency of the internal signal LCDCK when the OTPCK bit of the LCR2 register is 1 (valid):
$f(LCDCK) = \frac{\text{Frequency of LCD clock source}}{4 \times \text{division ratio} \times \text{option clock division ratio}}$
Frame frequency:
$f(FR) = \frac{f(LCDCK) \times \text{duty}}{2}$</td></tr>
<tr><td>Bias control</td><td>The bias can be controlled by using external division resistors.
• The LCD drive voltage is applied to the LD power supply pins VL1 to VL3 by using external division resistors.
• The following voltage values are applied to VL1 to VL3 according to the bias values set by the LBAS0 bit in the LCR0 register.
<table>
<tr><th>Bias Value</th><th>Voltage Value</th></tr>
<tr><td>1/3 bias</td><td>VL3 = VLCD
VL2 = 2/3 VLCD
VL1 = 1/3 VLCD</td></tr>
<tr><td>1/2 bias</td><td>VL3 = VLCD
VL2 = VL1 = 1/2 VLCD</td></tr>
</table>
VLCD: LCD power supply voltage</td></tr>
<tr><td>LCD display data register</td><td>Common output data corresponding to each segment output is written to bits COM0 to COM3 in registers LRA0L to LRA39L.
40 bytes
When a bit is set to 1, the corresponding segment is turned on.
When a bit is set to 0, the corresponding segment is turned off.</td></tr>
<tr><td>Interrupt according to the LCD display period</td><td>• An interrupt is enabled by setting the LINTE bit in the LCR4 register.
• The interrupt generation timing can be selected by setting the LINTS0 bit in the LCR4 register.
When LINTS0 is set to 0, an interrupt is generated at the falling edge of each frame.
When LINTS0 is set to 1, an interrupt is generated at the falling edge of LCDCK.
• While the memory-type liquid crystal panel is driven, a frame interrupt is generated after two frames are completed.</td></tr>
<tr><td>Pin status after reset</td><td>SEG0 to SEG39: High impedance
COM0 to COM3: High impedance
VL1 to VL3: High impedance</td></tr>
</table>

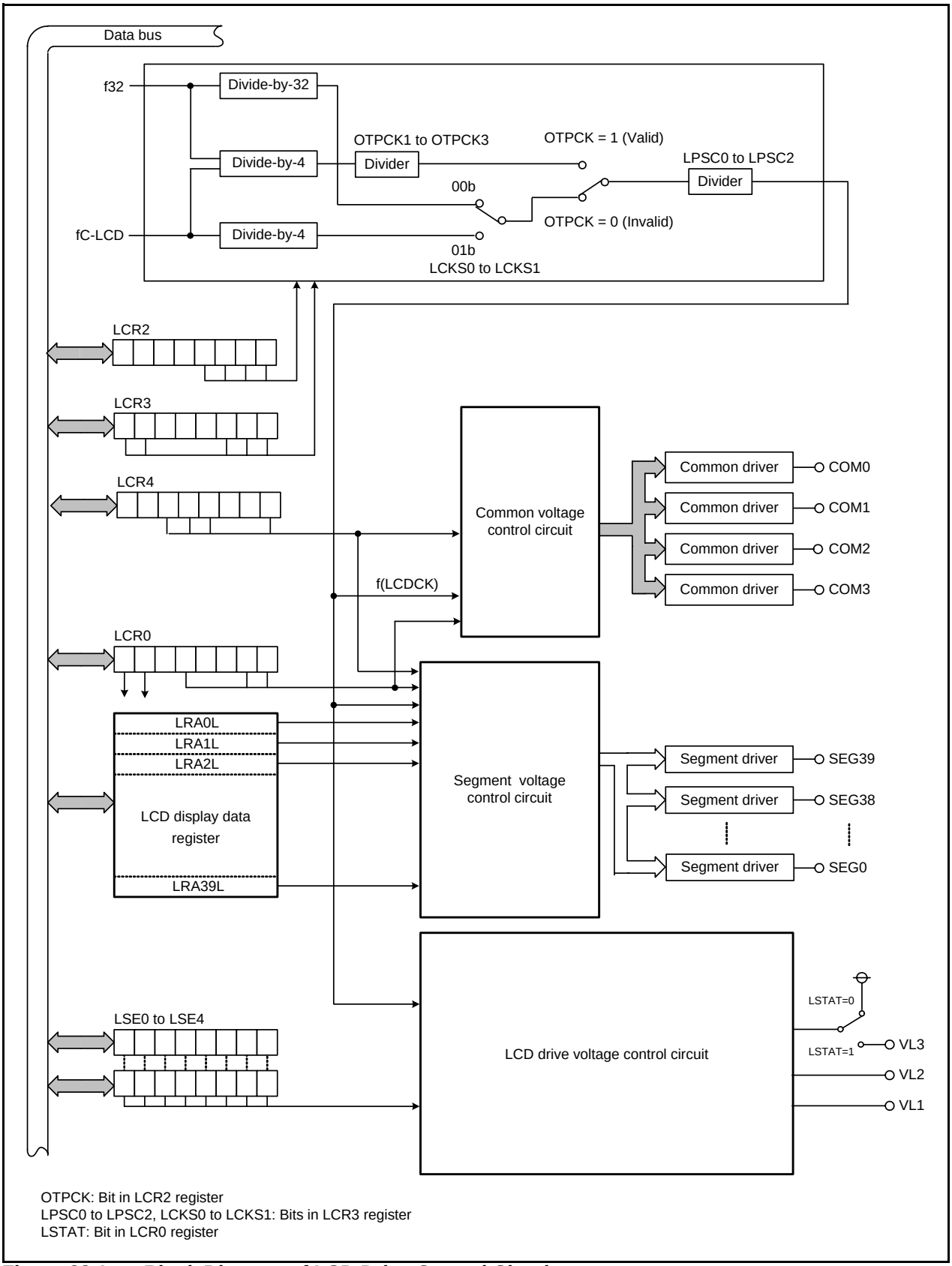


Figure 28.1 Block Diagram of LCD Drive Control Circuit

28.2 Registers

28.2.1 Module Standby Control Register 0 (MSTCR0)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MSTADC	—	MSTTRC	MSTLCD	MSTIIC	MSTURT2	MSTURT0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reseved bit	Set to 0.	R/W
b1	MSTURT0	UART0 standby bit	0: Active 1: Standby (1)	R/W
b2	MSTURT2	UART2 standby bit	0: Active 1: Standby (2)	R/W
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (3)	R/W
b4	MSTLCD	LCD standby bit	0: Active 1: Standby (4)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (5)	R/W
b6	—	Reseved bit	Set to 0.	R/W
b7	MSTADC	A/D standby bit (6)	0: Active 1: Standby	R/W

Notes:

1. When the MSTURT0 bit is set to 1 (standby), any access to the UART0 associated registers (addresses 00A0h to 00A7h) is disabled.
2. When the MSTURT2 bit is set to 1 (standby), any access to the timer UART2 associated registers (addresses 00A8h to 00BFh) is disabled.
3. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
4. When the MSTLCD bit is set to 1 (standby), any access to the timer LCD associated registers (addresses 0200h to 0237h) is disabled.
5. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
6. When the MSTADC bit is set to 1 (standby), any access to the timer A/D associated registers (addresses 00C0h to 00D9h, 00DCh to 00DFh) is disabled.
   Set the MSTADC bit to 0 (active) when the temperature sensor is used.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand. When peripheral functions are set to standby using each standby bit, their registers cannot be read or written. Also, the clock supply to the peripheral functions is stopped.
When changing from standby to active, set the registers of the corresponding peripheral function again after changing.

28.2.2 LCD Control Register (LCR0)

Address 0200h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSTAT	LDSPE	—	LBAS0	—	—	LDTY1	LDTY0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LDTY0	Duty Select Bit	b1 b0 0 0: Static (COM0 used) 0 1: 1/2 duty (COM0 and COM1 used) 1 0: 1/3 duty (COM0 to COM2 used) 1 1: 1/4 duty (COM0 to COM3 used)	R/W
b1	LDTY1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	LBAS0	LCD Bias select bit	0: 1/2 bias 1: 1/3 bias	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	LDSPE	LCD display enable bit	0: LCD panel turned off 1: LCD panel turned on	R/W
b7	LSTAT	LCD control start bit	0: LCD control stops 1: LCD control starts (1)	R/W

Note:
1. When the LCTZS bit in the LCR4 register is set to 1, the LSTAT bit is automatically set to 0 after the display ends.

28.2.3 LCD Option Clock Control Register (LCR2)

Address 0202h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OTPCK3	OTPCK2	OTPCK1	OTPCK
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OTPCK	Option clock select bit	0: Invalid 1: Valid	R/W
b1	OTPCK1	Option clock divide bit (1)	b3 b2 b1 0 0 0: Divide-by-2 0 0 1: Divide-by-3 0 1 0: Divide-by-4 0 1 1: Divide-by-5 1 0 0: Divide-by-6 1 0 1: Divide-by-7 1 1 0: Divide-by-8 1 1 1: Divide-by-9	R/W
b2	OTPCK2			R/W
b3	OTPCK3			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. Valid when the OTPCK bit is set to 1.

The LCR2 register is used to optimize the LCD drive waveform of memory-type liquid crystal panels manufactured by Citizen Seimitsu Co., LTD.
The frequency of the internal signal LCDCK when the OTPCK bit is 1 (valid)

$$f(LCDCK) = \frac{\text{Frequency of LCD clock source}}{4 \times \text{division ratio} \times \text{option clock division ratio}}$$

28.2.4 LCD Clock Control Register (LCR3)

Address 0203h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LCKS1	LCKS0	—	—	—	LPSC2	LPSC1	LPSC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LPSC0	Division ratio select bit	b2 b1 b0 0 0 0: No division 0 0 1: Divide-by-2 0 1 0: Divide-by-4 0 1 1: Divide-by-8 1 0 0: Divide-by-16 1 0 1: Divide-by-32 1 1 0: Divide-by-64 1 1 1: Divide-by-128	R/W
b1	LPSC1			R/W
b2	LPSC2			R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	LCKS0	LCD clock source select bit	b7 b6 0 0: f32 0 1: fC-LCD 1 0: Do not set. 1 1: Do not set.	R/W
b7	LCKS1			R/W

28.2.5 LCD Display Control Register (LCR4)

Address 0204h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	COMEXP	LCTZS	LINTE	—	—	LINTS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LINTS0	Interrupt timing select bit	0: Frame interrupt 1: LCDCK interrupt	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	LINTE	Counter interrupt enable bit	0: Disabled 1: Enabled	R/W
b4	LCTZS	Display waveform switch bit (1)	0: LCD drive waveform of segment panel 1: LCD drive waveform of memory-type liquid crystal panel (1)	R/W
b5	COMEXP	Memory-type liquid crystal panel COM output set bit	0: P4_7 is set to SEG39 1: P4_7 is set to COMEXP waveform	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Note:
1. The LCTZS bit is used to optimize the LCD drive waveform of memory-type liquid crystal panels manufactured by Citizen Seimitsu Co., LTD.
   Do not change the value set in the LCTZS bit while the LCD is driven.

28.2.6 LCD Port Select Register 0 (LSE0)

Address 0206h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE07	LSE06	LSE05	LSE04	LSE03	LSE02	LSE01	LSE00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE00	LCD port select bit 0	0: Port P0_0 1: SEG0	R/W
b1	LSE01	LCD port select bit 1	0: Port P0_1 1: SEG1	R/W
b2	LSE02	LCD port select bit 2	0: Port P0_2 1: SEG2	R/W
b3	LSE03	LCD port select bit 3	0: Port P0_3 1: SEG3	R/W
b4	LSE04	LCD port select bit 4	0: Port P0_4 1: SEG4	R/W
b5	LSE05	LCD port select bit 5	0: Port P0_5 1: SEG5	R/W
b6	LSE06	LCD port select bit 6	0: Port P0_6 1: SEG6	R/W
b7	LSE07	LCD port select bit 7	0: Port P0_7 1: SEG7	R/W

28.2.7 LCD Port Select Register 1 (LSE1)

Address 0207h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE15	LSE14	LSE13	LSE12	LSE11	LSE10	LSE09	LSE08
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE08	LCD port select bit 8	0: Port P1_0 1: SEG8	R/W
b1	LSE09	LCD port select bit 9	0: Port P1_1 1: SEG9	R/W
b2	LSE10	LCD port select bit 10	0: Port P1_2 1: SEG10	R/W
b3	LSE11	LCD port select bit 11	0: Port P1_3 1: SEG11	R/W
b4	LSE12	LCD port select bit 12	0: Port P1_4 1: SEG12	R/W
b5	LSE13	LCD port select bit 13	0: Port P1_5 1: SEG13	R/W
b6	LSE14	LCD port select bit 14	0: Port P1_6 1: SEG14	R/W
b7	LSE15	LCD port select bit 15	0: Port P1_7 1: SEG15	R/W

28.2.8 LCD Port Select Register 2 (LSE2)

Address 0208h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE23	LSE22	LSE21	LSE20	LSE19	LSE18	LSE17	LSE16
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE16	LCD port select bit 16	0: Port P2_0 1: SEG16	R/W
b1	LSE17	LCD port select bit 17	0: Port P2_1 1: SEG17	R/W
b2	LSE18	LCD port select bit 18	0: Port P2_2 1: SEG18	R/W
b3	LSE19	LCD port select bit 19	0: Port P2_3 1: SEG19	R/W
b4	LSE20	LCD port select bit 20	0: Port P2_4 1: SEG20	R/W
b5	LSE21	LCD port select bit 21	0: Port P2_5 1: SEG21	R/W
b6	LSE22	LCD port select bit 22	0: Port P2_6 1: SEG22	R/W
b7	LSE23	LCD port select bit 23	0: Port P2_7 1: SEG23	R/W

28.2.9 LCD Port Select Register 3 (LSE3)

Address 0209h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE31	LSE30	LSE29	LSE28	LSE27	LSE26	LSE25	LSE24
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE24	LCD port select bit 24	0: Port P3_0 1: SEG24	R/W
b1	LSE25	LCD port select bit 25	0: Port P3_1 1: SEG25	R/W
b2	LSE26	LCD port select bit 26	0: Port P3_2 1: SEG26	R/W
b3	LSE27	LCD port select bit 27	0: Port P3_3 1: SEG27	R/W
b4	LSE28	LCD port select bit 28	0: Port P3_4 1: SEG28	R/W
b5	LSE29	LCD port select bit 29	0: Port P3_5 1: SEG29	R/W
b6	LSE30	LCD port select bit 30	0: Port P3_6 1: SEG30	R/W
b7	LSE31	LCD port select bit 31	0: Port P3_7 1: SEG31	R/W

28.2.10 LCD Port Select Register 4 (LSE4)

Address 020Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSE39	LSE38	LSE37	LSE36	LSE35	LSE34	LSE33	LSE32
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LSE32	LCD port select bit 32	0: Port P4_0 1: SEG32	R/W
b1	LSE33	LCD port select bit 33	0: Port P4_1 1: SEG33	R/W
b2	LSE34	LCD port select bit 34	0: Port P4_2 1: SEG34	R/W
b3	LSE35	LCD port select bit 35	0: Port P4_3 1: SEG35	R/W
b4	LSE36	LCD port select bit 36	0: Port P4_4 1: SEG36	R/W
b5	LSE37	LCD port select bit 37	0: Port P4_5 1: SEG37	R/W
b6	LSE38	LCD port select bit 38	0: Port P4_6 1: SEG38	R/W
b7	LSE39	LCD port select bit 39	0: Port P4_7 1: SEG39/COMEXP (1)	R/W

Note:
1. Pins SEG39 and COMEXP can be selected by the COMEXP bit in the LCR4 register.
   The COMEXP pin is a LCD common output pin for the memory-type liquid crystal panel.
   This pin is used as a common signal for non pixels depending on the specifications of the memory-type liquid crystal panel.

28.2.11 LCD Port Select Register 5 (LSE5)

Address 020Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	LVLP3	LVLP2	LVLP1	LCOM3	LCOM2	LCOM1	LCOM0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LCOM0	LCDCOM port select bit 0	0: Port P5_0 1: COM3	R/W
b1	LCOM1	LCDCOM port select bit 1	0: Port P5_1 1: COM2	R/W
b2	LCOM2	LCDCOM port select bit 2	0: Port P5_2 1: COM1	R/W
b3	LCOM3	LCDCOM port select bit 3	0: Port P5_3 1: COM0	R/W
b4	LVLP1	LCDVL port select bit 1 (1)	0: Port P5_4 1: VL1	R/W
b5	LVLP2	LCDVL port select bit 2 (1)	0: Port P5_5 1: VL2	R/W
b6	LVLP3	LCDVL port select bit 3 (1)	0: Port P5_6 1: VL3	R/W
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

28.3 Data Registers

When 1 is written to a bit in the LCD display data register, the corresponding segment of the LCD panel is turned on. When 0 is written to a bit, the corresponding segment is turned off.

Symbol	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
LRA0L	0210h	Do not set.				SEG0			
LRA1L	0211h					SEG1			
LRA2L	0212h					SEG2			
LRA3L	0213h					SEG3			
LRA4L	0214h					SEG4			
LRA5L	0215h					SEG5			
LRA6L	0216h					SEG6			
LRA7L	0217h					SEG7			
LRA8L	0218h					SEG8			
LRA9L	0219h					SEG9			
LRA10L	021Ah					SEG10			
LRA11L	021Bh					SEG11			
LRA12L	021Ch					SEG12			
LRA13L	021Dh					SEG13			
LRA14L	021Eh					SEG14			
LRA15L	021Fh					SEG15			
LRA16L	0220h					SEG16			
LRA17L	0221h					SEG17			
LRA18L	0222h					SEG18			
LRA19L	0223h					SEG19			
LRA20L	0224h					SEG20			
LRA21L	0225h					SEG21			
LRA22L	0226h					SEG22			
LRA23L	0227h					SEG23			
LRA24L	0228h					SEG24			
LRA25L	0229h					SEG25			
LRA26L	022Ah					SEG26			
LRA27L	022Bh					SEG27			
LRA28L	022Ch					SEG28			
LRA29L	022Dh					SEG29			
LRA30L	022Eh					SEG30			
LRA31L	022Fh					SEG31			
LRA32L	0230h					SEG32			
LRA33L	0231h					SEG33			
LRA34L	0232h					SEG34			
LRA35L	0233h					SEG35			
LRA36L	0234h					SEG36			
LRA37L	0235h					SEG37			
LRA38L	0236h					SEG38			
LRA39L	0237h					SEG39			

Figure 28.2 LCD Display Data Register

28.4 LCD Drive Control

Table 28.3 and Table 28.4 show outlines of the LCD drive control procedure.

Table 28.3 LCD Drive Control Procedure and Status of Segment and Common Pins (Normal)

Procedure	Status of Segment and Common Pins
Reset	• I/O port (input) • High-impedance state (Depending on the pull-up control registers)
LSE0 to LSE5 register setting • Select segment output pins, common output pins, and the LCD power supply input pins	• High-impedance
LRA0L to LRA39L register initial setting • Set the initial value for the data output from the SEG pins	
LCR3 register setting • Bits LCKS0 and LCKS1: Select the LCD clock source • Bits LPSC0 to LPSC2: Select the division ratio	
LCR0 register setting • LSTAT bit: Start LCD control • LDSPE bit: Enable LCD display • LBAS0 bit: Select the bias • Bits LDTY0 and LDTY1: Select the duty	At start of LCD control • The content of the PiPUR register (i = 0 to 5) is invalid. • When the LDSPE bit is set to 0, the segment output and common output pins output a low-level signal. • When the LDSPE bit is set to 1, the segment output and common output pins output the content of the LCD display data register.
LRA0L to LRA39L register setting • Set the data output from the SEG pins	

Table 28.4 LCD Drive Control Procedure and Status of Segment and Common Pins (Memory-Type Liquid Crystal Panel)

Procedure	Status of Segment and Common Pins
Reset	• I/O port (input) • High-impedance state (Depending on the pull-up control registers)
LSE0 to LSE5 register setting • Select segment output pins, common output pins, and the LCD power supply input pins	• High-impedance
LRA0L to LRA39L register initial setting • Set the initial value for the data output from the SEG pins	
LCR2 register setting • OTPCK bit: Select the option clock • Bits OTPCK1 to OTPCK3: Select the division	
LCR3 register setting • Bits LCKS0 and LCKS1: Select the LCD clock source • Bits LPSC0 to LPSC2: Select the division ratio	
LCR4 register setting • LCTZS bit: Select the LCD drive waveform memory-type liquid crystal panel • COMEXP bit: Select the COMEXP waveform for P4_7	
LCR0 register setting • LBAS0 bit: Select the bias • Bits LDTY0 and LDTY1: Select the duty	
LRA0L to LRA39L register setting • Set the data output from the SEG pins	At start of LCD control • The content of the PiPUR register (i = 0 to 5) is invalid. • When the LDSPE bit is set to 0, the segment output and common output pins output a low-level signal. • When the LDSPE bit is set to 1, the segment output and common output pins output the content of the LCD display data register.
LCR0 register setting • LSTAT bit: Start LCD control • LDSPE bit: Enable LCD display	

28.4.1 Segment Output Pin Selection

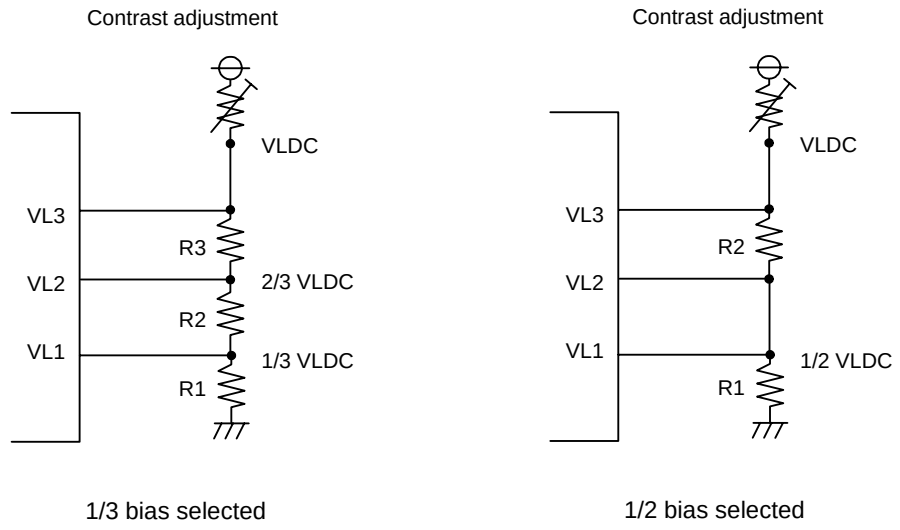
All of the segment output pins SEG0 to SEG39, common output pins COM0 to COM3, and LCD power supply pins VL1 to VL3 are shared with I/O ports. All these pins function as I/O ports after a reset. Thus, set the corresponding LSEi (i = 00 to 39), LCOMj (j = 0 to 3), or LVLPk (k = 1 to 3) bit to 1 for the pins to be used as segment output, common output, or LCD power supply for LCD displays. Set the corresponding LSEi, LCOMj, or LVLPk bit to 0 (I/O port) for the pins not to be used as segment output, common output, or LCD power supply. If these pins are not used as I/O ports, perform unassigned pin handling for I/O ports (refer to Table 7.77 Unassigned Pin Handling).

28.4.2 LCD Clock Selection

Either f32 or fC-LCD is selected as the LCD clock source by setting bits LCKS0 and LCKS1. The division ratio is selected from a range of no division to divide-by-128 by setting bits LPSC0 to LPSC2.

28.4.3 Bias Control

The LCD drive voltage is applied to the LCD power supply input pins VL1 to VL3 by connecting division resistors. Figure 28.3 shows the Pin Connection and Voltage Levels when External Division Resistors are Used.



Notes:
1. Apply the LCD drive voltage to the LCD power supply pins VL1 to VL3 by using external division resistors.
2. Be sure to connect a smoothing capacitor to pins VL1 to VL3. (Recommended value: 0.2 μF to 0.4 μF)

Figure 28.3 Pin Connection and Voltage Levels when External Division Resistors are Used

28.4.4 LCD Data Display

The bias is selected by setting the LBAS0 bit in the LCR0 register, and the duty is selected by setting bits LDTY0 and LDTY1. An LCD display is enabled by setting the LDSPE bit to 1, and the display is started by setting the LSTAT bit to 1.
The LCD display content is changed by rewriting the content of the LCD display data register.
Do not change the content of the LCD display data register while the memory-type liquid crystal panel is driven.

28.4.5 Pin Status in Stop Mode and Power-Off 2 Mode

In stop mode and power-off 2 mode, the status of the LCD display function pins selected by bits LSE00 to LSE39 in registers LSE0 to LSE5, bits LCOM0 to LCOM3, and bits LVLP1 to LVLP3 will be as shown in Table 28.5. LCD control is restarted by means of the same operation as that used to make LCR0 register settings, as shown the LCD drive control procedure in Table 28.3.

Table 28.5 LCD Display Function Pin Status in Stop Mode and Power-Off 2 Mode

Pin Name	Pin Status
SEG0 to SEG39	Outputs a low-level signal.
COM0 to COM3	Outputs a low-level signal.
VL1 to VL3	High-impedance state

28.4.6 Pin Status in Power-Off 0 Mode

In power-off 0 mode, the status of the LCD display function pins selected by bits LSE00 to LSE39 in registers LSE0 to LSE7, bits LCOM0 to LCOM3, and bits LVLP1 to LVLP3 will be as shown in Table 28.6. The operation is started from a reset as shown in Table 28.3.

Table 28.6 LCD Display Function Pin Status in Power-Off 0 Mode

Pin Name	Pin Status
SEG0 to SEG39	Outputs a low-level signal.
COM0 to COM3	
VL1 to VL3	High-impedance state

28.5 LCD Drive Waveform

28.5.1 Segment Panel Drive Waveform

Figure 28.4 to 28.12 show the LCD drive waveform.

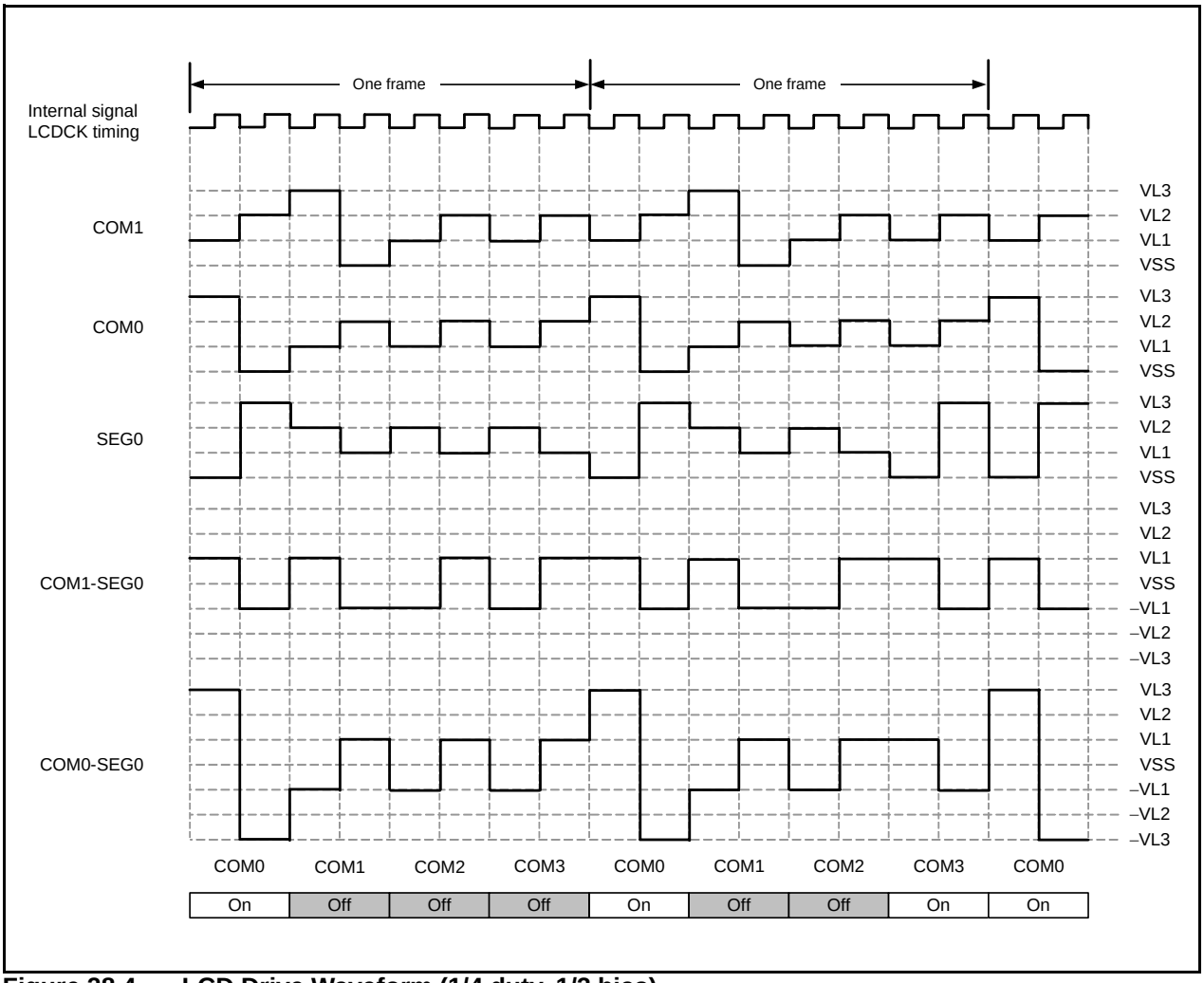


Figure 28.4 LCD Drive Waveform (1/4 duty, 1/3 bias)

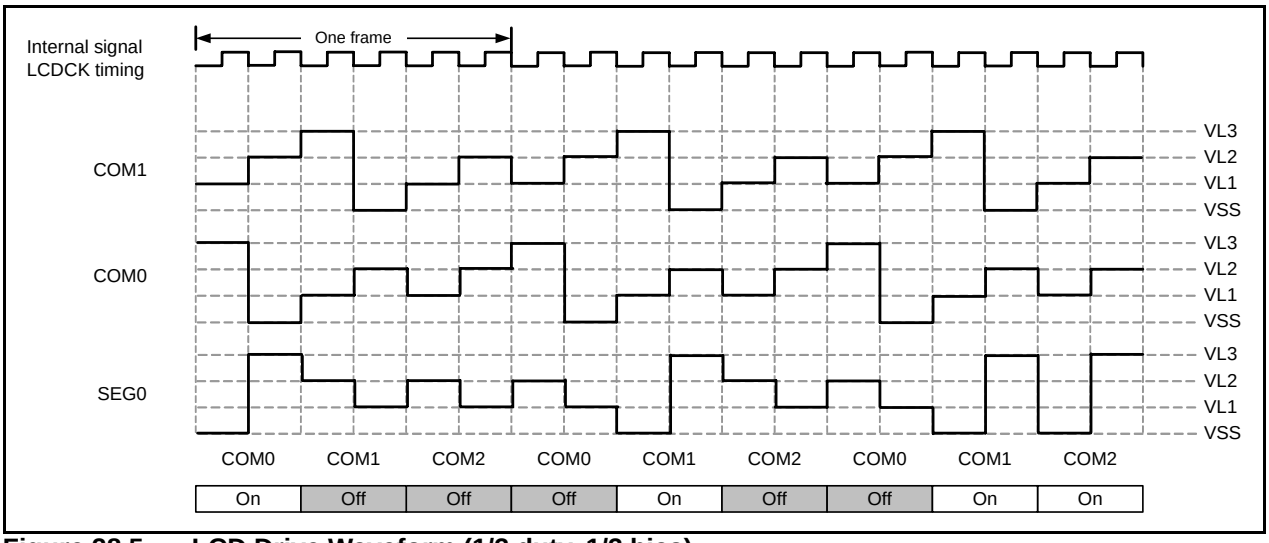


Figure 28.5 LCD Drive Waveform (1/3 duty, 1/3 bias)

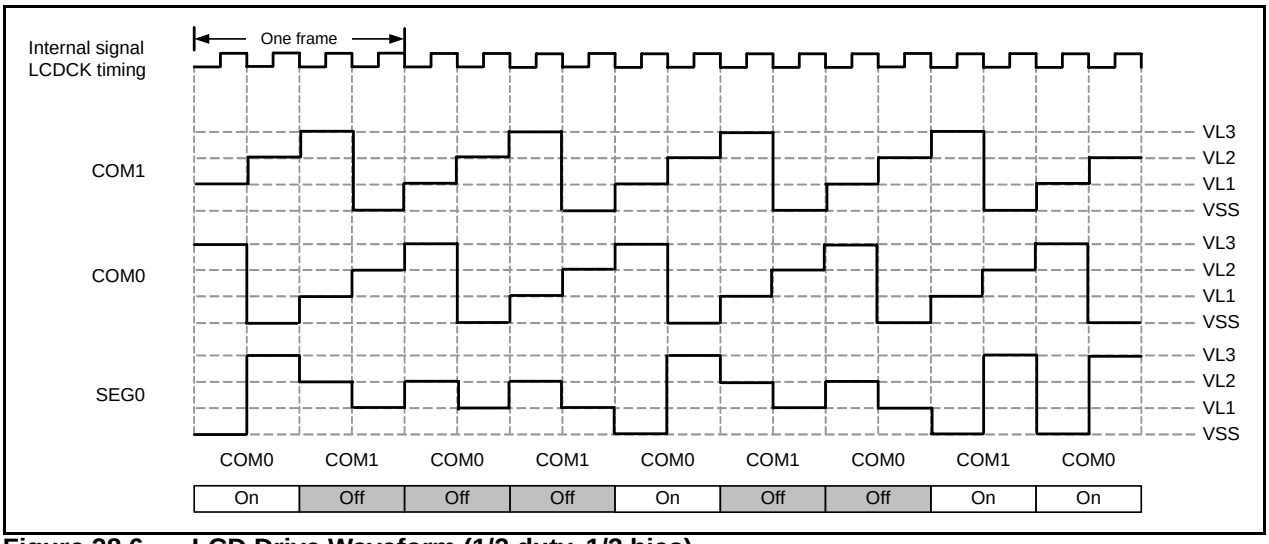


Figure 28.6 LCD Drive Waveform (1/2 duty, 1/3 bias)

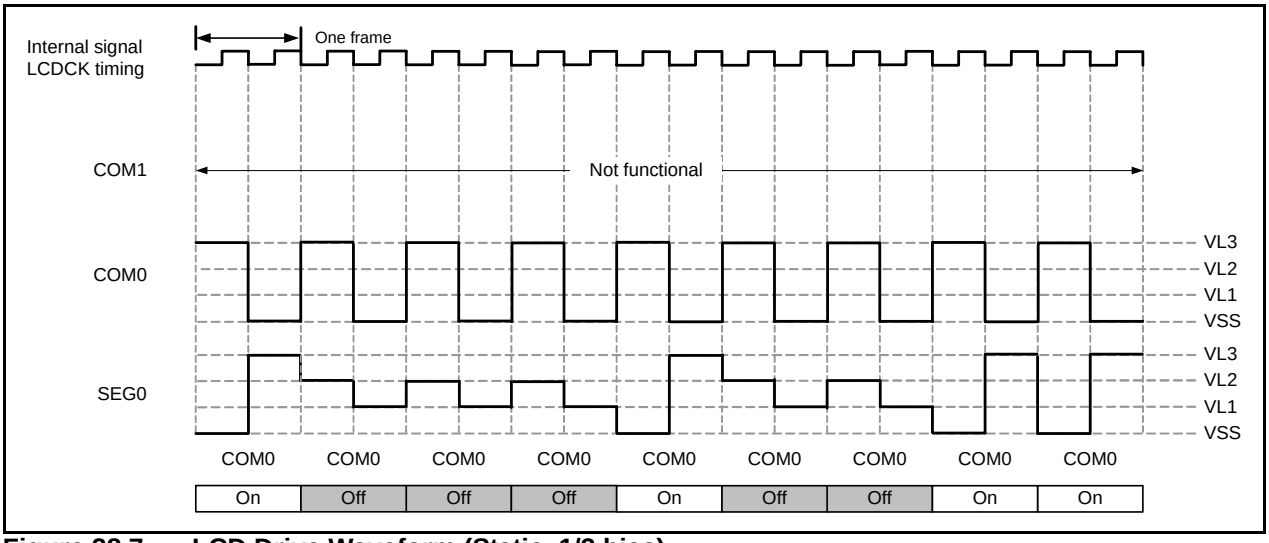


Figure 28.7 LCD Drive Waveform (Static, 1/3 bias)

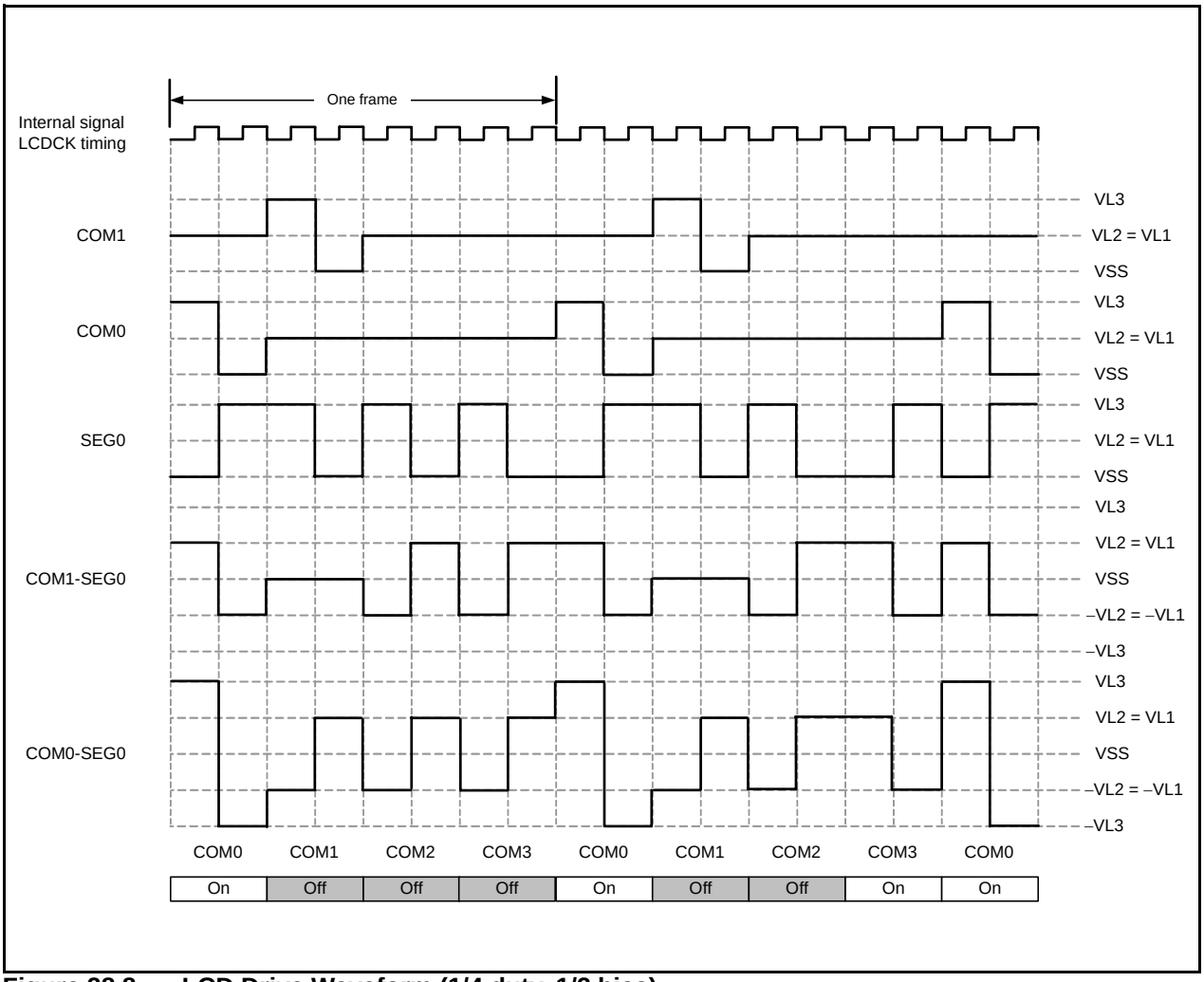


Figure 28.8 LCD Drive Waveform (1/4 duty, 1/2 bias)

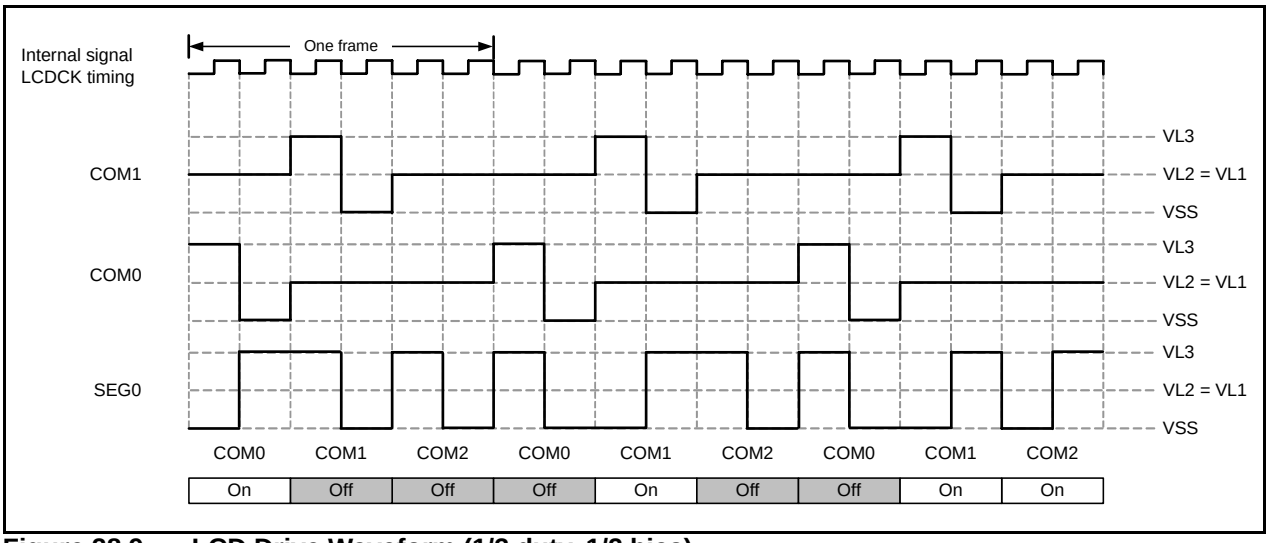


Figure 28.9 LCD Drive Waveform (1/3 duty, 1/2 bias)

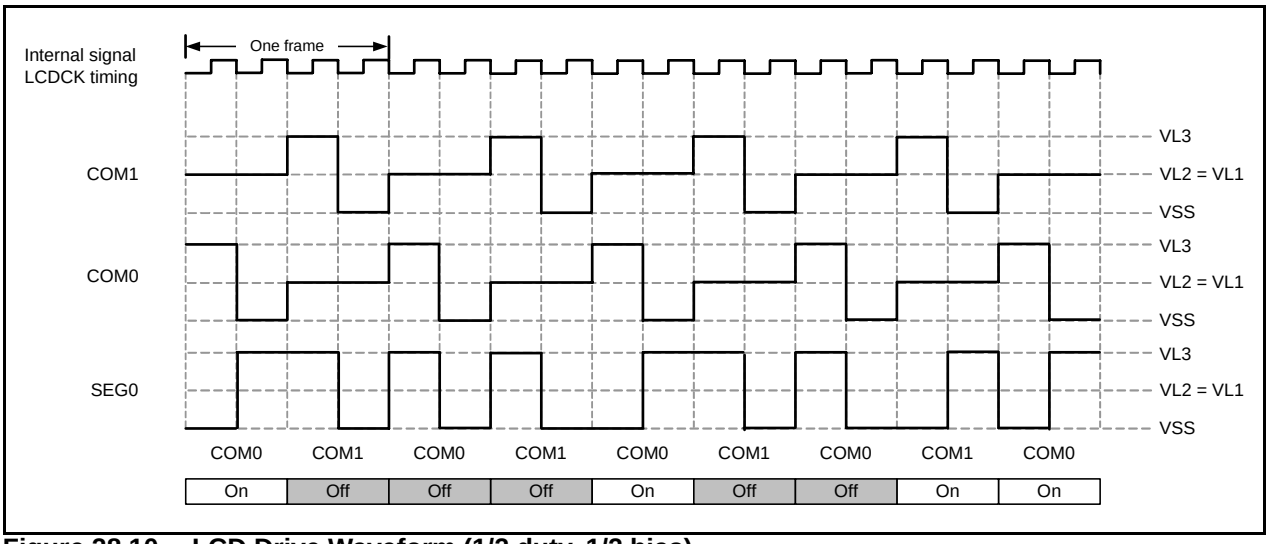


Figure 28.10 LCD Drive Waveform (1/2 duty, 1/2 bias)

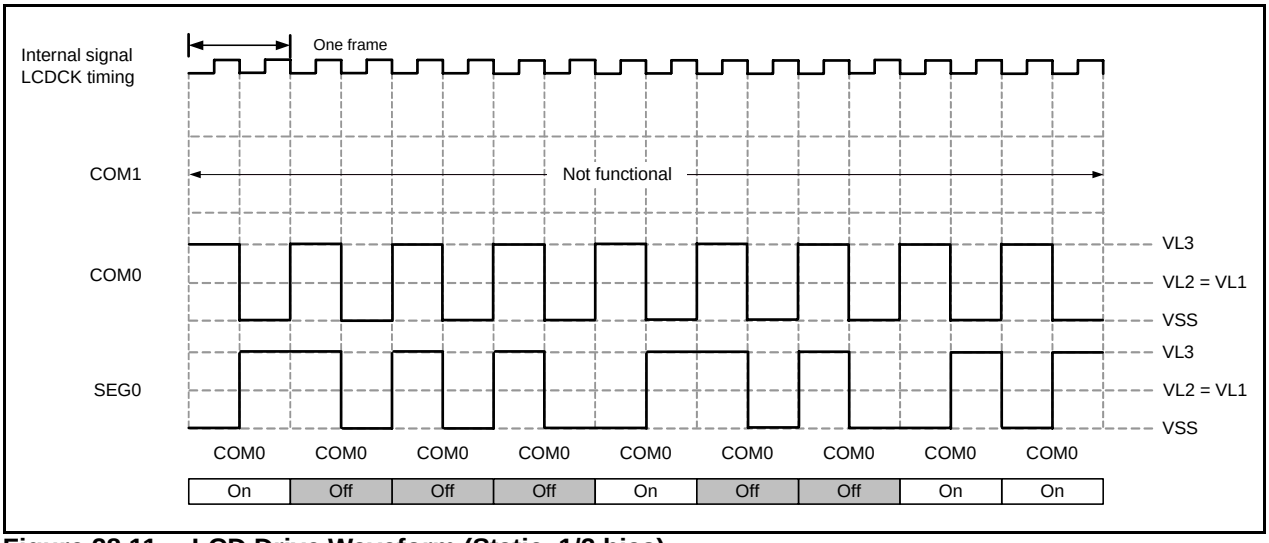


Figure 28.11 LCD Drive Waveform (Static, 1/2 bias)

28.5.2 Drive Waveform of Memory-Type Liquid Crystal Panel

Figure 28.12 shows the LCD drive waveform.

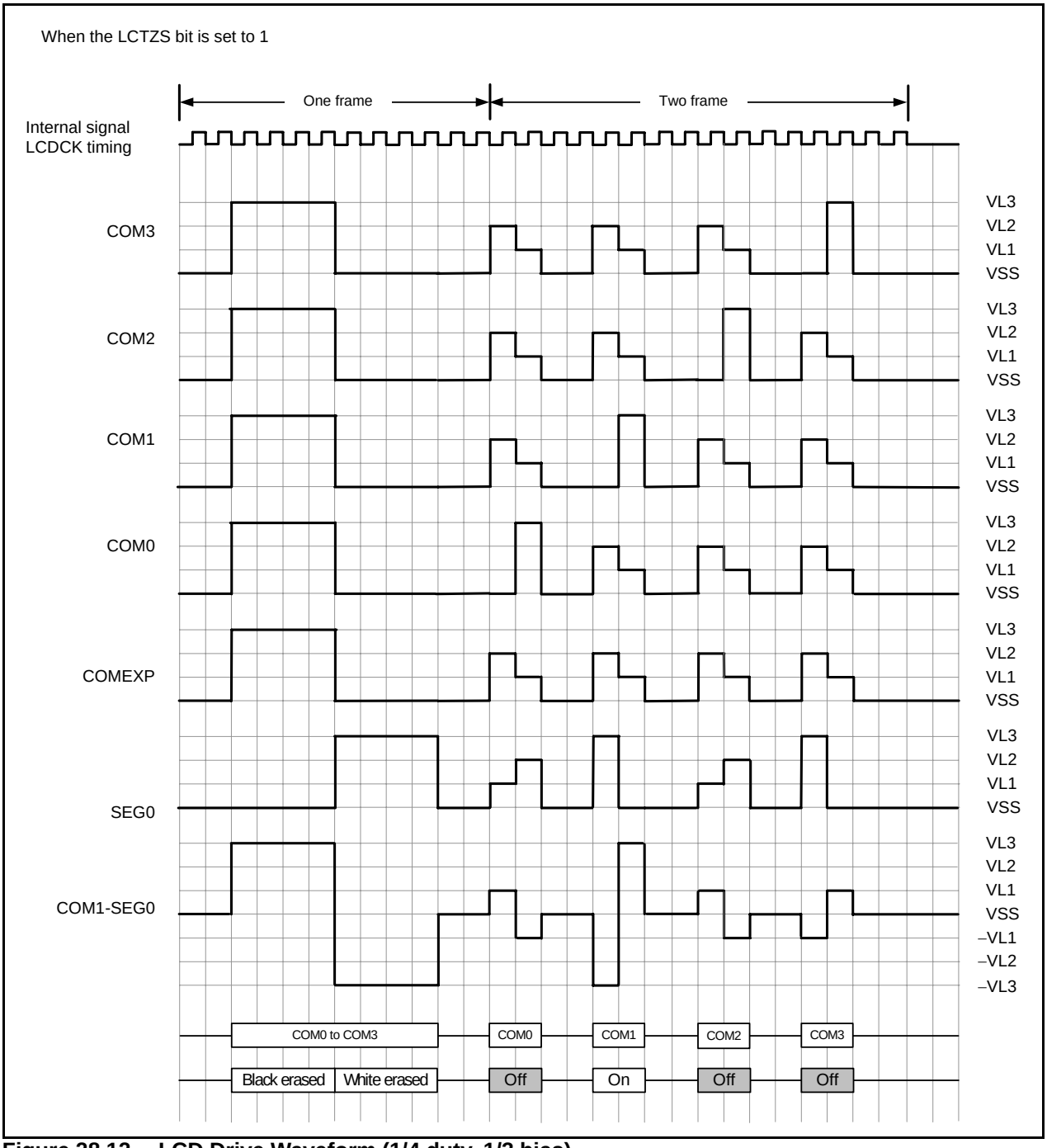


Figure 28.12 LCD Drive Waveform (1/4 duty, 1/3 bias)

28.5.3 Interrupt Control Waveform

Figure 28.13 shows the Interrupt Control Waveform.

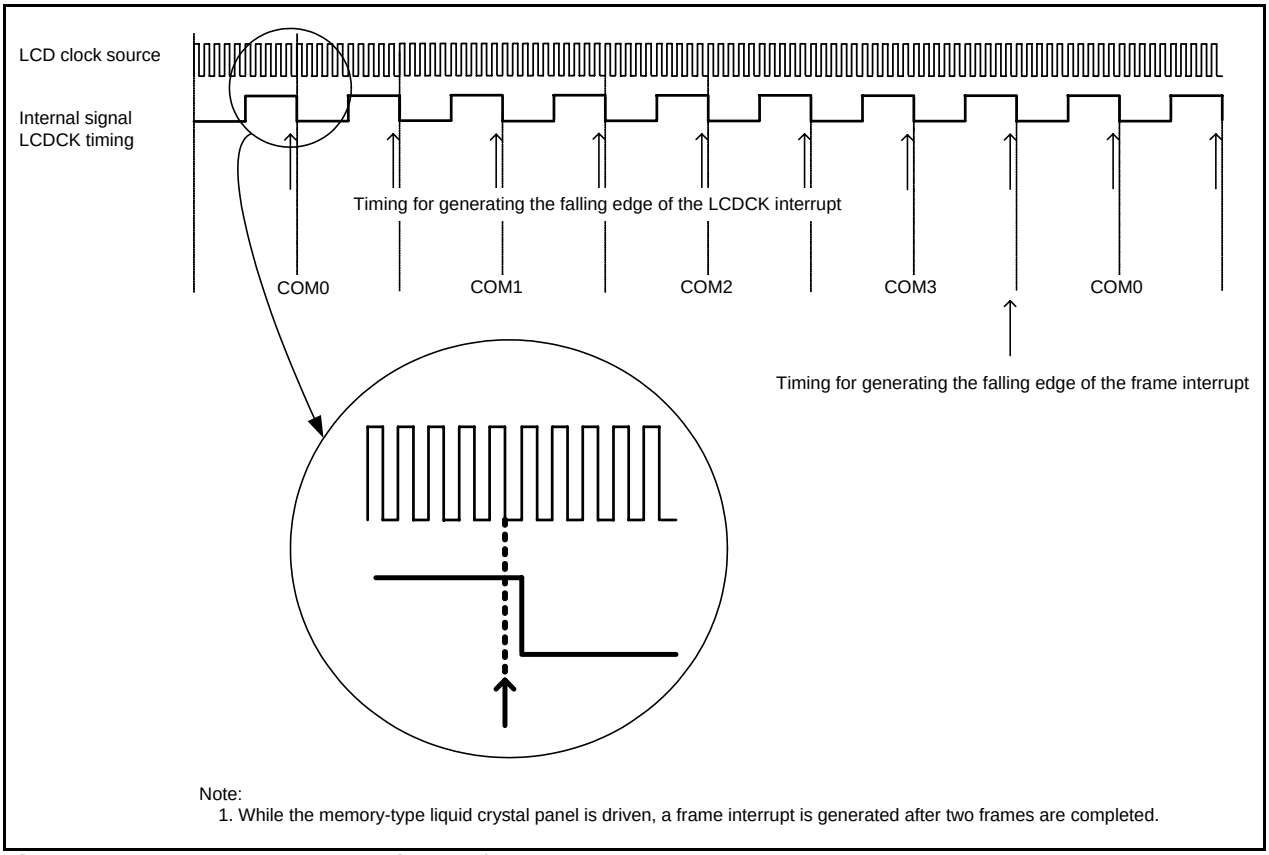

LCD clock source
Internal signal
LCDCK timing
Timing for generating the falling edge of the LCDCK interrupt
COM0
COM1
COM2
COM3
COM0
Timing for generating the falling edge of the frame interrupt
Note:
1. While the memory-type liquid crystal panel is driven, a frame interrupt is generated after two frames are completed.

Figure 28.13 Interrupt Control Waveform

28.6 Notes on LCD Drive Control Circuit

28.6.1 When Division Resistors are Connected Externally

The reference values of R1 to R3 are 10 kΩ to 200 kΩ. These reference values depend on the used LCD panel, number of segment and common pins, frame frequency, and environment. Careful evaluation should be performed for the system to determine the values (refer to Figure 28.3).

29. Flash Memory

The flash memory can perform in the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

29.1 Introduction

Table 29.1 lists the Flash Memory Version Performance. (Refer to the specifications in **Table 1.4** to **Table 1.6** for items not listed in Table 29.1.)

Table 29.1 Flash Memory Version Performance

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figure 29.1**.
Programming method		Byte units
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite control method (2)	Blocks 0 to 5 (Program ROM)(4)	Rewrite protect control in block units by the lock bit
	Blocks A and B (Data flash)	Individual rewrite protect control on blocks A and B by bits FMR14 and FMR15 in the FMR1 register
Number of commands		7 commands
Programming and erasure endurance (3)	Blocks 0 to 5 (Program ROM)(4)	10,000 times
	Blocks A, B, C, and D (Data flash)	10,000 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

Notes:
1. To program and erasure program ROM, use VCC = 1.8 V to 5.5 V as the supply voltage.
2. To program and erasure data flash, use VCC = 1.8 V to 5.5 V as the supply voltage.
3. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programing/erasure endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. The number of blocks and block division vary with the MCU. Refer to **Figure 29.1 Flash Memory Block Diagrams of R8C/LA6A Group and R8C/LA8A Group** for details.

Table 29.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten using a dedicated serial programmer.	User ROM area is rewritten using a dedicated parallel programmer.
Rewritable area	User ROM	User ROM	User ROM
Rewrite programs	User program	Standard boot program	–

29.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 29.1 shows the Flash Memory Block Diagrams of R8C/LA6A Group and R8C/LA8A Group.
The user ROM area contains program ROM and data flash.
Program ROM: Flash memory mainly used for storing programs
Data flash: Flash memory mainly used for storing data to be rewritten

The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.

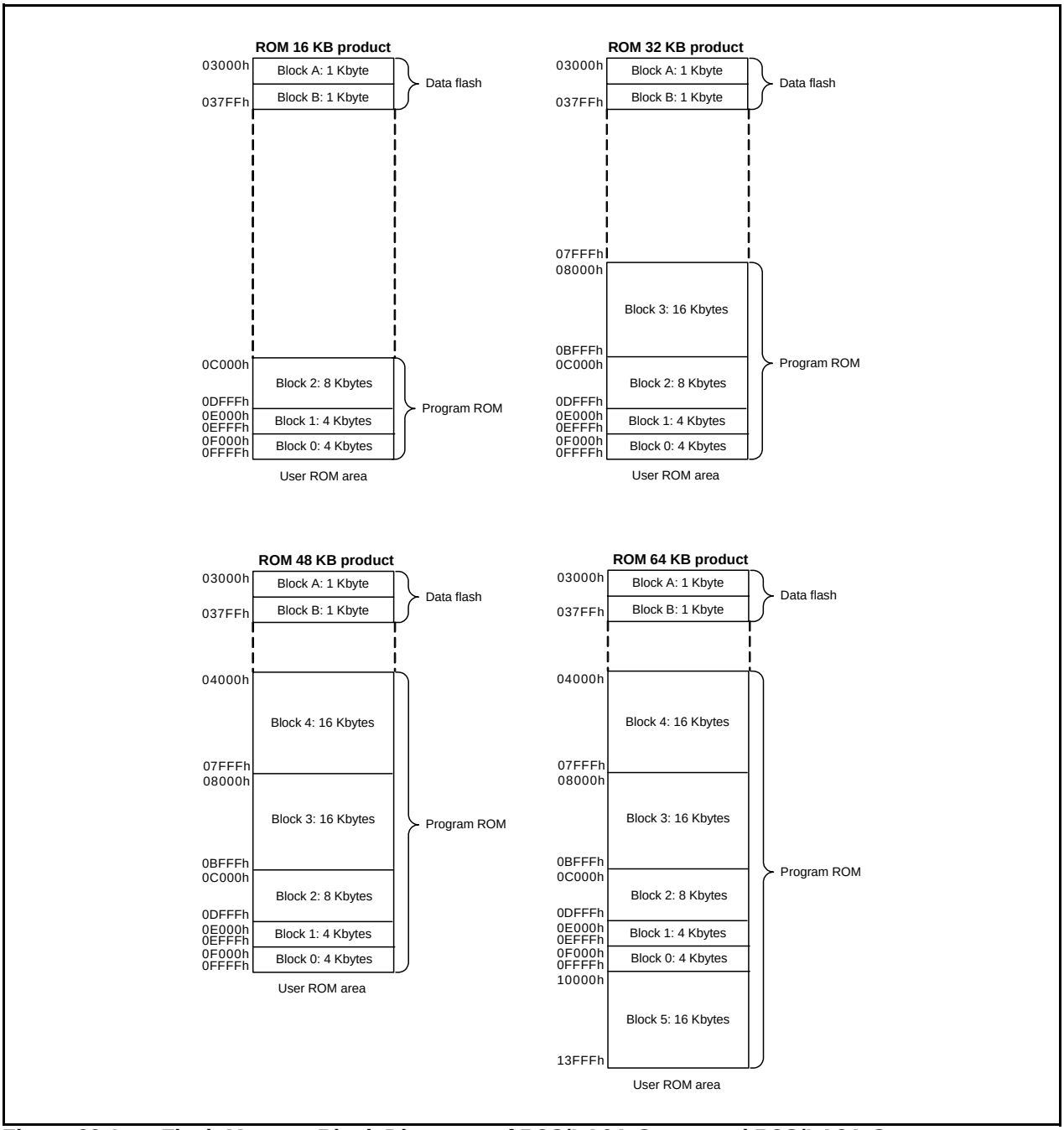


Figure 29.1 Flash Memory Block Diagrams of R8C/LA6A Group and R8C/LA8A Group

29.3 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

29.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. For details of the ID code check function, refer to **13. ID Code Areas**.

29.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.
Refer to **14. Option Function Select Area** for details of the option function select area.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the content of the on-chip flash memory from being read or rewritten.
Once ROM code protection is enabled, the content of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

29.3.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User setting value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **14.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

29.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
The flash module has a suspend function (program-suspend, erase-suspend) which halts erase or program operation temporarily in CPU rewrite mode. During suspend, the flash memory can be read. For erase-suspend only, the flash memory can also be programmed.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 29.3 lists the Differences between EW0 Mode and EW1 Mode.

Table 29.3 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Rewrite control program allocatable area	User ROM	User ROM
Rewrite control program executable areas	RAM (The rewrite control program must be transferred before being executed.)	User ROM or RAM
Rewritable area	User ROM	User ROM However, blocks which contain the rewrite control program are excluded.
Software command restrictions	—	Program and block commands cannot be executed to any block which contains the rewrite control program.
Mode after programming or block erasure or after entering suspend	Read array mode	Read array mode
CPU state during programming and block erasure	The CPU operates.	The CPU is put in a hold state during programming and block erasure. (I/O ports retain the states before the command execution).
Flash memory status detection	Read bits FST7, FST5, and FST4 in the FST register by a program.	Read bits FST7, FST5, and FST4 in the FST register by a program.
Conditions for entering erase-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
Conditions for entering program-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	Max. 20 MHz	Max. 20 MHz

29.4.1 Flash Memory Status Register (FST)

Address 01B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	FST3	LBDATA	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4)	0: No flash ready status interrupt request 1: Flash ready status interrupt request	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4)	0: No flash access error interrupt request 1: Flash access error interrupt request	R/W
b2	LBDATA	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	FST3	Program-suspend status flag	0: Other than program-suspend 1: During program-suspend	R
b4	FST4	Program error flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error flag (3)	0: No erase error/blank check error 1: Erase error/blank check error	R
b6	FST6	Erase-suspend status flag	0: Other than erase-suspend 1: During erase-suspend	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt request) by a program.
   When writing 0 (no flash ready status interrupt request) to the RDYSTI bit, read this bit (dummy read) before writing to it.
   To confirm this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt request) by a program.
   When writing 0 (no flash access error interrupt request) to the BSYAEI bit, read this bit (dummy read) before writing to it.
   To confirm this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command error occurs.
4. When this bit is set to 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

RDYSTI Bit (Flash Ready Status Flag Interrupt Request Flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt request).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt request).

[Condition for setting to 0]
Set to 0 by an interrupt handling program.
[Condition for setting to 1]
When the flash memory status changes from busy to ready while the RDYSTIE bit in the FRMR0 register is set to 1, the RDYSTI bit is set to 1.
The status is changed from busy to ready in the following states:

- Completion of erasing/programming the flash memory
- Suspend acknowledgement
- Completion of forcible termination
- Completion of the lock bit program
- Completion of the read lock bit status
- Completion of the block blank check
- When the flash memory can be read after it has been stopped.

BYSAEI Bit (Flash Access Error Interrupt Request Flag)

The BYSAEI bit is set to 1 (flash access error interrupt request) when the BSYAEIE bit in the FMR0 register is set to 1 (flash access error interrupt enabled) and the block during auto-programming/auto-erasure is accessed. This bit is also set to 1 if an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt request).

[Conditions for setting to 0]
(1) Set to 0 by an interrupt handling program.
(2) Execute the clear status register command.
[Conditions for setting to 1]
(1) Read or write the area that is being erased/written when the BSYAEIE bit in the FRMR0 register is set to 1 and while the flash memory is busy.
Or, read the data flash area while erasing/writing to the program ROM area. (Note that the read value is undefined in both cases. Writing has no effect.)
(2) If a command sequence error, erase error, blank check error, or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

LBDATA Bit (LBDATA Monitor Flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).
The condition for updating this bit is when the program, erase, read lock bit status commands are generated.
When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

FST3 Bit (Program-Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when a program-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST4 Bit (Program Error Flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. For details, refer to the description in **29.4.11 Full Status Check**.

FST5 Bit (Erase Error/Blank Check Error Flag)

This is a read-only bit indicating the status of auto-programming or the block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise, it is set to 0. Refer to **29.4.11 Full Status Check** for details.

FST6 Bit (Erase Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST7 Bit (Ready/Busy Status Flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:

- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During the block blank check
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

29.4.2 Flash Memory Control Register 0 (FMR0)

Address 01B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory stops (Low-power consumption state, flash memory initialization)	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped. When read, the content is 0.	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled 1: Erase/write error interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.
2. Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is set to 1 (ready).
3. The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).
4. To set the FMR01 bit to 0 (CPU rewrite mode disabled), set it when the RDYSTI bit in the FST register is set to 0 (no flash ready status interrupt request) and the BSYAEI bit is set to 0 (no flash access error interrupt request).

FMR01 Bit (CPU Rewrite Mode Select Bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 Mode Select Bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash Memory Stop Bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.
Write to the FMSTP bit by a program transferred to the RAM.
To reduce the power consumption further in high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stopped), and low-speed clock mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **10.8.10 Stopping Flash Memory** for details.
When entering stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when exiting stop or wait mode.
When the FMSTP bit is set to 1 (including during the busy status (the period while the FST7 bit is 0) immediately after the FMSTP bit is changed from 1 to 0), do not set to low-current-consumption read mode at the same time.

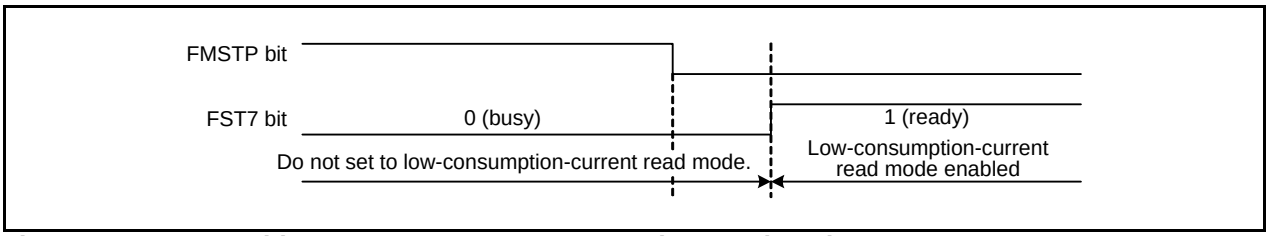


Figure 29.2 Transition to Low-Current-Consumption Read Mode

CMDRST Bit (Erase/Write Sequence Reset Bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or erase command.
If the program or erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is changed to 1 (ready). To program to the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erasure command again.
When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly terminated and reading from the flash memory is enabled.

CMDERIE Bit (Erase/Write Error Interrupt Enable Bit)

This bit enables a flash command error interrupt to be generated if the following errors occur:

- Program error
- Block erase error
- Command sequence error
- Block blank check error

If the CMDERIE bit is set to 1 (erase/write error interrupt enabled), an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

To change the CMDERIE bit from 0 (erase/write error interrupt disabled) to 1 (erase/write error interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash Access Error Interrupt Enable Bit)

This bit enables a flash access error interrupt to be generated if the flash memory during rewriting is accessed.

To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), make the setting as follows:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash Ready Status Interrupt Enable Bit)

This bit enables a flash ready status error interrupt to be generated when the status of the flash memory sequence changes from the busy to ready status.

To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), make the setting as follows:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

29.4.3 Flash Memory Control Register 1 (FMR1)

Address 01B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	FMR15	FMR14	FMR13	—	—	—
After Reset	0	0	0	0	0	0	X	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R
b2	—			R/W
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	FMR14	Data flash block A rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b5	FMR15	Data flash block B rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.
2. To set this bit to 0, first write 1 and then 0 immediately. Disable interrupts between writing 1 and writing 0.
3. This bit is set to 0 when the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).

FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **29.4.9 Data Protect Function** for the details of the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met:
- Completion of the program command
- Completion of the erase command
- Generation of a command sequence error
- Transition to erase-suspend
- The FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- The FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- The CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]
Set to 1 by a program.

FMR14 Bit (Data Flash Block A Rewrite Disable Bit)

When the FMR 14 bit is set to 0, data flash block A accepts program and block erase commands.

FMR15 Bit (Data Flash Block B Rewrite Disable Bit)

When the FMR 15 bit is set to 0, data flash block B accepts program and block erase commands.

29.4.4 Flash Memory Control Register 2 (FMR2)

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Suspend enable bit (1)	0: Suspend disabled 1: Suspend enabled	R/W
b1	FMR21	Suspend request bit (2)	0: Restart 1: Suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Suspend request disabled by interrupt request 1: Suspend request enabled by interrupt request	R/W
b3	—	Nothing is assigned. If necessary, set to 0.		—
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	FMR27	Low-current-consumption read mode enable bit (1, 3)	0: Low-current-consumption read mode disabled 1: Low-current-consumption read mode enabled	R/W

Note:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.
2. To set the FMR21 bit to 0 (restart), set it when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled).
3. Set the FMR27 bit to 1 after setting either of the following:
   - Set the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
   - Set the CPU clock to the XCIN clock divided by 1 (no division), 2, 4, or 8.

   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR20 Bit (Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the suspend function is enabled.

FMR21 Bit (Suspend Request Bit)

When the FMR21 bit is set to 1, suspend mode is entered. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request for the enabled interrupt is generated, and suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
- The FMR22 bit is set to 1 (suspend request enabled by interrupt request) when an interrupt is generated.
- Set to 1 by a program.

FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) at the time an interrupt request is generated during auto-erasure.
Set the FMR22 bit to 1 when using suspend while rewriting the user ROM area in EW1 mode.

FMR27 Bit (Low-Current-Consumption Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed clock mode (XIN clock stopped) or low-speed on-chip oscillator mode (XIN clock stopped), current consumption when reading the flash memory can be reduced. Refer to **10.8.11 Low-Current-Consumption Read Mode** for details.
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

29.4.5 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. At this time, the FMR02 bit in the FMR0 register is set to 0 so that EW0 mode is selected.
Software commands are used to control program and erase operations. The FST register can be used to confirm whether programming or erasure has completed.
To enter suspend during auto-programming or auto-erasure, set the FMR20 bit to 1 (suspend enabled) and the FMR21 bit to 1 (suspend request). Next, verify the FST7 bit in the FST register is set to 1 (ready), then verify the FST3 bit is set to 1 (during program-suspend) or the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST3 bit is set to 0, program completes, the FST6 bit is set to 0, erasure completes.
When the FMR21 bit in the FMR2 register is set to 0 (restart), auto-programming or auto-erasure restarts. To confirm whether auto-programming or auto-erasure has restarted, verify the FST7 bit in the FST register is set to 0, then verify the FST3 bit is set to 0 (other than program-suspend) the FST6 bit is set to 0 (other than erase-suspend).

29.4.6 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit is set to 1.
The FST register can be used to confirm whether programming and erasure has completed.
To enable the suspend function, execute the program or block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (suspend request enabled by interrupt request). Also, the interrupt to enter suspend must be enabled beforehand.
When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (suspend request) and auto-programming or auto-erasure suspends after td(SR-SUS). After interrupt handling completes, set the FMR21 bit to 0 (restart) to restart auto-programming or auto-erasure.

29.4.7 Suspend Operation

The suspend function halts the operation temporarily during auto-programming or auto-erasure.
When auto-programming or auto-erasure is suspended, the next operation can be executed. (Refer to **Table 29.4 Executable Operation during Suspend**.)

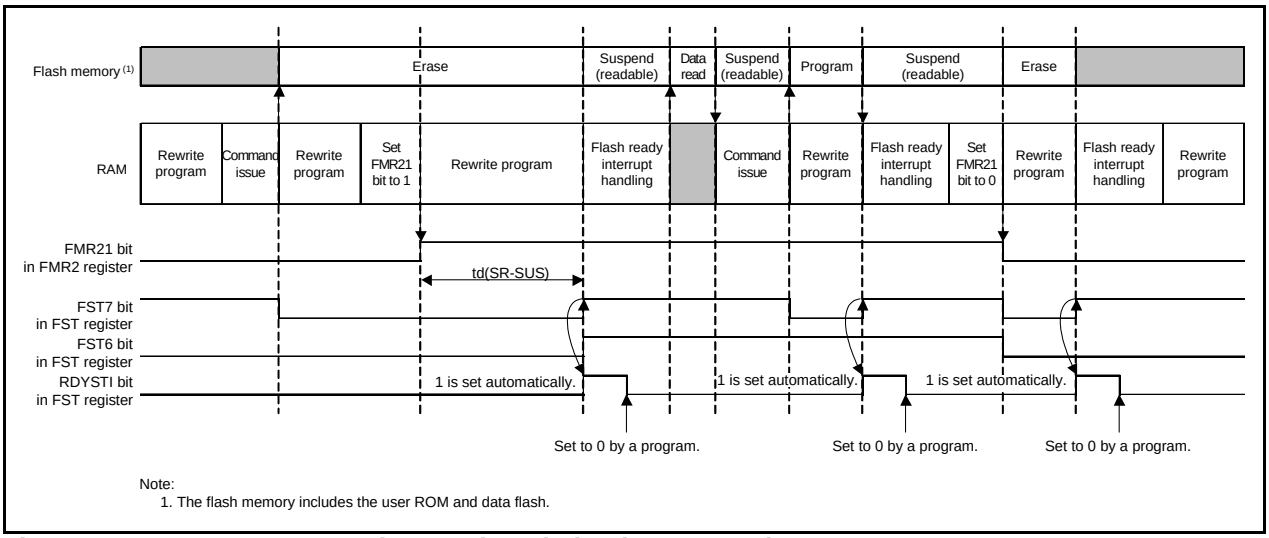
- To check the program-suspend, verify the FST7 bit is set to 1 (ready), then verify the FST3 bit is set to 1 (during program-suspend) to confirm whether programming has been suspended. (When the FST3 bit is set to 0 (other than program-suspend), programming completes.)
- To check the erase-suspend, verify the FST7 bit is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) to confirm whether erasure has been suspended. (When the FST6 bit is set to 0 (other than erase-suspend), erasure completes.)

Figure 29.3 shows the Erase-Suspend Operation Timing in EW0 Mode.

Table 29.4 Executable Operation during Suspend

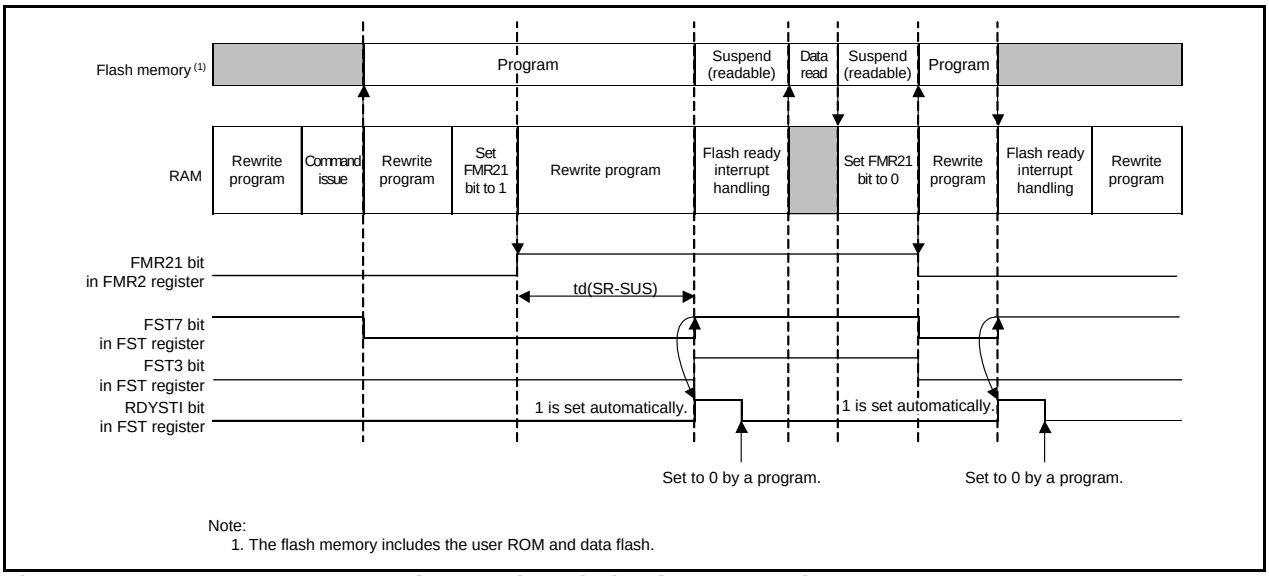
		Operation during Suspend											
		Data flash (Block during erasure execution before entering suspend)			Data flash (Block during no erasure execution before entering suspend)			Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read	Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Data flash	D	D	D	D	E	E	N/A	N/A	N/A	D	E	E
	Program ROM	N/A	N/A	N/A	D	E	E	D	D	D	D	E	E
Areas during program execution before entering suspend	Data flash	D	D	D	D	D	E	N/A	N/A	N/A	D	D	E
	Program ROM	N/A	N/A	N/A	D	D	E	D	D	D	D	D	E

Notes:
1. E indicates operation is enabled by using the suspend function, D indicates operation is disabled, and N/A indicates no combination is available.
2. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The operation of block blank check is disabled during suspend.
3. The MCU enters read array mode immediately after entering suspend.



Note:
1. The flash memory includes the user ROM and data flash.

Figure 29.3 Erase-Suspend Operation Timing in EW0 Mode



Note:
1. The flash memory includes the user ROM and data flash.

Figure 29.4 Program-Suspend Operation Timing in EW0 Mode

29.4.8 How to Set and Exit Each Mode

Figure 29.5 shows How to Set and Exit EW0 Mode and Figure 29.6 shows How to Set and Exit EW1 Mode (When Rewriting Data Flash) and EW1 Mode.

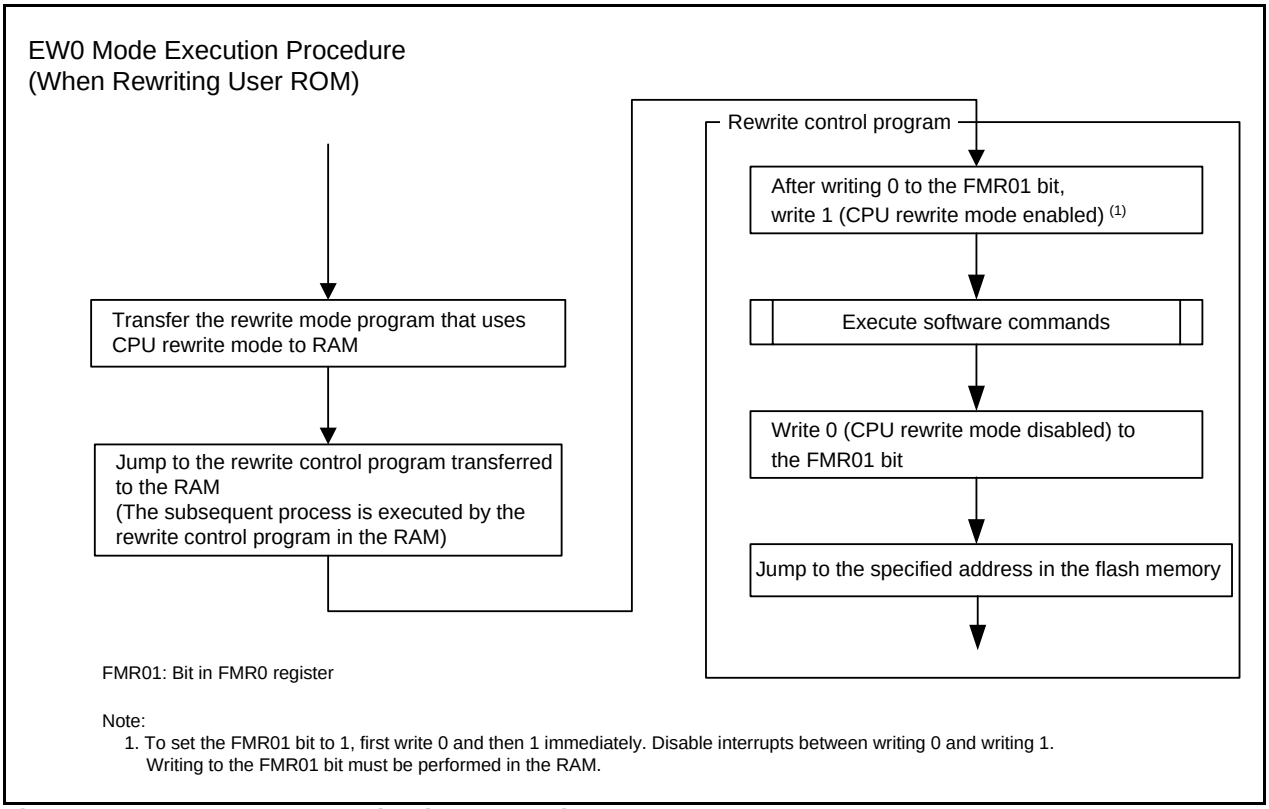

EW0 Mode Execution Procedure
(When Rewriting User ROM)
Transfer the rewrite mode program that uses CPU rewrite mode to RAM
Jump to the rewrite control program transferred to the RAM
(The subsequent process is executed by the rewrite control program in the RAM)
Rewrite control program
After writing 0 to the FMR01 bit, write 1 (CPU rewrite mode enabled) (1)
Execute software commands
Write 0 (CPU rewrite mode disabled) to the FMR01 bit
Jump to the specified address in the flash memory
FMR01: Bit in FMR0 register
Note:
1. To set the FMR01 bit to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1. Writing to the FMR01 bit must be performed in the RAM.

Figure 29.5 How to Set and Exit EW0 Mode

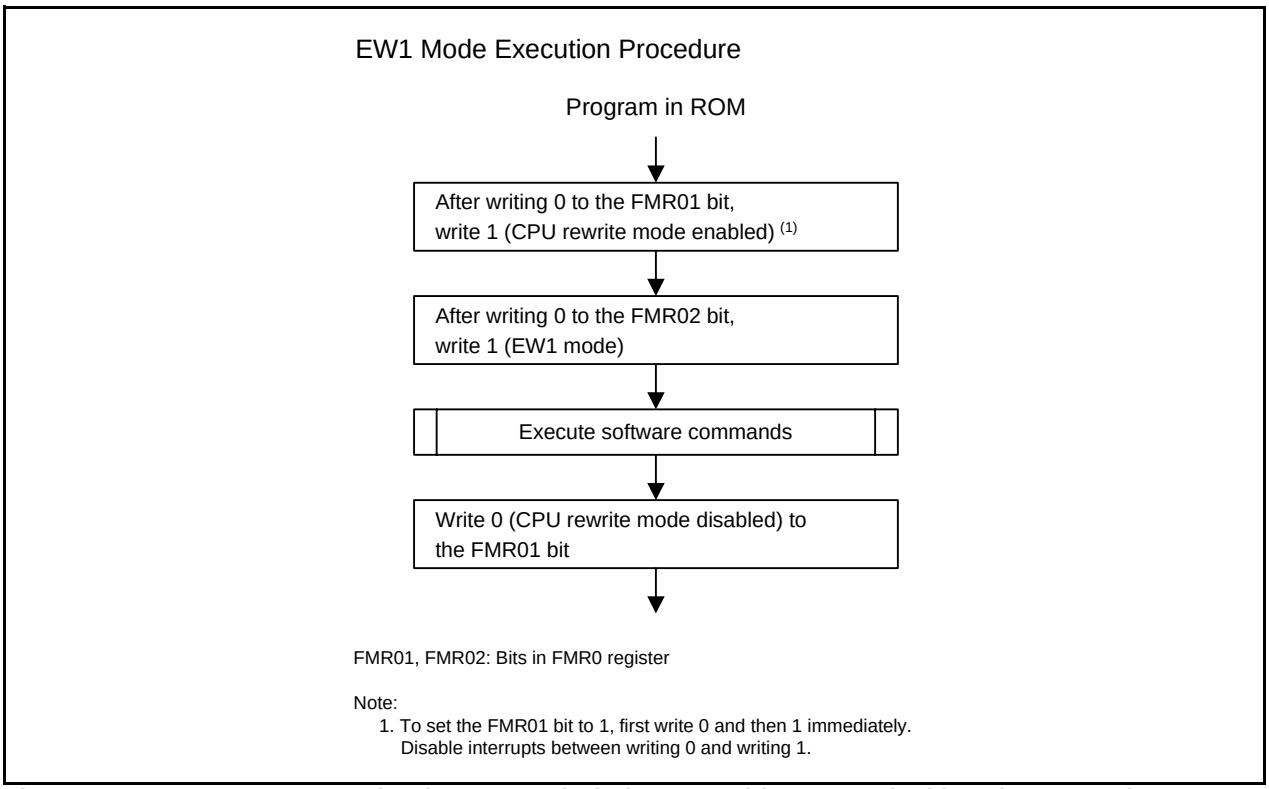

EW1 Mode Execution Procedure
Program in ROM
After writing 0 to the FMR01 bit, write 1 (CPU rewrite mode enabled) (1)
After writing 0 to the FMR02 bit, write 1 (EW1 mode)
Execute software commands
Write 0 (CPU rewrite mode disabled) to the FMR01 bit
FMR01, FMR02: Bits in FMR0 register
Note:
1. To set the FMR01 bit to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.

Figure 29.6 How to Set and Exit EW1 Mode (When Rewriting Data Flash) and EW1 Mode

29.4.9 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register is set to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. A block status changes according to the lock bit as follows:

- When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
- When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. No commands can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and all blocks are not locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).
When the block erase command is executed while the FMR13 bit is set to 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after auto-erasure completes.
Refer to **29.4.10 Software Commands** for the details of individual commands.
The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR 13 bit to 1 again and execute the block erase or program command.

- If the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready).
- If a command sequence error occurs.
- If the FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
- If the FMSTP bit in the FM0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

Figure 29.7 shows the FMR13 Bit Operation Timing.

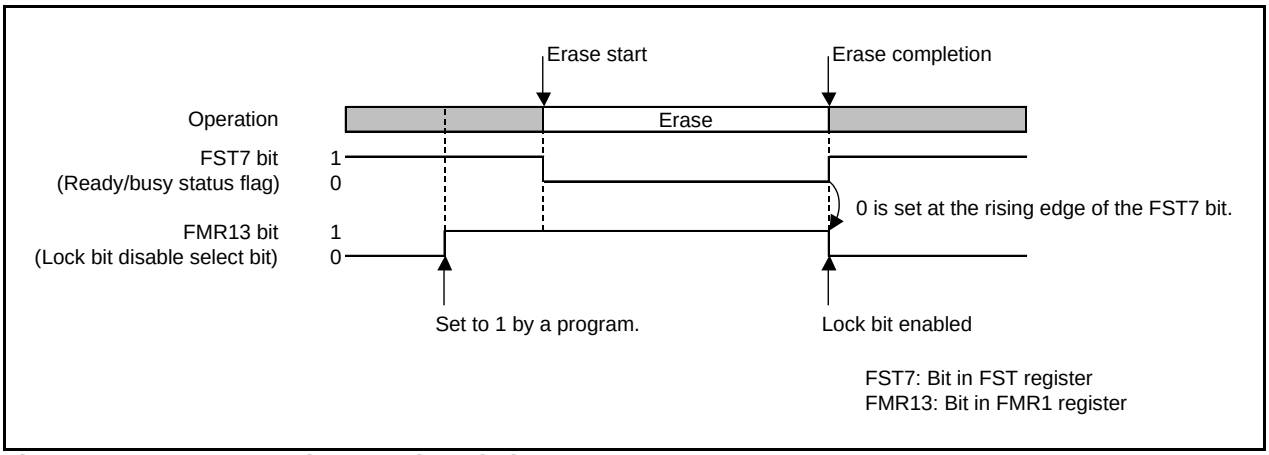


Figure 29.7 FMR13 Bit Operation Timing

29.4.10 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units.

Table 29.5 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	×	FFh			
Clear status register	Write	×	50h			
Program (byte units)	Write	WA	40h	Write	WA	WD
Block erase	Write	×	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	×	71h	Write	BT	D0h
Block blank check	Write	×	25h	Write	BA	D0h

WA: Write address (specify the even address to program in word units.)
WD: Write data
BA: Any block address
BT: Starting block address
×: Any address in the user ROM area

29.4.10.1 Read Array Command

The read array command is used to read the flash memory.
When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since read array mode remains until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, block blank check, read lock bit status, or clear status register command, or after entering erase-suspend.

29.4.10.2 Clear Status Register Command

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register are set to 0.

29.4.10.3 Program Command

The program command is used to write data to the flash memory in 1-byte.
When 40h is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (refer to **29.4.11 Full Status Check**).
Do not write additions to the already programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).

Figure 29.8 shows a Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 29.9 shows a Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled).

In EW1 mode, do not execute this command to any address where a rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. If the FMR21 bit changes to 1 (suspend request) while the RDYSTIE bit is 1 and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when auto-programming suspends. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

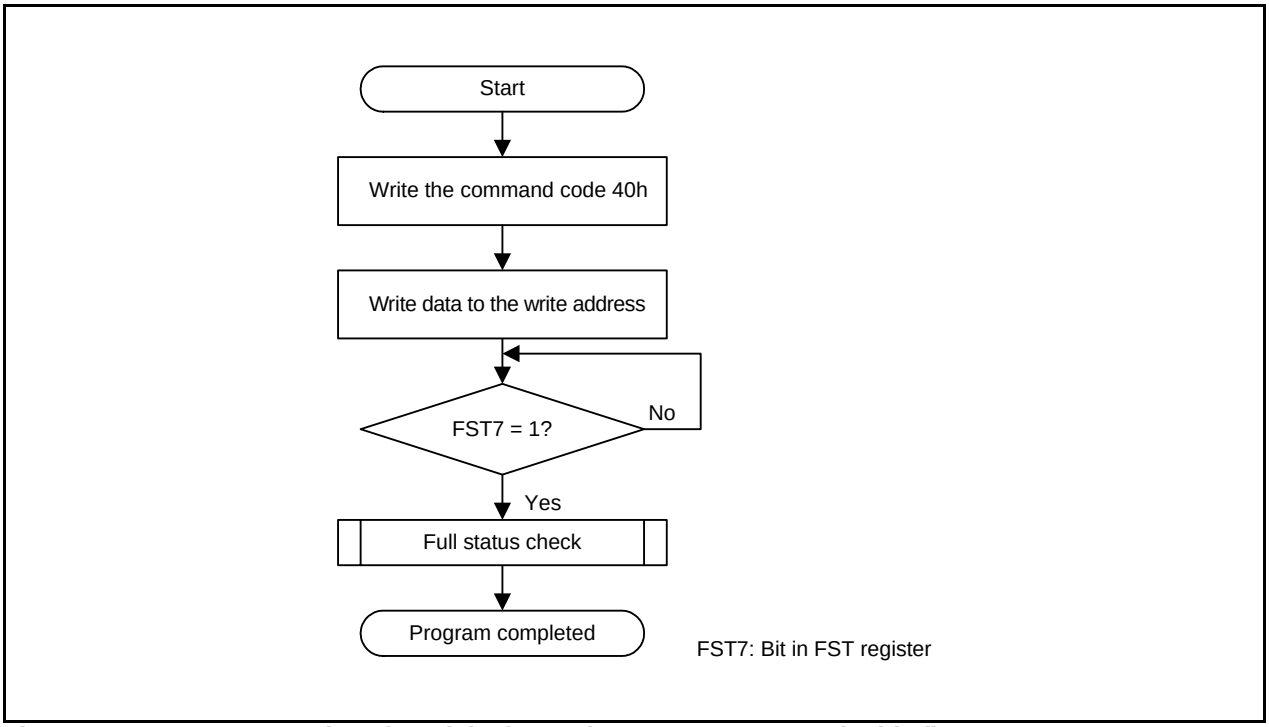
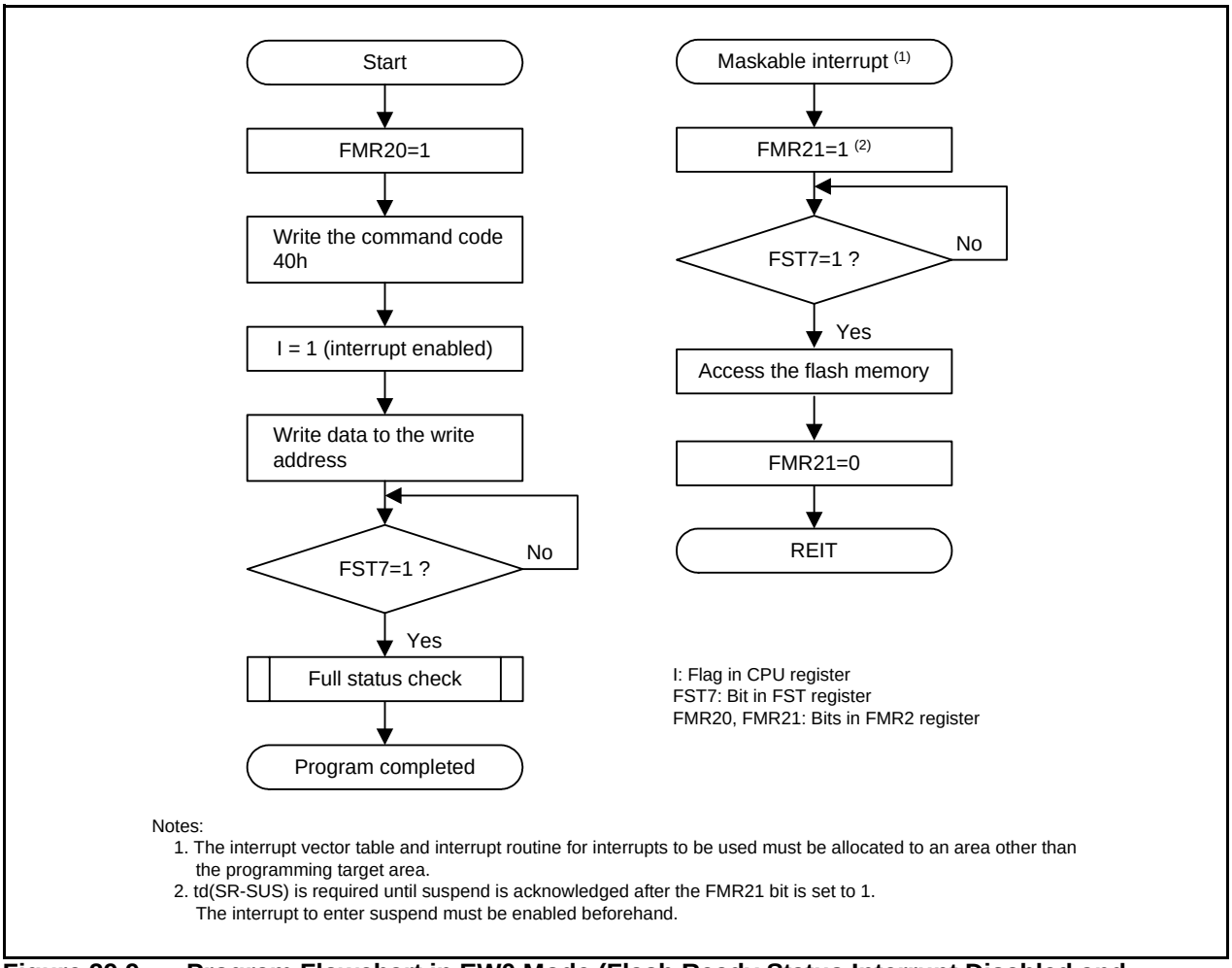
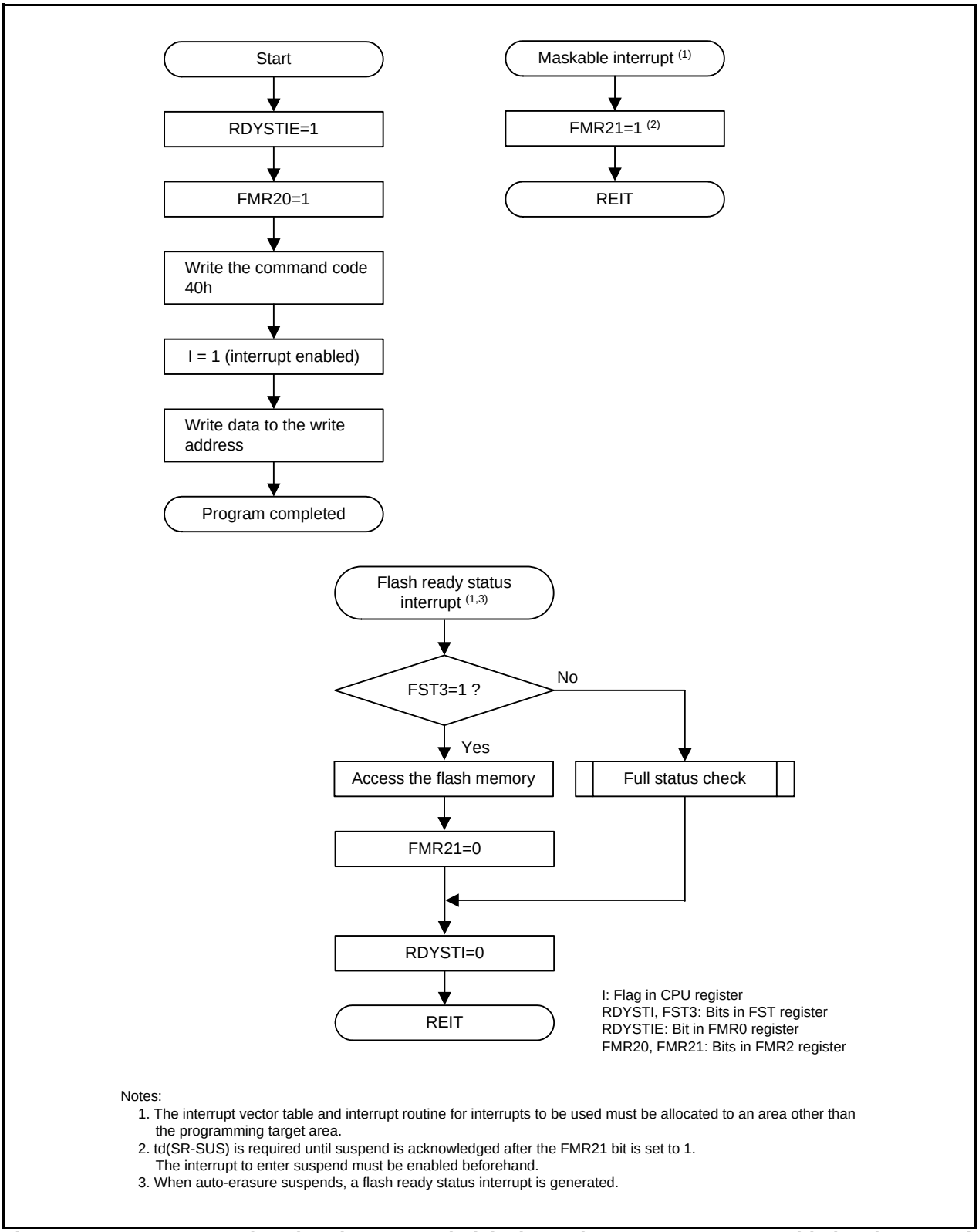


Figure 29.8 Program Flowchart (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1. The interrupt to enter suspend must be enabled beforehand.

Figure 29.9 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1. The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 29.10 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR 22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when suspend is used while the user ROM area is rewritten in EW1 mode.

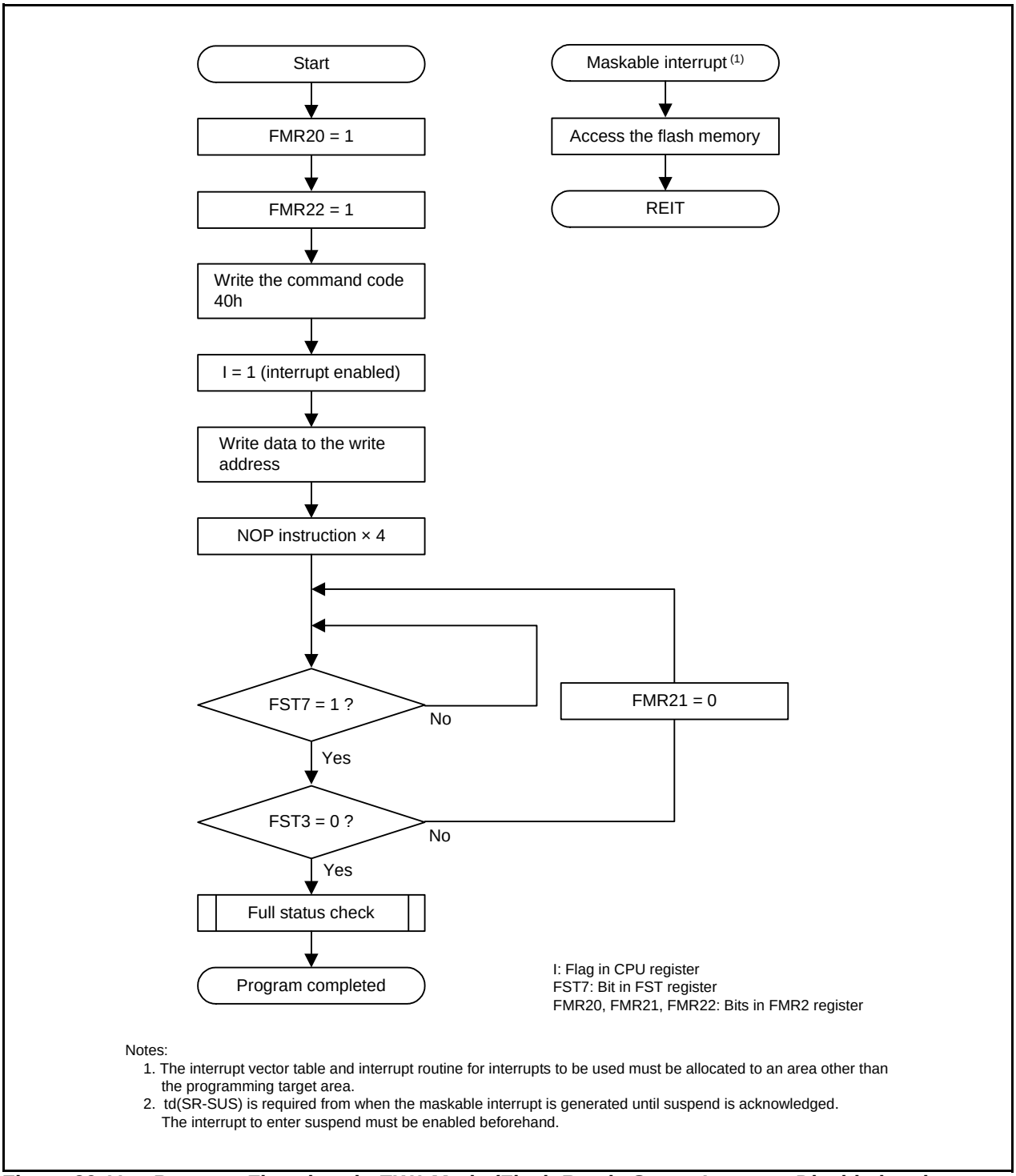

Start
FMR20 = 1
FMR22 = 1
Write the command code 40h
I = 1 (interrupt enabled)
Write data to the write address
NOP instruction × 4
FST7 = 1 ?
No
Yes
FST3 = 0 ?
No
Yes
Full status check
Program completed
Maskable interrupt (1)
Access the flash memory
REIT
FMR21 = 0
I: Flag in CPU register
FST7: Bit in FST register
FMR20, FMR21, FMR22: Bits in FMR2 register
Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the maskable interrupt is generated until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.

Figure 29.11 Program Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

29.4.10.4 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any block address, auto-erasure (erase and erase verify operation) starts in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes. After auto-erasure completes, all data in the block is set to FFh.
After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register. (Refer to **29.4.11 Full Status Check**).

The block erase command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).

Figure 29.12 shows the Block Erase Flowchart (Flash Ready Status Interrupt Disabled), Figure 29.13 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled), and Figure 29.14 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled).

In EW1 mode, do not execute this command to any block where a rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. If the FMR21 bit changes to 1 (suspend request) while the RDYSTIE bit is 1 and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

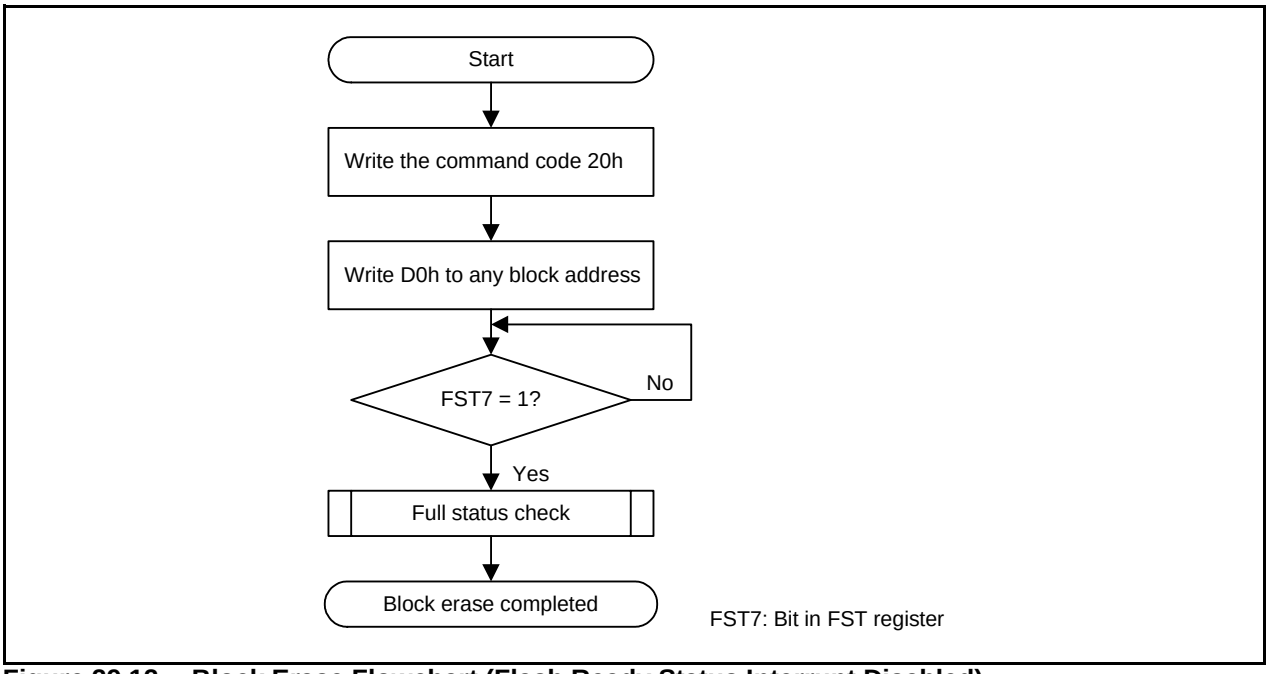
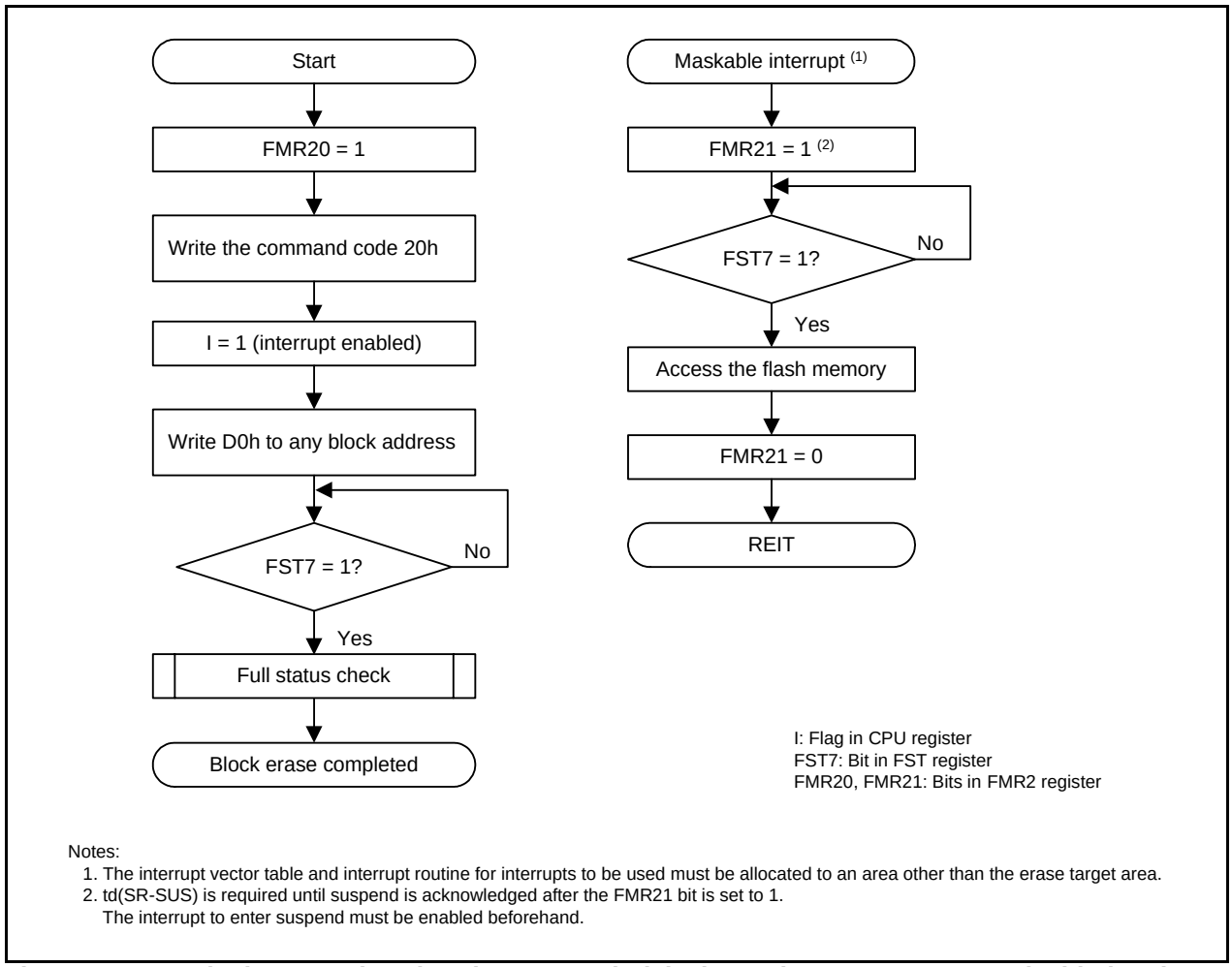
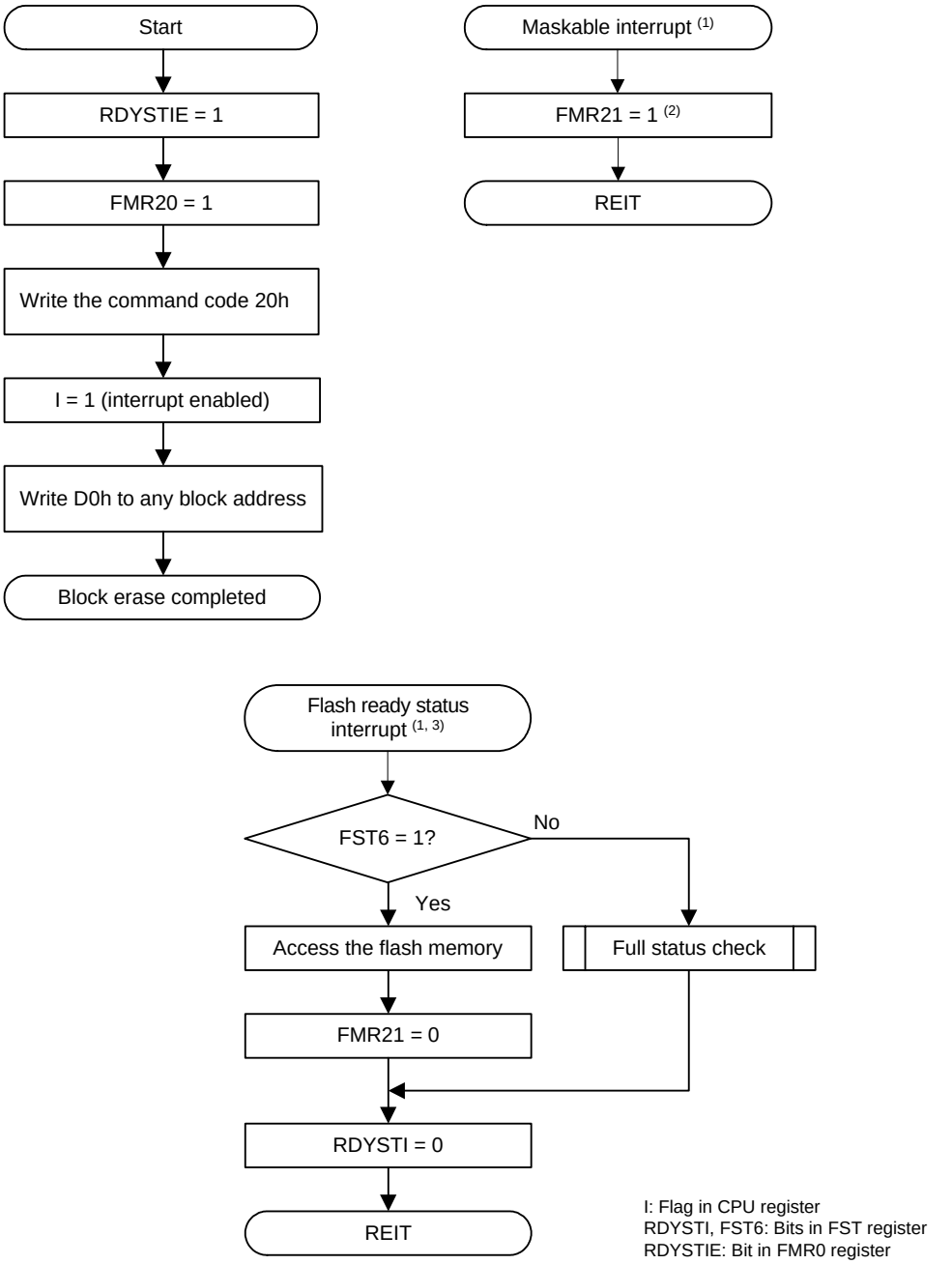


Figure 29.12 Block Erase Flowchart (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.

Figure 29.13 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 29.14 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR 22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when suspend is used while the user ROM area is rewritten in EW1 mode.

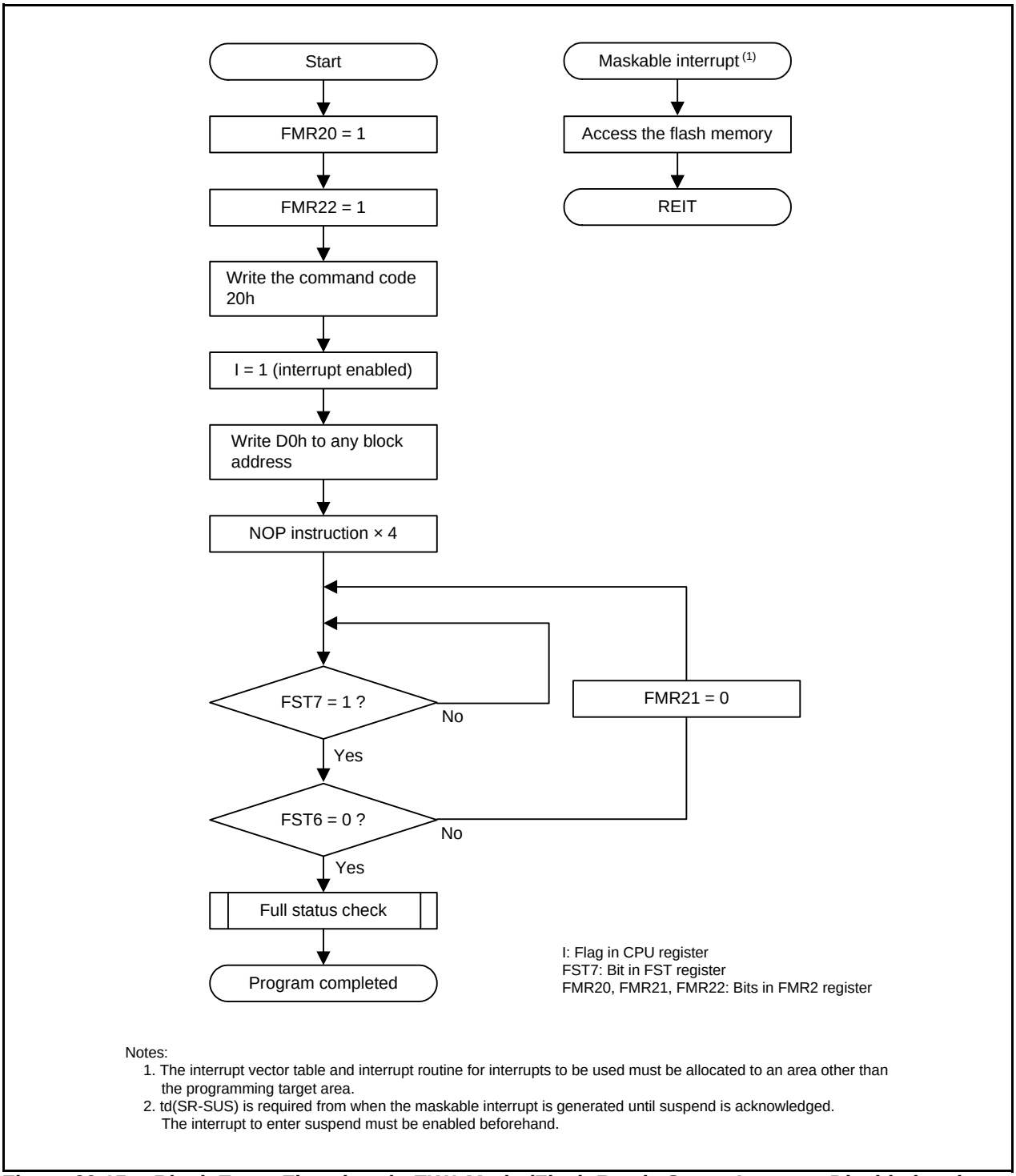

Start
FMR20 = 1
FMR22 = 1
Write the command code 20h
I = 1 (interrupt enabled)
Write D0h to any block address
NOP instruction × 4
FST7 = 1 ?
No
Yes
FST6 = 0 ?
No
Yes
Full status check
Program completed
Maskable interrupt (1)
Access the flash memory
REIT
FMR21 = 0
I: Flag in CPU register
FST7: Bit in FST register
FMR20, FMR21, FMR22: Bits in FMR2 register
Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the maskable interrupt is generated until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.

Figure 29.15 Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

29.4.10.5 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).
When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the starting block address, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the starting block address specified in the second bus cycle.
Figure 29.16 shows the Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.
Refer to **29.4.9 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

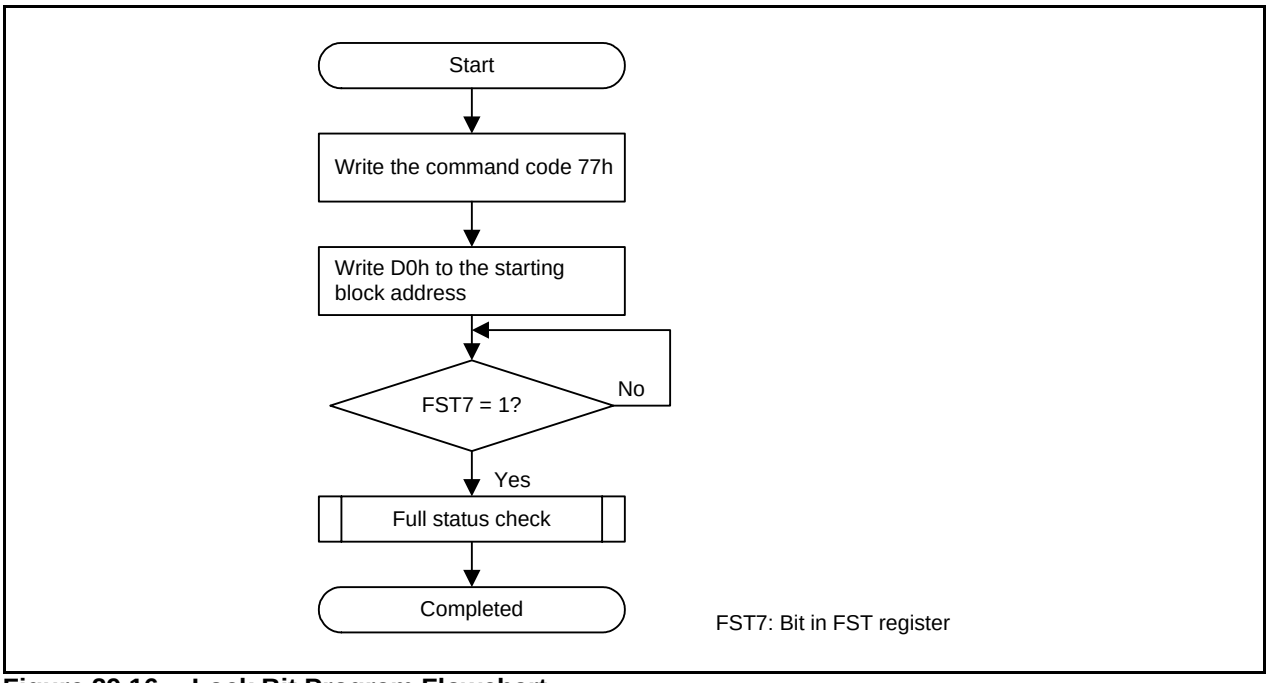


Figure 29.16 Lock Bit Program Flowchart

29.4.10.6 Read Lock Bit Status Command

This command is used to read the lock bit status of any address in the program ROM area.
When 71h written in the first bus cycle and D0h is written in the second cycle to the starting block address, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.
Figure 29.17 shows the Read Lock Bit Status Flowchart.

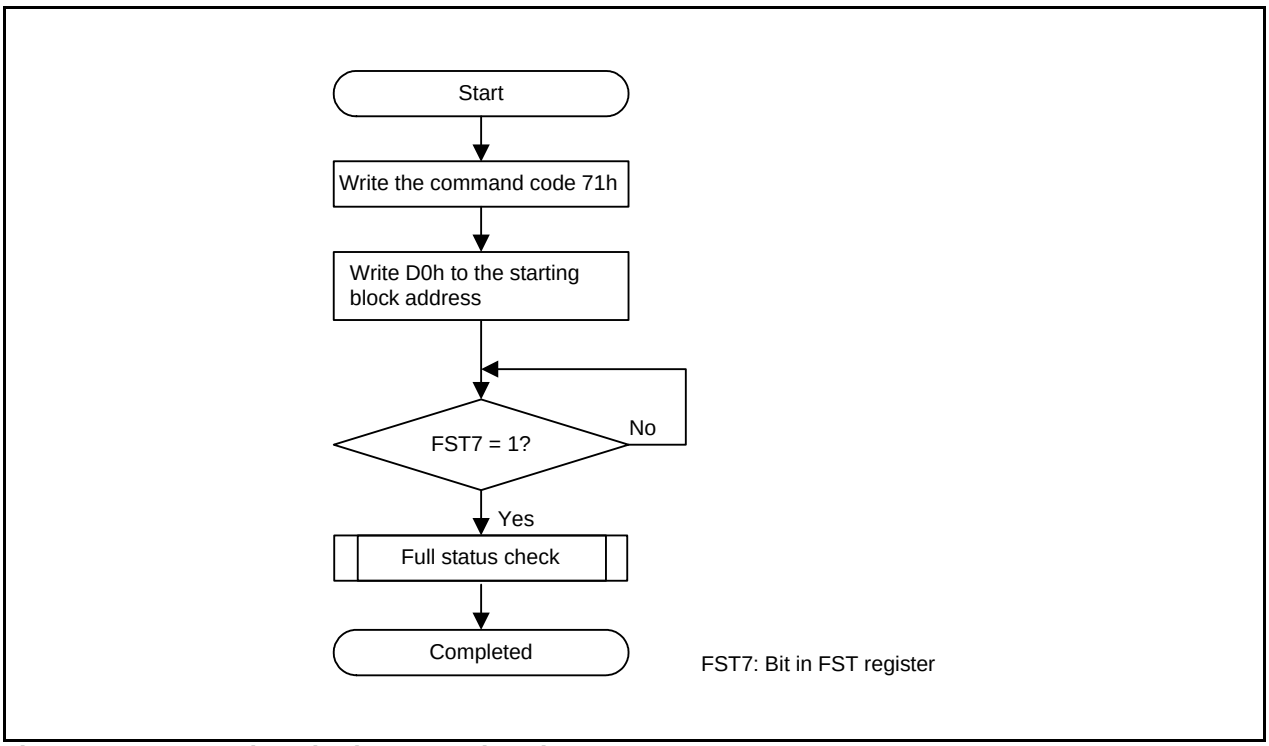


Figure 29.17 Read Lock Bit Status Flowchart

29.4.10.7 Block Blank Check Command

This command is used to confirm that all addresses in any block are blank data FFh.
When 25h is written in the first bus cycle and D0h is written in the second bus cycle to any block address, blank checking starts in the specified block. The FST7 bit in the FST register can be used to confirm whether blank checking has completed. The FST7 bit is set to 0 during the blank-check period and set to 1 when blank checking completes.
After blank checking has completed, the blank-check result can be confirmed by the FST5 bit in the FST register. (Refer to **29.4.11 Full Status Check**.). This command is used to verify the target block has not been written to. To confirm whether erasure has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit is set to 1 (during erase-suspend).
Figure 29.18 shows the Block Blank Check Flowchart.

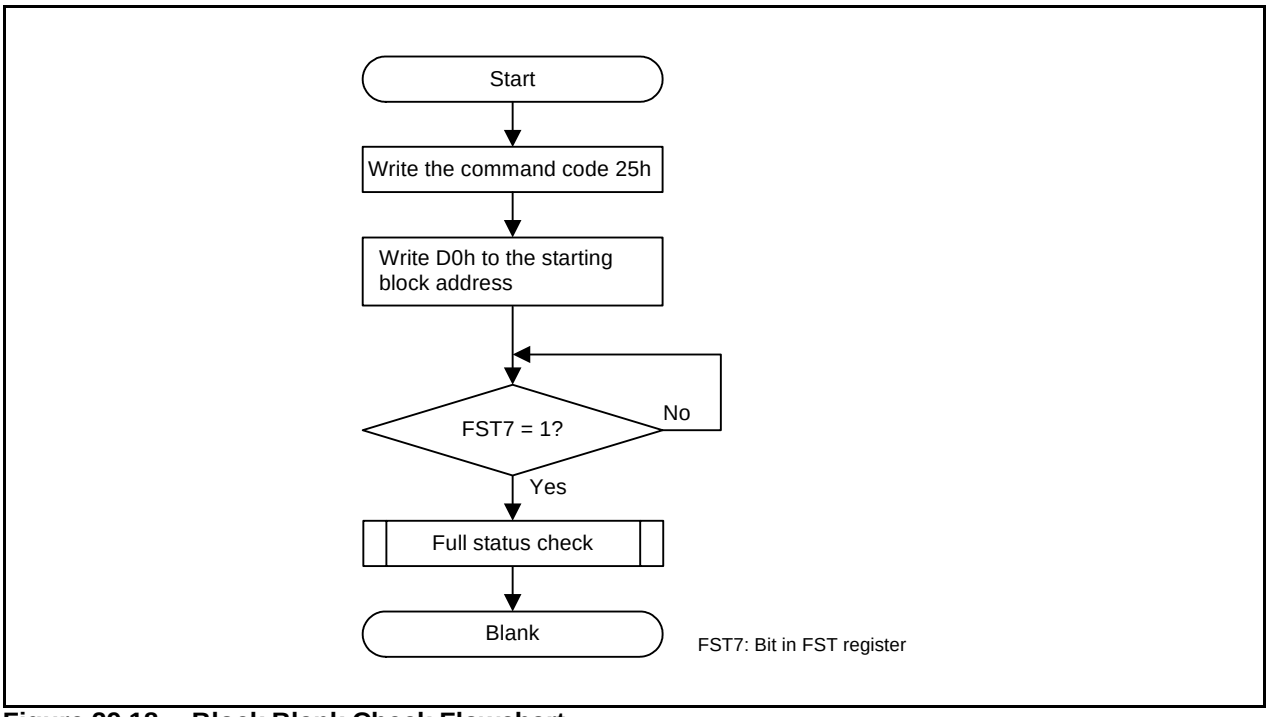


Figure 29.18 Block Blank Check Flowchart

This commanded is intended for programmer manufactures, not for general users.

29.4.11 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).
Table 29.6 lists the Errors and FST Register Status. Figure 29.19 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 29.6 Errors and FST Register Status

FST Register Status		Error	Error Occurrence Condition
FST5	FST4		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command (1). • The erase command is executed during erase-suspend • The program command or erase command is executed during program-suspend • The command is executed to the block during suspend
1	0	Erase error	When the block erase command is executed, but auto-erasure does not complete correctly.
		Blank check error	When the block blank check command is executed and data other than blank data FFh is read.
0	1	Program error/ lock bit program error	When the program command is executed, but auto-programming does not complete correctly.

Note:
1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle is invalid.

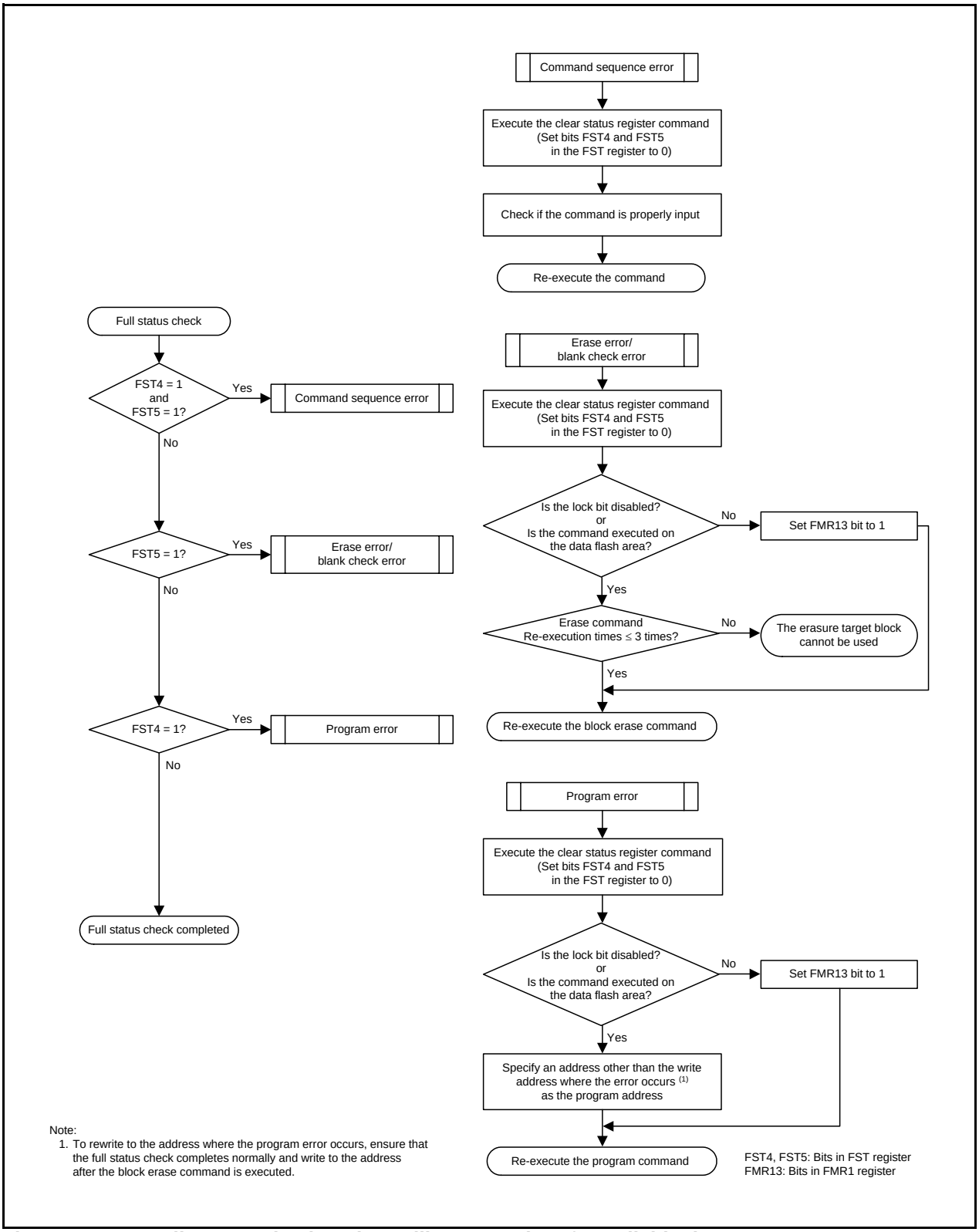

Full status check
FST4 = 1 and FST5 = 1?
Yes
Command sequence error
No
FST5 = 1?
Yes
Erase error/ blank check error
No
FST4 = 1?
Yes
Program error
No
Full status check completed
Command sequence error
Execute the clear status register command (Set bits FST4 and FST5 in the FST register to 0)
Check if the command is properly input
Re-execute the command
Erase error/ blank check error
Execute the clear status register command (Set bits FST4 and FST5 in the FST register to 0)
Is the lock bit disabled? or Is the command executed on the data flash area?
No
Set FMR13 bit to 1
Yes
Erase command Re-execution times ≤ 3 times?
No
The erasure target block cannot be used
Yes
Re-execute the block erase command
Program error
Execute the clear status register command (Set bits FST4 and FST5 in the FST register to 0)
Is the lock bit disabled? or Is the command executed on the data flash area?
No
Set FMR13 bit to 1
Yes
Specify an address other than the write address where the error occurs (1) as the program address
Re-execute the program command
Note:
1. To rewrite to the address where the program error occurs, ensure that the full status check completes normally and write to the address after the block erase command is executed.
FST4, FST5: Bits in FST register
FMR13: Bits in FMR1 register

Figure 29.19 Full Status Check and Handling Procedure for Individual Errors

29.5 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.
There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 .....Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 .....Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 .....Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples with Serial Programmer** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

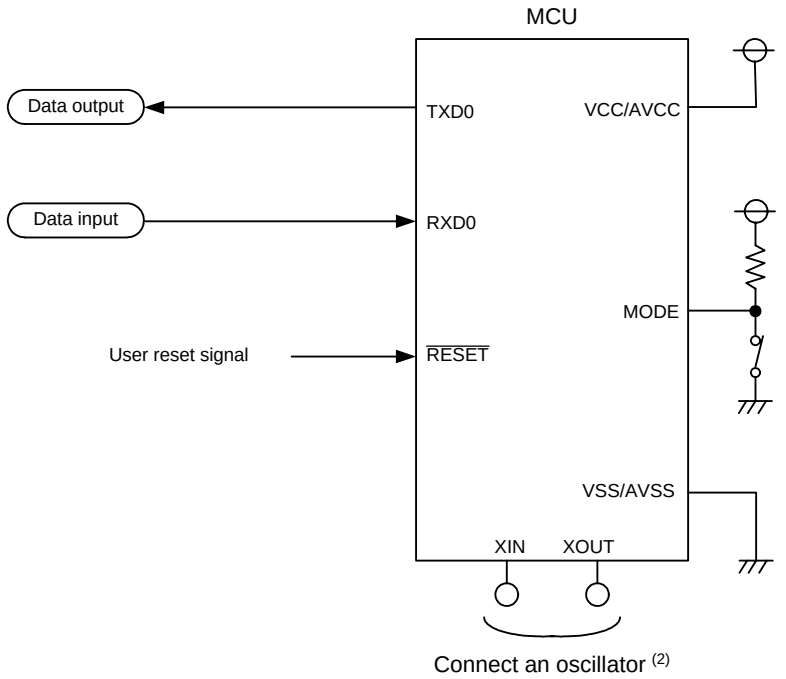
Table 29.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 29.20 shows Pin Handling in Standard Serial I/O Mode 2. Table 29.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 29.21 shows Pin Handling in Standard Serial I/O Mode 3.
After handling the pins shown in Table 29.8 and rewriting the flash memory using the programmer, apply a high-level signal to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

29.5.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **13. ID Code Areas** for details of the ID code check.

Table 29.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P9_0/XIN	P9_0 input/clock input	I	Connect a ceramic resonator or crystal oscillator between pins XIN and XOUT.
P9_1/XOUT	P9_1 input/clock output	I/O	
XCIN	Clock input	I	Connect a crystal oscillator between pins XCIN and XCOUT.
XCOUT	Clock output	I/O	
VREF	Reference voltage	I	Input a high-level signal.
MODE	MODE	I/O	Input a low-level signal.
P8_5	TXD0 output	O	Serial data output pin
P8_6	RXD0 input	I	Serial data input pin
Other I/O port pins		I	Input a high-level signal, output a low-level signal, or leave open.

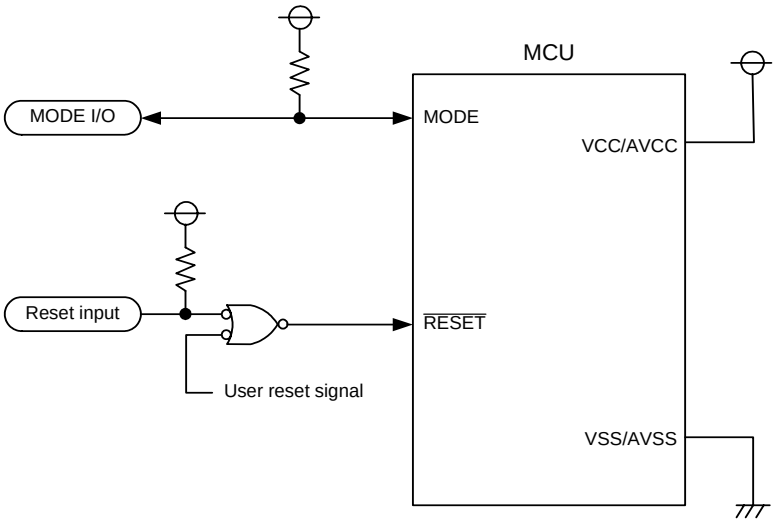


Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Refer to **Appendix 2 Connection Examples with Serial Programmer**.

Figure 29.20 Pin Handling in Standard Serial I/O Mode 2

Table 29.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P9_0/XIN	P9_0 input/clock input	I	If an external oscillator is connected, connect a ceramic resonator or crystal oscillator between pins XIN and XOUT.
P9_1/XOUT	P9_1 input/clock output	I/O	
XCIN	Clock input	I	If an external oscillator is connected, connect a crystal oscillator between pins XCIN and XCOUT.
XCOUT	Clock output	I/O	
VREF	Reference voltage	I	Input a high-level signal.
MODE	MODE	I/O	Serial data I/O pin. Connect the pin to a programmer.
Other I/O port pins		I	Input a high-level signal, output a low-level signal, or leave open.



Notes:
1. Controlled pins and external circuits vary depending on the programmer.
   Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 29.21 Pin Handling in Standard Serial I/O Mode 3

29.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory.
Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.
In parallel I/O mode, the user ROM areas shown in Figure 29.1 can be rewritten.

29.6.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten. (Refer to the **29.3.2 ROM Code Protect Function**.)

29.7 Notes on Flash Memory

29.7.1 CPU Rewrite Mode

29.7.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

29.7.1.2 Interrupts

Tables 29.9 to 29.10 list CPU Rewrite Mode Interrupts (1) and (2), respectively.

Table 29.9 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). If suspend is required while the FMR22 bit is 0 (suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart).
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). If suspend is required while the FMR22 bit is 0 (suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart).
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
EW1	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is acknowledged. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS) and interrupt handling is executed. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)	If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is acknowledged. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS) and interrupt handling is executed. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.

FMR21, FMR22: Bits in FMR2 register

Table 29.10 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step (Note 1)
EW0	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the suspend function.	Do not use during auto-erasure or auto-programming.
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)		
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
EW1	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)		
		During auto-erasure/ programming FMR20=0 (suspend disabled)		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

29.7.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.

- The FMR01 or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20, FMR22, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts between writing 1 and writing 0.

- The FMR14 or FMR15 bit in the FMR1 register

29.7.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

29.7.1.5 Programming

Do not write additions to the already programmed address.

29.7.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
When the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

29.7.1.7 Programming and Erasure Voltage for Flash Memory

To program and erasure program ROM, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

29.7.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

29.7.1.9 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
. The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
. The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.
However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **10.8 Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

30. Electrical Characteristics

30.1 Absolute Maximum Ratings

Table 30.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		P5_4/VL1		–0.3 to VL2 (2)	V
		P5_5/VL2		VL1 to VL3	V
		P5_6/VL3		VL2 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		COM0 to COM3		–0.3 to VL3	V
		SEG0 to SEG39		–0.3 to VL3	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version)/ –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit**.
2. The VL1 voltage should be VCC or below.

30.2 Recommended Operating Conditions

Table 30.2 Recommended Operating Conditions
(Vcc = 1.8 to 5.5 V and Topr = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc/AVcc	Supply voltage					1.8	–	5.5	V
Vss/AVss	Supply voltage					–	0	–	V
VIH	Input “H” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0.8 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.8 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.9 Vcc	–	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	–	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	–	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	–	Vcc	V
VIL	Input “L” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.05 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.35 Vcc	V
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)				–	–	−160	mA
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)				–	–	−80	mA
IOH(peak)	Peak output “H” current	Port P7_0, P7_1, P8 (2)				–	–	−40	mA
		Other pins				–	–	−10	mA
IOH(avg)	Average output “H” current (1)	Port P7_0, P7_1, P8 (2)				–	–	−20	mA
		Other pins				–	–	−5	mA
IOL(sum)	Peak sum output “L” current	Sum of all pins IOL(peak)				–	–	160	mA
IOL(sum)	Average sum output “L” current	Sum of all pins IOL(avg)				–	–	80	mA
IOL(peak)	Peak output “L” current	Port P7_0, P7_1, P8 (2)				–	–	40	mA
		Other pins				–	–	10	mA
IOL(avg)	Average output “L” current (1)	Port P7_0, P7_1, P8 (2)				–	–	20	mA
		Other pins				–	–	5	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	2	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	2	–	8	MHz
f(XCIN)	XCIN oscillation frequency				1.8 V ≤ Vcc ≤ 5.5 V	–	32.768	–	kHz
	XCIN external clock input frequency				1.8 V ≤ Vcc ≤ 5.5 V	–	–	50	kHz
fOCO20M	When used as the count source for timer RC (3)				2.7 V ≤ Vcc ≤ 5.5 V	18.432	–	20	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	-	-	20	MHz
					1.8 V ≤ Vcc < 2.7 V	-	-	8	MHz
–	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	-	-	20	MHz
					1.8 V ≤ Vcc < 2.7 V	-	-	8	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	0	-	20	MHz
					1.8 V ≤ Vcc < 2.7 V	0	-	8	MHz

Notes:
1. The average output current indicates the average value of current measured during 100 ms.
2. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.
3. fOCO20M can be used as the count source for timer RC in the range of Vcc = 2.7 V to 5.5V.

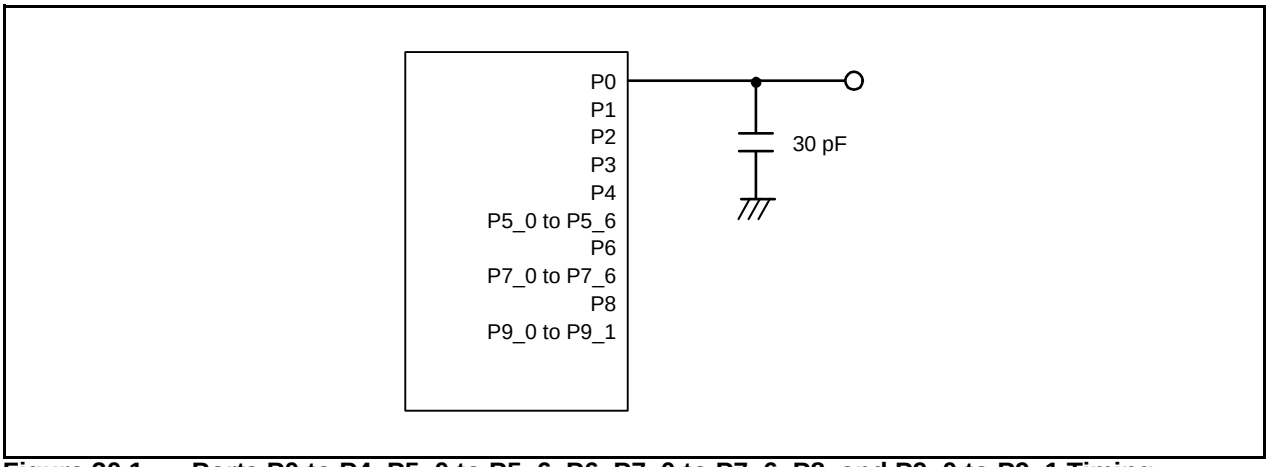


Figure 30.1 Ports P0 to P4, P5_0 to P5_6, P6, P7_0 to P7_6, P8, and P9_0 to P9_1 Timing Measurement Circuit

30.3 Peripheral Function Characteristics

Table 30.3 A/D Converter Characteristics
(Vcc/AVcc = Vref = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVcc		–	–	10	Bit
–	Absolute accuracy (2)	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN11 input	–	–	±3	LSB
			Vref = AVcc = 2.2 V	AN0 to AN11 input	–	–	±5	LSB
			Vref = AVcc = 1.8 V	AN0 to AN11 input	–	–	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN11 input	–	–	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN11 input	–	–	±2	LSB
			Vref = AVcc = 1.8 V	AN0 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	20	MHz
			3.2 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	16	MHz
			2.7 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	10	MHz
			1.8 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	8	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	ms
tSAMP	Sampling time		ϕAD = 20 MHz		0.75	–	–	µs
IVref	Vref current		Vcc = 5 V, XIN = f1 = ϕAD = 20 MHz		-	45	–	µA
Vref	Reference voltage				1.8	–	AVcc	V
VIA	Analog input voltage (3)				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:
1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 30.4 Temperature Sensor Characteristics
(Topr = –20 to 85°C and Vss = 0 V, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
VTMP	Temperature sensor output voltage	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz Topr = 25 °C	–	600	–	mV
–	Temperature coefficient	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz Topr = 25 °C	–	–2.1	–	mV/°C
–	Start-up time	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz	–	–	200	µs
ITMP	Operating current	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz	–	100	–	µA

Table 30.5 Comparator B Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		-0.3	–	V_{CC} + 0.3	V
–	Offset		–	5	100	mV
t_d	Comparator output delay time (1)	V_I = Vref ± 100 mV	–	–	1	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	–	12	–	µA

Note:
1. When the digital filter is disabled.

Table 30.6 Flash Memory (Program ROM) Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time		–	80	–	µs
–	Block erase time		–	0.12	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (6)	Ambient temperature = 85°C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 30.7 Flash Memory (Data flash Block A and Block B) Characteristics (V_{CC} = 1.8 to 5.5 V and T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time (program/erase endurance ≤ 10,000 times)		–	150	–	µs
–	Block erase time (program/erase endurance ≤ 10,000 times)		–	0.05	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		−20 (6)	–	85	°C
–	Data hold time (7)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. −40°C for D version.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

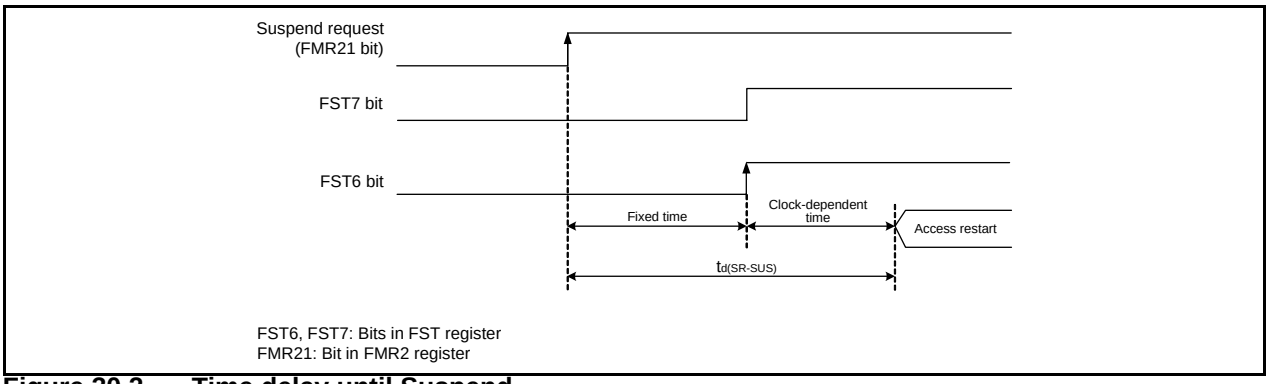


Figure 30.2 Time delay until Suspend

Table 30.8 Voltage Detection 0 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)			1.8	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)			2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)			2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)			3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (3)	In operation	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	50	500	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	100	500	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V		–	1.5	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 30.9 Voltage Detection 1 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	At the falling of Vcc		2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	At the falling of Vcc		2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	At the falling of Vcc		2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	At the falling of Vcc		2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	At the falling of Vcc		2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	At the falling of Vcc		2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	At the falling of Vcc		2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	At the falling of Vcc		3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	At the falling of Vcc		3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	At the falling of Vcc		3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	At the falling of Vcc		3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	At the falling of Vcc		3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	At the falling of Vcc		3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	At the falling of Vcc		3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	At the falling of Vcc		4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	At the falling of Vcc		4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected		–	0.07	–	V
		Vdet1_6 to Vdet1_F selected		–	0.10	–	V
–	Voltage detection 1 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	60	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	250	500	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 30.10 Voltage Detection 2 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

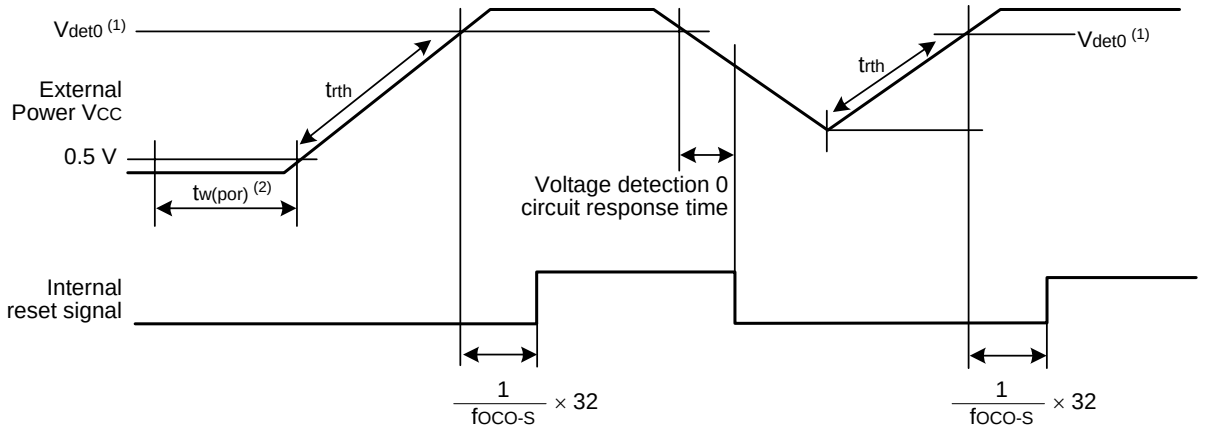
Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0 (1)	At the falling of V_{CC}		3.70	4.0	4.30	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit			–	0.10	–	V
–	Voltage detection 2 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	20	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	200	500	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 30.11 Power-on Reset Circuit Characteristics (1)
(T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		0	–	50,000	mV/msec

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 30.3 Power-on Reset Circuit Characteristics

Table 30.12 High-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	VCC = 1.8 V to 5.5 V – 20°C ≤ Topr ≤ 85°C	19.2	20	20.8	MHz
		VCC = 1.8 V to 5.5 V – 40°C ≤ Topr ≤ 85°C	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (1)	VCC = 1.8 V to 5.5 V – 20°C ≤ Topr ≤ 85°C	17.694	18.432	19.169	MHz
		VCC = 1.8 V to 5.5 V – 40°C ≤ Topr ≤ 85°C	17.510	18.432	19.353	MHz
–	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	–	5	30	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	530	–	µA

Note:
1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 30.13 Low-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	–	30	100	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	2	–	µA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
–	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	–	30	100	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	2	–	µA

Table 30.14 Power Supply Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on (1)		–	–	2000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 30.15 LCD Drive Control Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL3	2.2	–	5.5	V
VL2	VL2 voltage		VL1	–	VL3	V
VL1	VL1 voltage		1	–	VL2 (2)	V
f(FR)	Frame frequency		50	–	180	Hz
ILCD	LCD drive control circuit current		–	(1)	–	µA

Notes:
1. Refer to Table 30.18 DC Characteristics (2), Table 30.20 DC Characteristics (4), and Table 30.22 DC Characteristics (6).
2. The VL1 voltage should be VCC or below.

Table 30.16 Power-Off Mode Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Power-off mode operating supply voltage		1.8	–	5.5	V

30.4 DC Characteristics

Table 30.17 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition			Standard			Unit
						Min.	Typ.	Max.	
VOH	Output “H” voltage		Port P7_0, P7_1, P8 (1)	VCC = 5V	IOH = –20 mA	VCC – 2.0	–	VCC	V
			Other pins	VCC = 5V	IOH = –5 mA	VCC – 2.0	–	VCC	V
VOL	Output “L” voltage		Port P7_0, P7_1, P8 (1)	VCC = 5V	IOL = 20 mA	–	–	2.0	V
			Other pins	VCC = 5V	IOL = 5 mA	–	–	2.0	V
VT+-VT-	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{INT5}$, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO				0.05	0.5	–	V
		$\overline{RESET}$, $\overline{WKUP0}$				0.1	0.8	–	V
IIH	Input “H” current		VI = 5 V, VCC = 5 V			–	–	5.0	µA
IIL	Input “L” current		VI = 0 V, VCC = 5 V			–	–	–5.0	µA
RPULLUP	Pull-up resistance		VI = 0 V, VCC = 5 V			20	40	80	kΩ
RfXIN	Feedback resistance	XIN				–	2.0	–	MΩ
RfXCIN	Feedback resistance	XCIN				–	14	–	MΩ
VRAM	RAM hold voltage		During stop mode			1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 30.18 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition							Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			16 MHz	Off	Off	125 kHz	No division	–		–	3.9	8	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	–	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	3.1	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.5	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	110	320	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	63	220	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	60	220	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	46	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.8	33	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	4.6	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	2.4	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.03	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	2	6.4	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2.7	–	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 30.19 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P7_0, P7_1, P8 (1)	I_{OH} = –5 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P7_0, P7_1, P8 (1)	I_{OL} = 5 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V		–	–	–5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V		25	80	140	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 30.20 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	6	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	2.9	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	10 MHz	125 kHz	No division	–		–	2.9	–	mA
			Off	Off	10 MHz	125 kHz	Divide-by-8	–		–	1.5	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	54	200	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	36	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	3.1	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	1.7	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.02	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.5	4.5	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2.2	–	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 3.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 30.21 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P7_0, P7_1, P8 (1)	I_{OH} = –2 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P7_0, P7_1, P8 (1)	I_{OL} = 2 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 1.8 V, V_{CC} = 1.8 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 1.8 V		–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 1.8 V		85	220	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 30.22 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition							Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	8 MHz	Off	Off	125 kHz	No division	–		–	2.1	–	mA
			8 MHz	Off	Off	125 kHz	Divide-by-8	–		–	0.9	–	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	–		–	1.8	5	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	–		–	1.1	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	54	200	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	36	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	2.4	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	1.7	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.02	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.2	4	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2	–	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 2.2 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open.The standard value does not include the current that flows through external division resistors.

30.5 AC Characteristics

Table 30.23 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	-	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1t_{CYC} + 20	ns
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

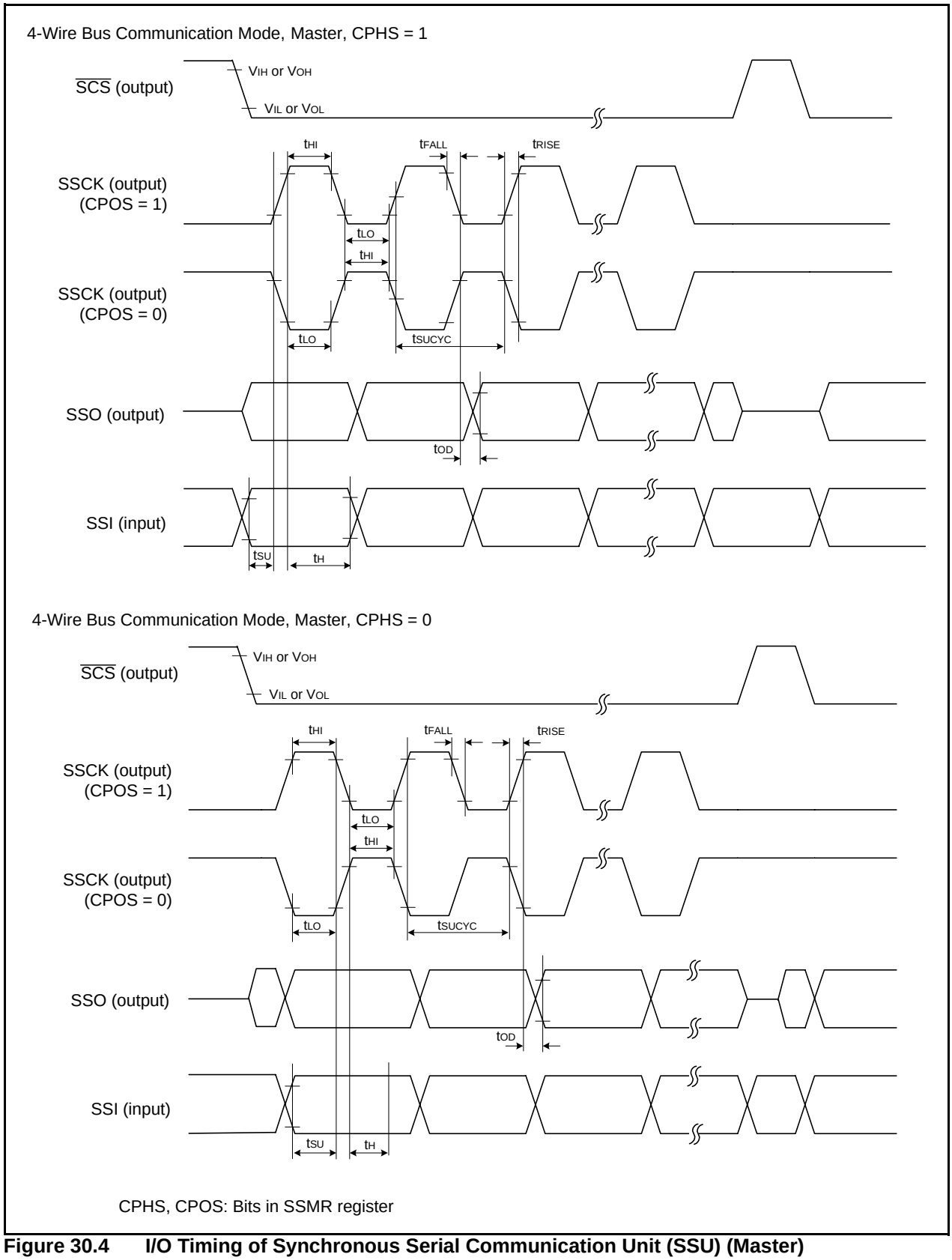


Figure 30.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

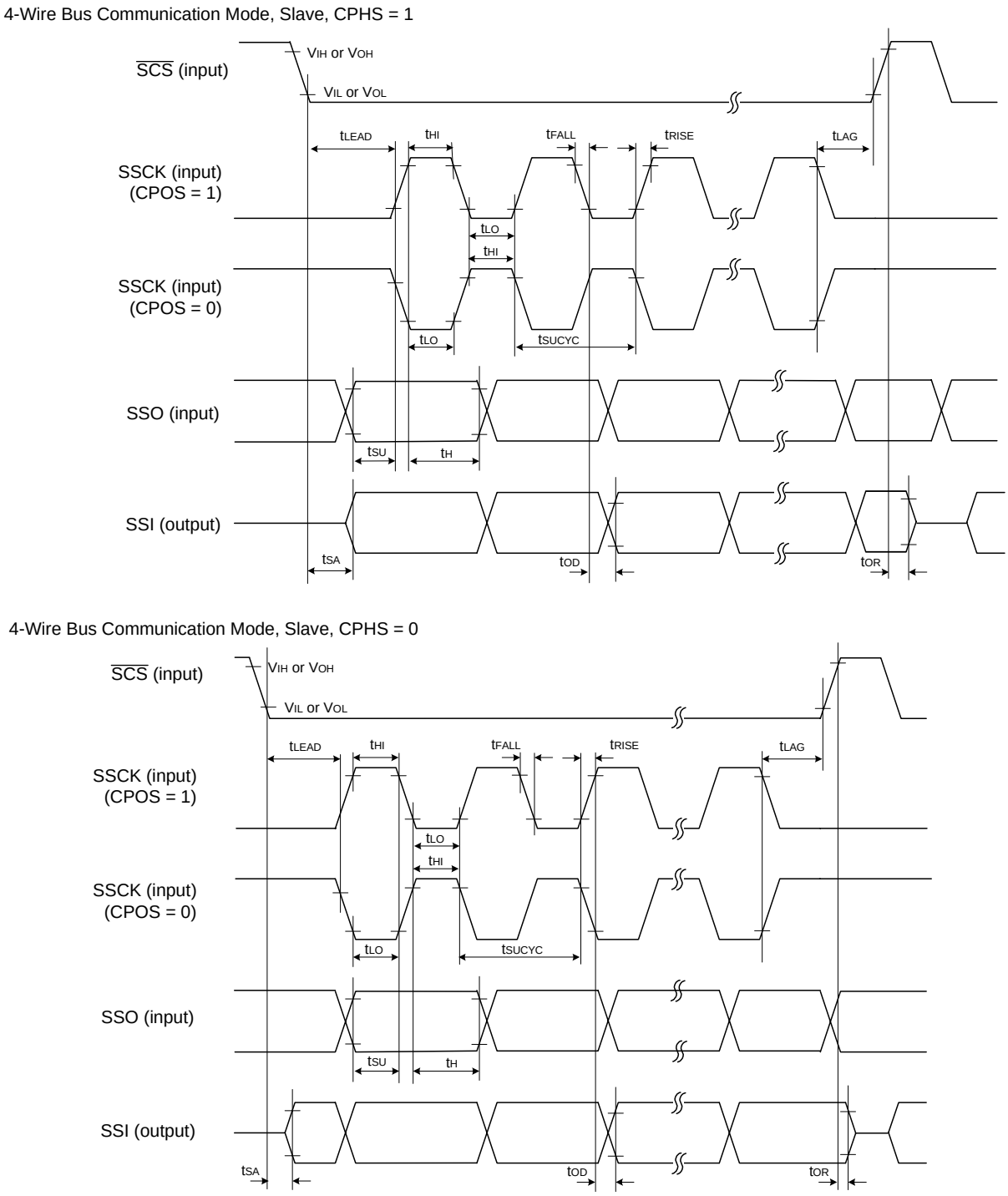


Figure 30.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

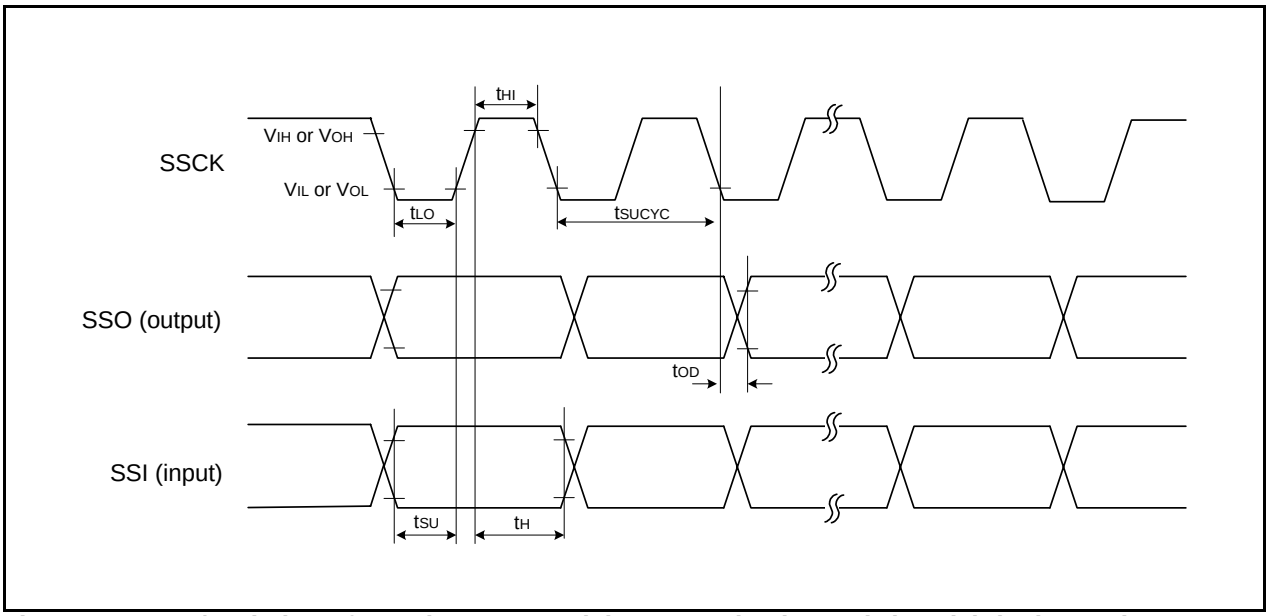
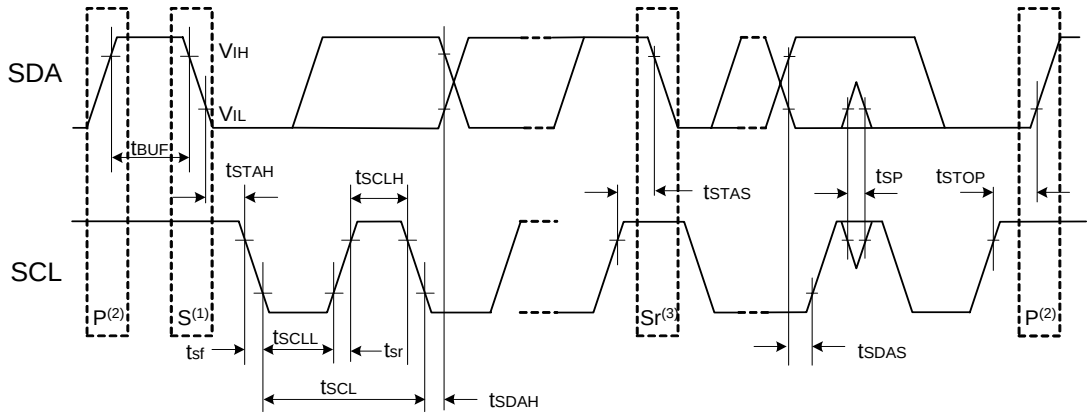


Figure 30.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 30.24 Timing Requirements of I²C bus Interface (1)
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tCYC + 600 (1)	–	–	ns
tSCLH	SCL input “H” width		3tCYC + 300 (1)	–	–	ns
tSCLL	SCL input “L” width		5tCYC + 500 (1)	–	–	ns
tsf	SCL, SDA input fall time		–	–	300	ns
tSP	SCL, SDA input spike pulse rejection time		–	–	1tCYC (1)	ns
tBUF	SDA input bus-free time		5tCYC (1)	–	–	ns
tSTAH	Start condition input hold time		3tCYC (1)	–	–	ns
tSTAS	Retransmit start condition input setup time		3tCYC (1)	–	–	ns
tSTOP	Stop condition input setup time		3tCYC (1)	–	–	ns
tSDAS	Data input setup time		1tCYC + 40 (1)	–	–	ns
tSDAH	Data input hold time		10	–	–	ns

Note:
1. 1tCYC = 1/f1(s)



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 30.7 I/O Timing of I²C bus Interface

Table 30.25 External Clock Input (XIN, XCIN)
(Vss = 0 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	50	–	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	24	–	24	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	24	–	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	20	–	20	–	20	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	10	–	10	–	10	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	10	–	10	–	10	–	µs

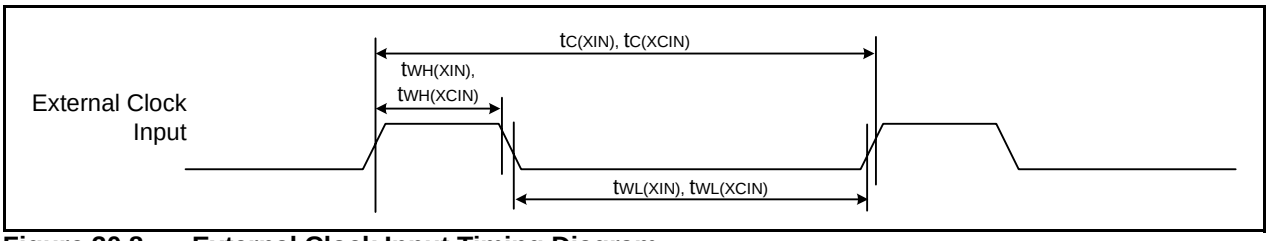


Figure 30.8 External Clock Input Timing Diagram

Table 30.26 Timing Requirements of TRJiIO (i = 0 to 2)
(Vss = 0 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJiIO input cycle time	500	–	300	–	100	–	ns
$t_{WH(TRJIO)}$	TRJiIO input “H” width	200	–	120	–	40	–	ns
$t_{WL(TRJIO)}$	TRJiIO input “L” width	200	–	120	–	40	–	ns

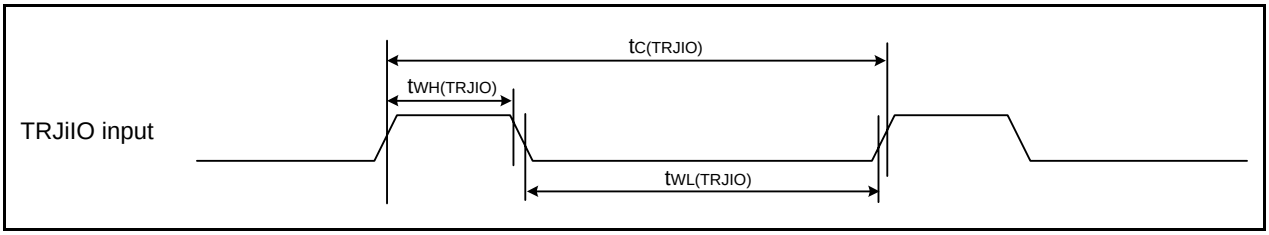


Figure 30.9 Input Timing of TRJiIO

Table 30.27 Timing Requirements of Serial Interface
(Vss = 0 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	300	–	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	150	–	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	150	–	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	–	80	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	0	–	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	70	–	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	90	–	90	–	ns

i = 0, 2

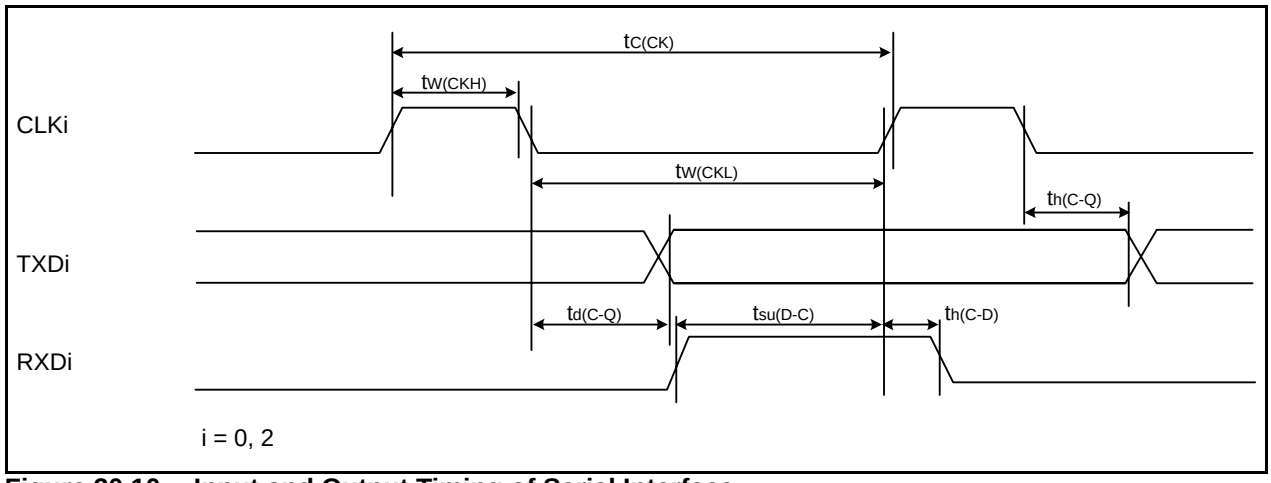


Figure 30.10 Input and Output Timing of Serial Interface

Table 30.28 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 7) and Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)
(Vss = 0 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	–	380 (1)	–	250 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	–	380 (2)	–	250 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

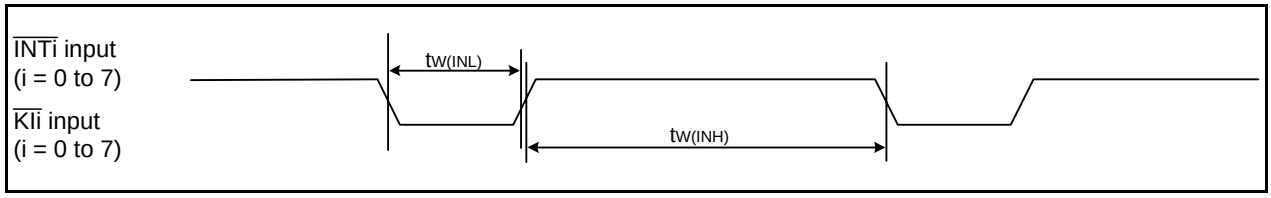


Figure 30.11 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$

31. Usage Notes

31.1 Notes on Clock Generation Circuit

31.1.1 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b.

31.1.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

31.1.3 XCIN Clock

To use the XCIN clock, set the CM03 bit to 1 once and then set it to 0 (XCIN clock oscillates).

31.2 Notes on Power Control

31.2.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) first and then set the CM00 bit in the CM0 register to 0 and the CM10 bit in the CM1 register to 1. An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0,PRCR      ; Writing to registers CM0 and CM1 enabled
        FSET    I           ; Interrupt enabled
        BLCR    0,CM0       ; Stop mode selected
        BSET    0,CM1       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

31.2.2 Wait Mode

To enter wait mode by setting the CM30 bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        FSET    I           ; Interrupt enabled
        WAIT                ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

- Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM3 register enabled
        FCLR    I           ; Interrupt disabled
        BSET    0, CM3      ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR     ; Writing to CM3 register disabled
        FSET    I           ; Interrupt enabled
```

31.2.3 Power-Off 0 Mode

To enter power-off mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then access the POMCR0 register. A period of a few microseconds is required between accessing the POMCR0 register and entering power-off 0 mode. As the CPU continues to operate during this period, insert the NOP and the WAIT instructions to stop the program.

• Program example to enter power-off 0 mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        MOV.B   #02H, POMCR0    ; Fixed value
        MOV.B   #88H, POMCR0    ; Fixed value
        MOV.B   #15H, POMCR0    ; Fixed value
        MOV.B   #92H, POMCR0    ; Fixed value
        MOV.B   #25H, POMCR0    ; Fixed value
        NOP;
        NOP;
        NOP;
        NOP                     ; Enter power-off 0 mode
        WAIT                    ; Wait mode
```

31.2.4 Power-Off 2 Mode

To enter power-off 2 mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) first, and set the CM00 bit in the CM0 register to 1 and bits CM02 to CM01 to 11b, and then set the CM10 bit in the CM1 register to 1. An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter power-off 2 mode

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0,PRCR      ; Writing to registers CM0 and CM1 enabled
        FSET    I           ; Interrupt enabled
        BSET    0,CM0       ; Power-off 2 mode selected
        BSET    1,CM0       ;
        BSET    2,CM0       ;
        BSET    0,CM1       ; Power-off 2 mode
        JMP.B   LABEL_001
LABEL_001
        NOP
        NOP
        NOP
        NOP
```

31.3 Notes on Interrupts

31.3.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

31.3.2 SP Setting

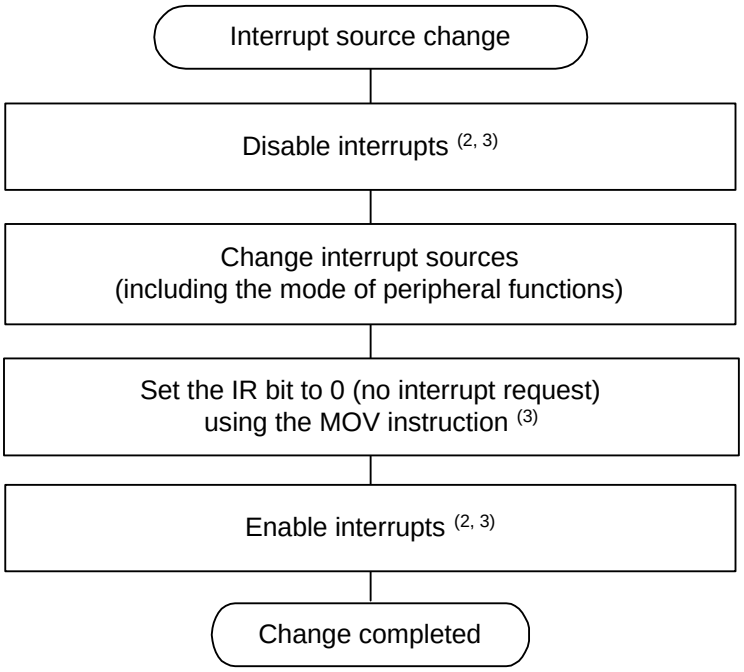
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

31.3.3 External Interrupt, Key Input Interrupt

Either the low-level width or high-level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT7}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$, regardless of the CPU clock.
For details, refer to Table 30.28 **Timing Requirements of External Interrupt $\overline{\text{INTi}}$ (i = 0 to 7) and Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 7)**.

31.3.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 31.1 shows a Procedure Example for Changing Interrupt Sources.


Interrupt source change
Disable interrupts (2, 3)
Change interrupt sources
(including the mode of peripheral functions)
Set the IR bit to 0 (no interrupt request)
using the MOV instruction (3)
Enable interrupts (2, 3)
Change completed

IR bit: Bit in the interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt request). Refer to **12.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 31.1 Procedure Example for Changing Interrupt Sources

31.3.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register:
AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.
Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRJ0IC register to 00h
    POPC    FLG             ; Enable interrupts
```

31.4 Notes on ID Code Areas

31.4.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

31.5 Notes on Option Function Select Area

31.5.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h) ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

31.6 Notes on Timer RB

- Timer RBi stops counting after a reset. Set the values in the timer RBi and timer RBi prescalers before the count starts.
- Even if the prescaler and timer RBi is read out in 16-bit units, these registers are read 1 byte at a time in the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBiCR register to 0 (count stops) or setting the TOSSP bit in the TRBiOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for one or two cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RBi (1) other than the TCSTF bit. Timer RB starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for one or two cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RBi counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RBi (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RBi:
     TRBiCR, TRBiOCR, TRBiIOC, TRBiMR, TRBiPRE, TRBiSC, and TRBiPR

- When the TSTOP bit in the TRBiCR register is set to 1 during timer operation, timer RBi stops immediately.
- When 1 is written to the TOSST or TOSSP bit in the TRBiOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. When 1 is written to the TOSSP bit during the period between when 1 is written to the TOSST bit and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, when 1 is written to the TOSST bit during the period between when 1 is written to the TOSSP bit and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RJi as the count source for timer RB, set timer RJi in timer mode, pulse output mode, or event counter mode.

31.6.1 Timer Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR register (i = 0 or 1) is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

31.6.2 Programmable Waveform Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

31.6.3 Programmable One-Shot Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously during count operation, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously during count operation, allow three or more cycles of the prescaler underflow for each write interval.

31.6.4 Programmable Wait One-shot Generation Mode

To write to registers TRBiPRE and TRBiPR during count operation (TCSTF bit in the TRBiCR (i = 0 or 1) register is set to 1), note the following:

- When the TRBiPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBiPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

31.7 Notes on Timer RC

31.7.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRC register cleared by compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.W   TRC,DATA       ;Read
```

31.7.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA     ;Read
```

31.7.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

31.7.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO20M to another clock, allow two or more cycles of f1 to elapse after changing the clock setting before stopping fOCO20M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for two or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO20M, allow a minimum of one cycle of fOCO-F + fOCO20M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO20M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

31.7.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 18.1 Timer RC Operating Clocks**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 18.5 Block Diagram of Digital Filter**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

31.7.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

31.8 Notes on Timer RH

31.8.1 Reset

A reset input does not reset the timer RH registers that store data of seconds, minutes, hours, days of the week, dates, months, years, 12-hour/24-hour operating mode, a.m./p.m., alarms, interrupts, error correction. This requires the initial setting of all registers after power on.

31.8.2 Starting and Stopping Count

Timer RH uses the RUN bit in the TRHCR register to instruct the count to start or stop.
When the RUN bit is set to 1 (count starts), timer RH starts counting. It takes the time for up to two cycles of the count source until the 15-bit counter starts counting. During this time, do not access registers associated with timer RH (1).
Similarly, when the RUN bit is set to 0 (count stops), timer RH stops counting. It takes the time for up to two cycles of the count source until the 15-bit counter stops counting. During this time, do not access registers associated with timer RH (1).

Note:
1. Registers associated with timer RH: MSTCR1, TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, TRHYR, TRHCR, TRHCSR, TRHADJ, TRHIFR, TRHIER, TRHAMIN, TRHAHR, TRHWK, TRHPRC, and TRHICR

31.8.3 Register Setting

Write to the following registers or bits when the RUN bit in the TRHCR register is set to 0 (count stops).
- Timer TRH data registers (1)
- The TRHIER register
- Bits TRHOE, HR24, PM, and CCLR in the TRHCR register
- Bits CS0 to CS3 and OS0 to OS2 in the TRHCSR register

Set the TRHIER register after setting other registers and bits mentioned above (immediately before timer RH count starts).
Figure 19.5 shows a Setting Example in Real-Time Clock Mode.

Note:
1. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR

31.8.4 Time Reading Procedure in Real-Time Clock Mode

In real-time clock mode, read timer RH data registers (1) and bits HR24 and PM in the TRHCR register when the BSY bit in the TRHSEC is set to 0 (not while data is updated).
When reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.
In order to prevent this, use the reading procedure shown below:

- Using an interrupt
  Read necessary contents of timer RH data registers (1) and bits HR24 and PM in the TRHCR register in the timer RH interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TRHIC register with a program and read necessary contents of timer RH data registers (1) and bits HR24 and PM in the TRHCR register after the IR bit is set to 1 (timer RH interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after it is set to 1 (approximately 15.6 ms while the BSY bit is 1).
(3) Read necessary contents of timer RH data registers (1) and bits HR24 and PM in the TRHCR register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of timer RH data registers (1) and bits HR24 and PM in the TRHCR register
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match the previous contents.

Also, when reading several registers, read them as continuously as possible.

Note:
1. Timer RH data registers: TRHSEC, TRHMIN, TRHHR, TRHWK, TRHDY, TRHMON, and TRHYR

31.9 Notes on Timer RJ

- Timer RJi stops counting after a reset. Set the values in the timer before the count starts.
- Read the timer in 16-bit units.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRJiCR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRJiCR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RJi underflow signal generated after the count starts.
- When using pulse period measurement mode, leave two or more periods of the timer RJi register immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit remains 0 (count stops) for zero or one cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RJi (1) other than the TCSTF bit.
  Timer RJi starts counting at the first active edge of the count source after the TCSTF bit is set to 1 (during count operation).
  The TCSTF bit remains 1 for zero or one cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RJi counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RJi (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RJi: TRJiCR, TRJiIOC, TRJiMR, and TRJi

- When the TRJi register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.

31.10 Notes on Serial Interface (UART0)

- When reading data from the U0RB register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the U0RB register is read, bits PER and FER in the U0RB register and the RI bit in the U0C1 register are set to 0.
  To check receive errors, read the U0RB register and then use the read data.

  Program example to read the receive buffer register:
  ```
  MOV.W    00A6H,R0    ; Read the U0RB register
  ```

- When writing data to the U0TB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:
  ```
  MOV.B    #XXH,00A3H  ; Write to the high-order byte of the U0TB register
  MOV.B    #XXH,00A2H  ; Write to the low-order byte of the U0TB register
  ```

31.11 Notes on Serial Interface (UART2)

31.11.1 Clock Synchronous Serial I/O Mode

31.11.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs a high-level signal when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

31.11.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register is set to 1 (transmission enabled).
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register).
- If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.

31.11.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmission even if the MCU is used for reception only. Dummy data is output from the TXD2 pin during reception.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and setting dummy data in the U2TB register. When an external clock is selected, the shift clock is generated by setting the TE bit to 1 (transmission enabled), setting dummy data in the U2TB register, and inputting an external clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register is set to 1 (reception enabled).
- The TE bit in the U2C1 register is set to 1 (transmission enabled).
- The TI bit in the U2C1 register is set to 0 (data in the U2TB register).

31.11.2 Special Mode 1 (I^2C Mode)

To generate start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than half cycle of the transfer clock before changing each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

31.12 Notes on Synchronous Serial Communication Unit (SSU)

To use the synchronous serial communication unit, set the IICSEL bit in the SSUIICSR register to 0 (SSU function selected).

31.13 Notes on I2C bus Interface

To use the I2C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I2C bus interface function selected).

31.13.1 Master Receive Mode

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

31.13.1.1 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.
Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

31.13.2 The ICE Bit in the ICCR1 Register and the IICRST Bit in the ICCR2 Register

When writing 0 to the ICE bit or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

31.13.2.1 Conditions When Bits Become Undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

31.13.2.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

31.13.2.3 Additional Descriptions Regarding the IICRST Bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.

31.14 Notes on A/D Converter

31.14.1 A/D Converter

- Write to the ADMOD, ADINSEL, ADCON0 (other than the ADST bit), ADCON1, or OCVREFCR register must be performed while A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select fOCO-F as ϕAD.
- Connect 0.1 µF capacitor between pins VREF and AVSS.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) or the FMR27 bit to 1 (low-current-consumption read mode enabled) during A/D conversion. Otherwise, the A/D conversion result will be undefined.
- Do not change the CKS2 bit in the ADMOD register while fOCO-F is stopped.
- During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

31.14.2 Temperature Sensor

- When the ADTSEN bit is set to 1 (operation starts), the temperature sensor starts operation. After the setting to start operation, wait until the voltage stabilizes a maximum of 200 µs before starting A/D conversion.
- The A/D conversion result of the temperature sensor output voltage will include fluctuations in the output voltage and errors in the A/D converter absolute accuracy. This may cause discrepancies in the Temperature Sensor Performance (refer to Table 26.9) or the Temperature Characteristics (Typical Characteristics) of Temperature Sensor Output Voltage (refer to Figure 26.10).
- Depending on the environment surrounding the MCU, the thermal conductivity from the measured object to the temperature sensor circuit varies, affecting the response time and accuracy of the temperature sensor output voltage. Careful evaluation should be performed for the system before use.
- If the temperature sensor output voltage amplified by the gain amplifier exceeds the reference voltage, A/D conversion cannot be performed correctly.
- The temperature sensor output voltage cannot be output from the pins.

31.15 Notes on LCD Drive Control Circuit

31.15.1 When Division Resistors are Connected Externally

The reference values of R1 to R3 are 10 kΩ to 200 kΩ. These reference values depend on the used LCD panel, number of segment and common pins, frame frequency, and environment. Careful evaluation should be performed for the system to determine the values (refer to Figure 28.3).

31.16 Notes on Flash Memory

31.16.1 CPU Rewrite Mode

31.16.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

31.16.1.2 Interrupts

Tables 31.1 to 31.2 list CPU Rewrite Mode Interrupts (1) and (2), respectively.

Table 31.1 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). If suspend is required while the FMR22 bit is 0 (suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart).
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). If suspend is required while the FMR22 bit is 0 (suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart).
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
EW1	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is acknowledged. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS) and interrupt handling is executed. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)	If the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is acknowledged. The flash memory suspends auto-erasure or auto-programming after td(SR-SUS) and interrupt handling is executed. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. While auto-programming is being suspended, any block other than the block during auto-programming execution can be read. Auto-erasure or auto-programming can be restarted by setting the FMR21 bit to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-erasure/ programming FMR20=0 (suspend disabled)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.

FMR21, FMR22: Bits in FMR2 register

Table 31.2 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step (Note 1)
EW0	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the suspend function.	Do not use during auto-erasure or auto-programming.
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)		
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
EW1	Data flash	During auto-erasure/ programming FMR20=1 (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure/ programming FMR20=0 (suspend disabled)		
	Program ROM	During auto-erasure/ programming FMR20=1 (suspend enabled)		
		During auto-erasure/ programming FMR20=0 (suspend disabled)		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

31.16.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts between writing 0 and writing 1.
- The FMR01 or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20, FMR22, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts between writing 1 and writing 0.
- The FMR14 or FMR15 bit in the FMR1 register

31.16.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

31.16.1.5 Programming

Do not write additions to the already programmed address.

31.16.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
When the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

31.16.1.7 Programming and Erasure Voltage for Flash Memory

To program and erasure program ROM, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

31.16.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

31.16.1.9 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
. The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
. The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.
However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **10.8 Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

31.17 Notes on Noise

31.17.1 Inserting Bypass Capacitor between Pins VCC and VSS as Countermeasure against Noise and Latch-up

Connect a bypass capacitor (approximately 0.1 μF) using the shortest and thickest wire possible.

31.17.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

31.18 Note on Supply Voltage Fluctuation

After reset is deasserted, the supply voltage applied to the VCC pin must meet either or both the allowable ripple voltage Vr (vcc) or ripple voltage falling gradient dVr (vcc)/dt shown in Figure 31.2.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr (vcc)	Allowable ripple voltage			0.1 VCC	V
dVr (vcc)/dt	Ripple voltage falling gradient			10	V/ms

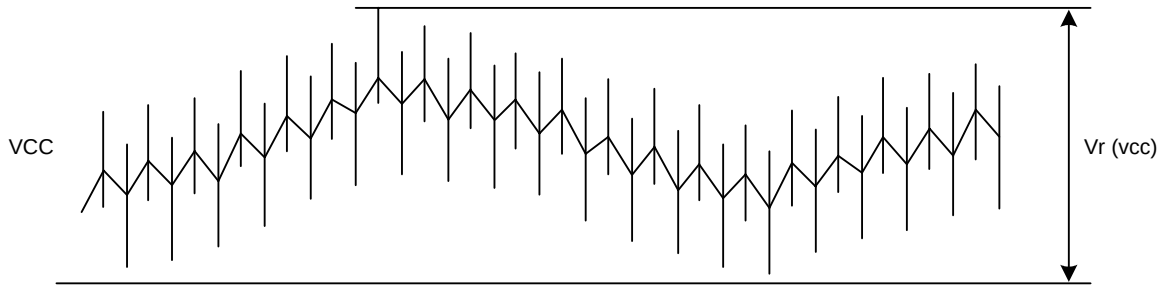


Figure 31.2 Definition of Ripple Voltage

32. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/LA6A Group and R8C/LA8A Group, take note of the following:

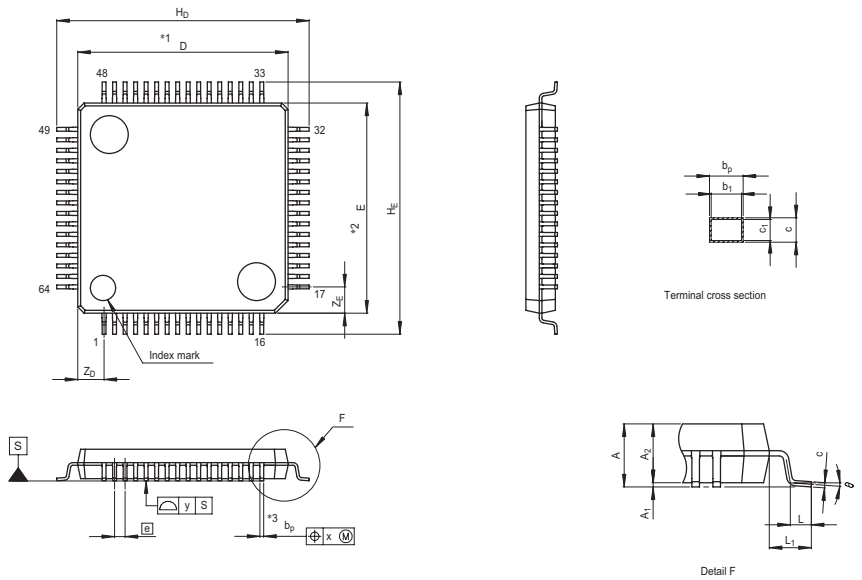
(1) Some of the user flash memory and RAM areas are used by the on-ship debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) Debugging is available under the condition of supply voltage VCC = 1.8 to 5.5 V. Set the supply voltage to 1.8 V or above for rewriting the flash memory.

Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

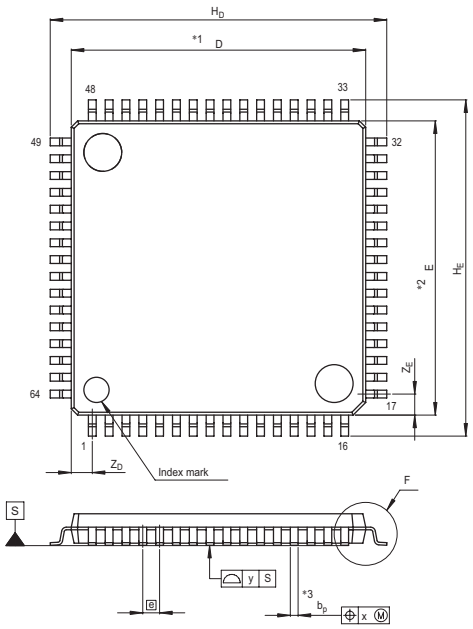
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

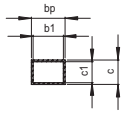


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

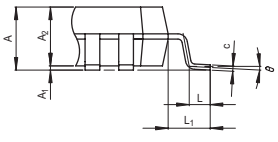
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section

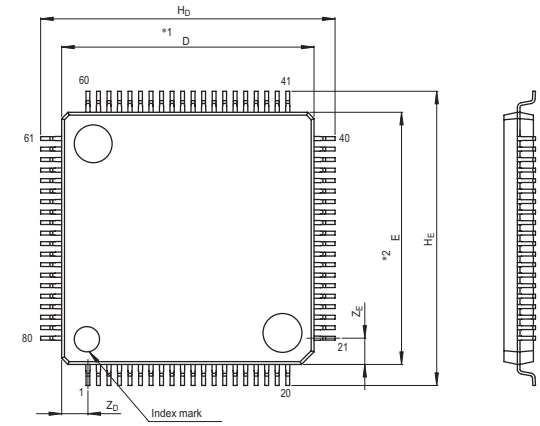


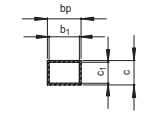
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

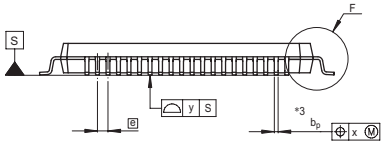
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

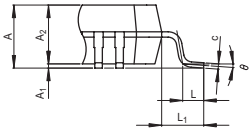
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g





Terminal cross section



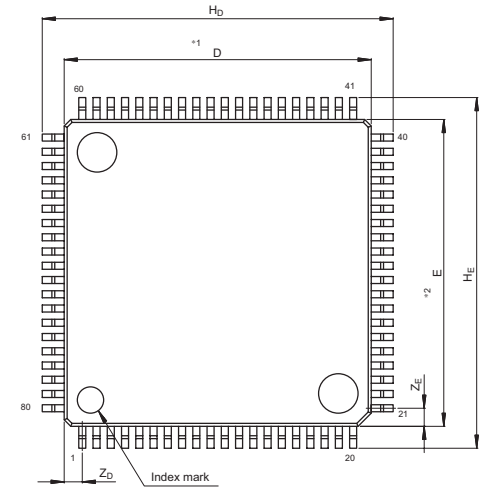


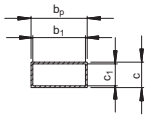
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

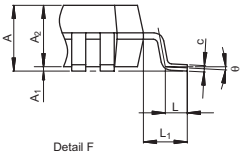
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g

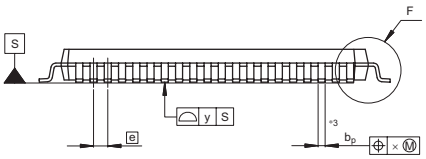




Terminal cross section



Detail F

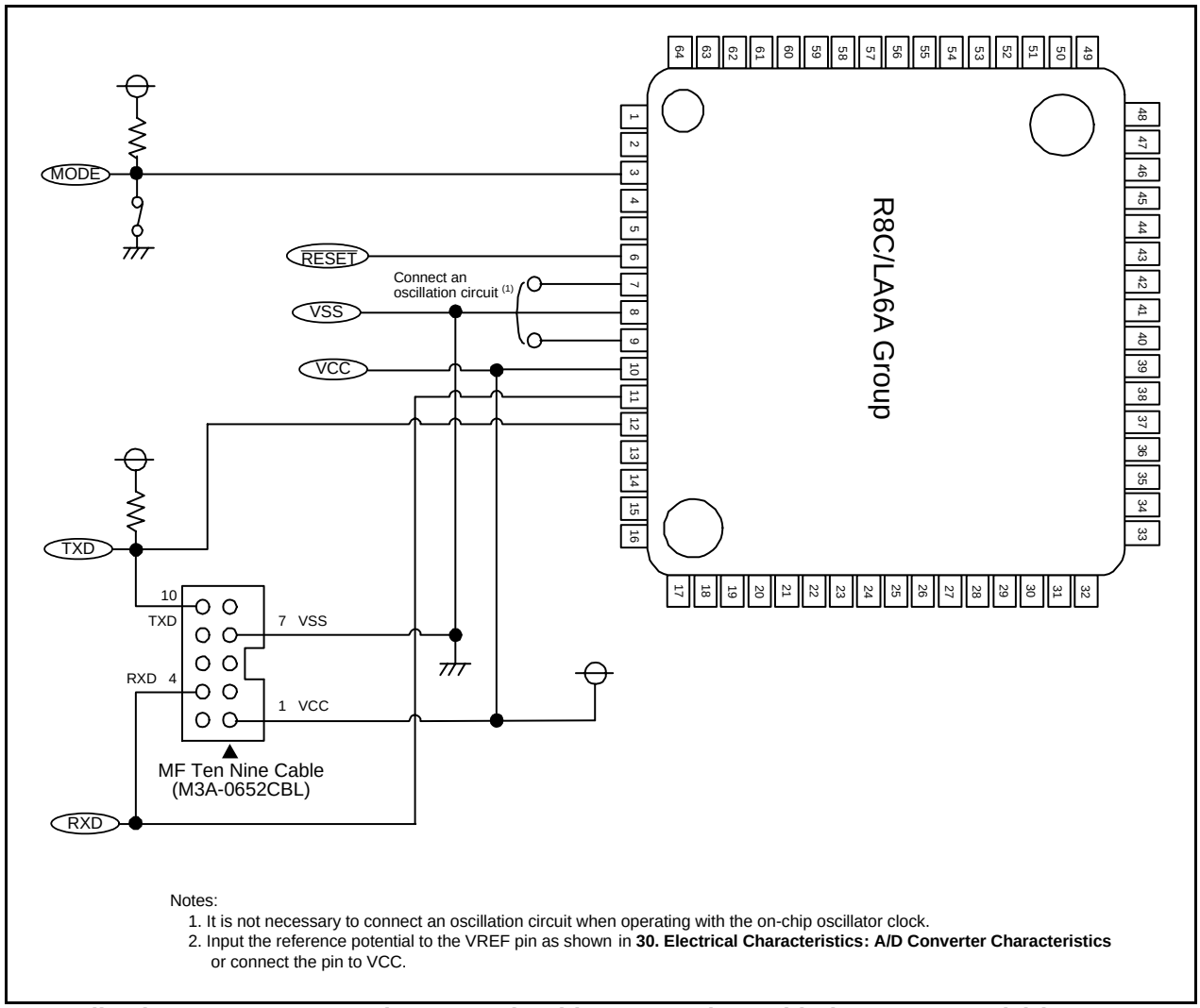


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

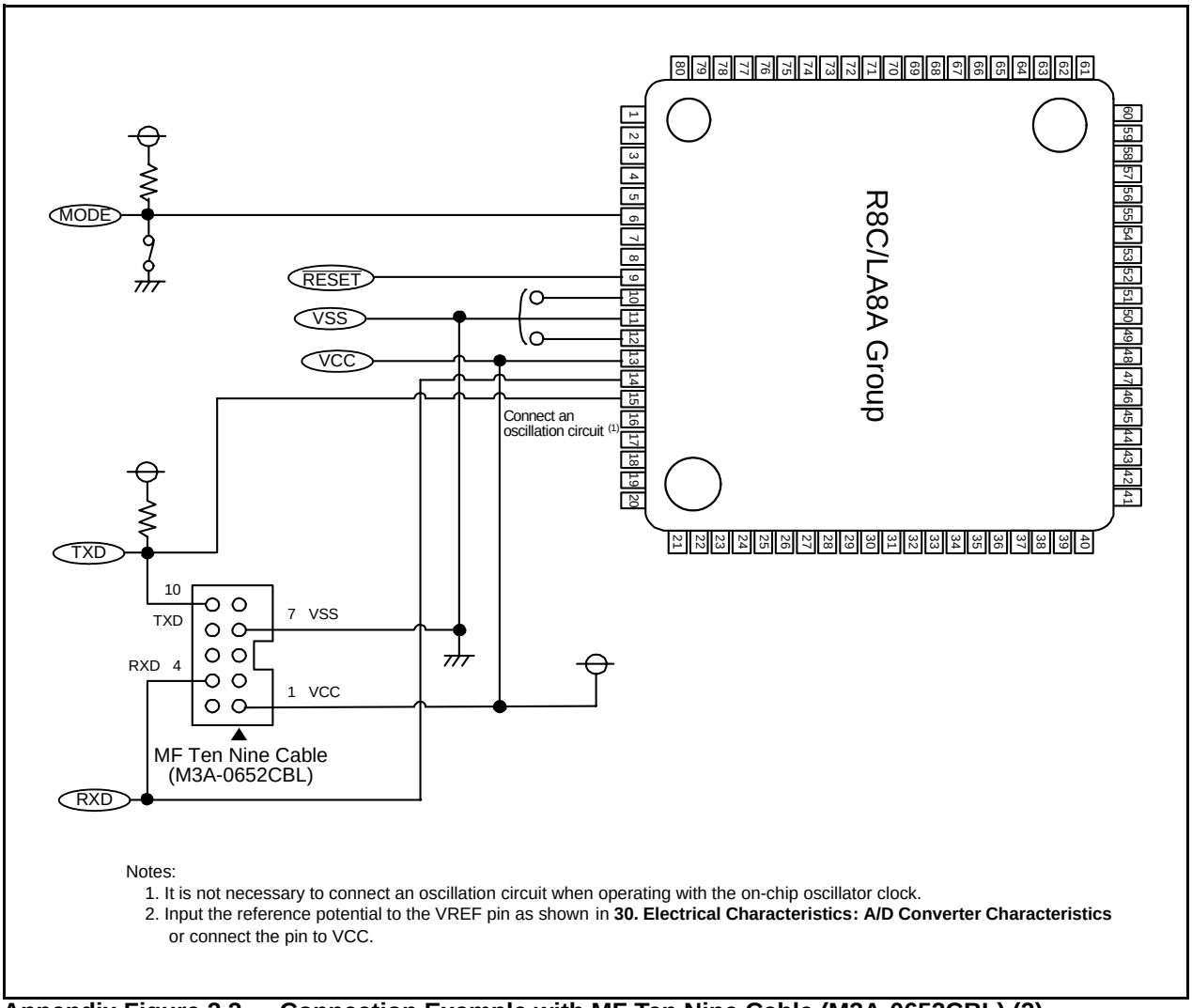
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Appendix 2. Connection Examples with Serial Programmer

Appendix Figures 2.1 to 2.2 show connection examples with the MF Ten Nine Cable (M3A-0652CBL).



Appendix Figure 2.1 Connection Example with MF Ten Nine Cable (M3A-0652CBL) (1)

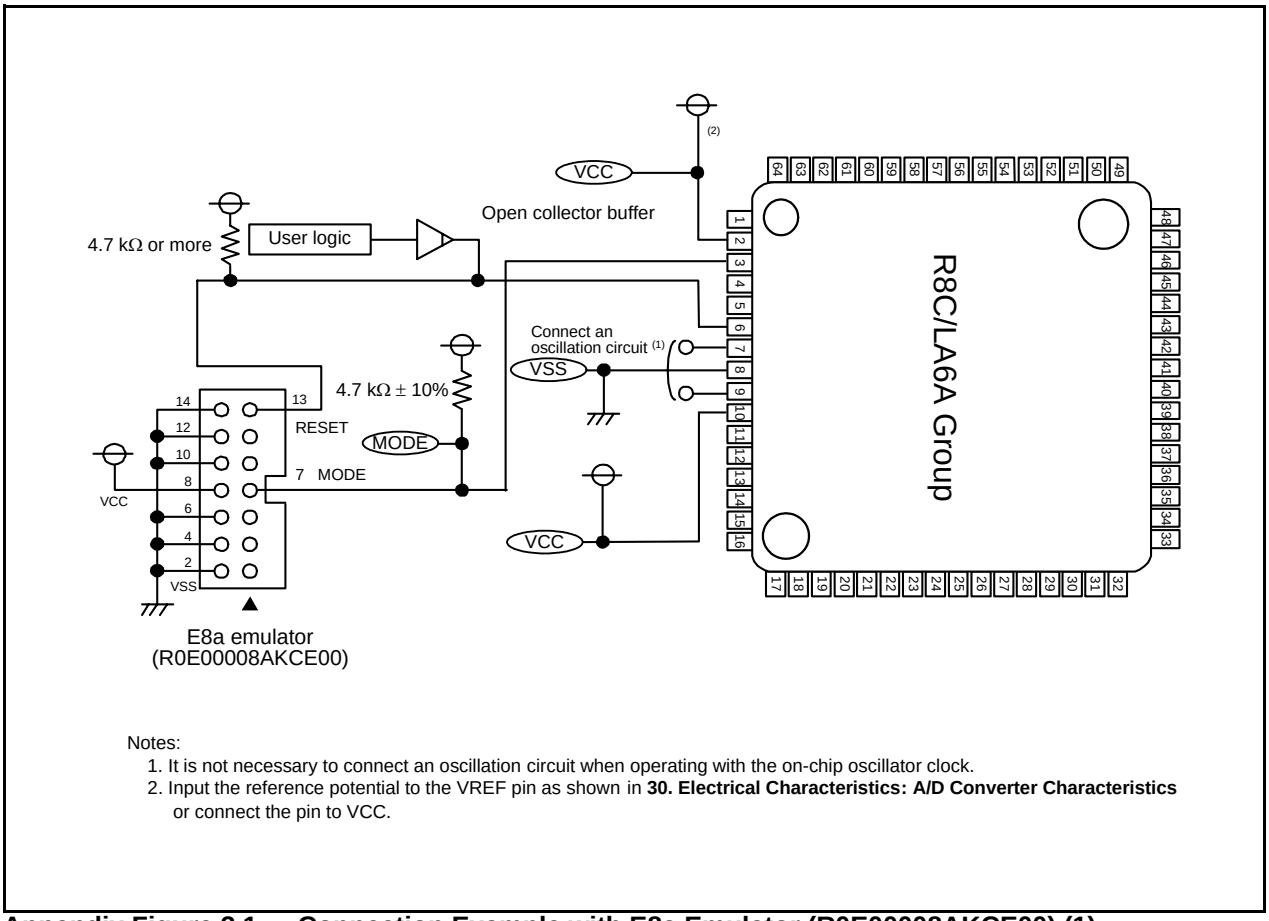


Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **30. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 2.2 Connection Example with MF Ten Nine Cable (M3A-0652CBL) (2)

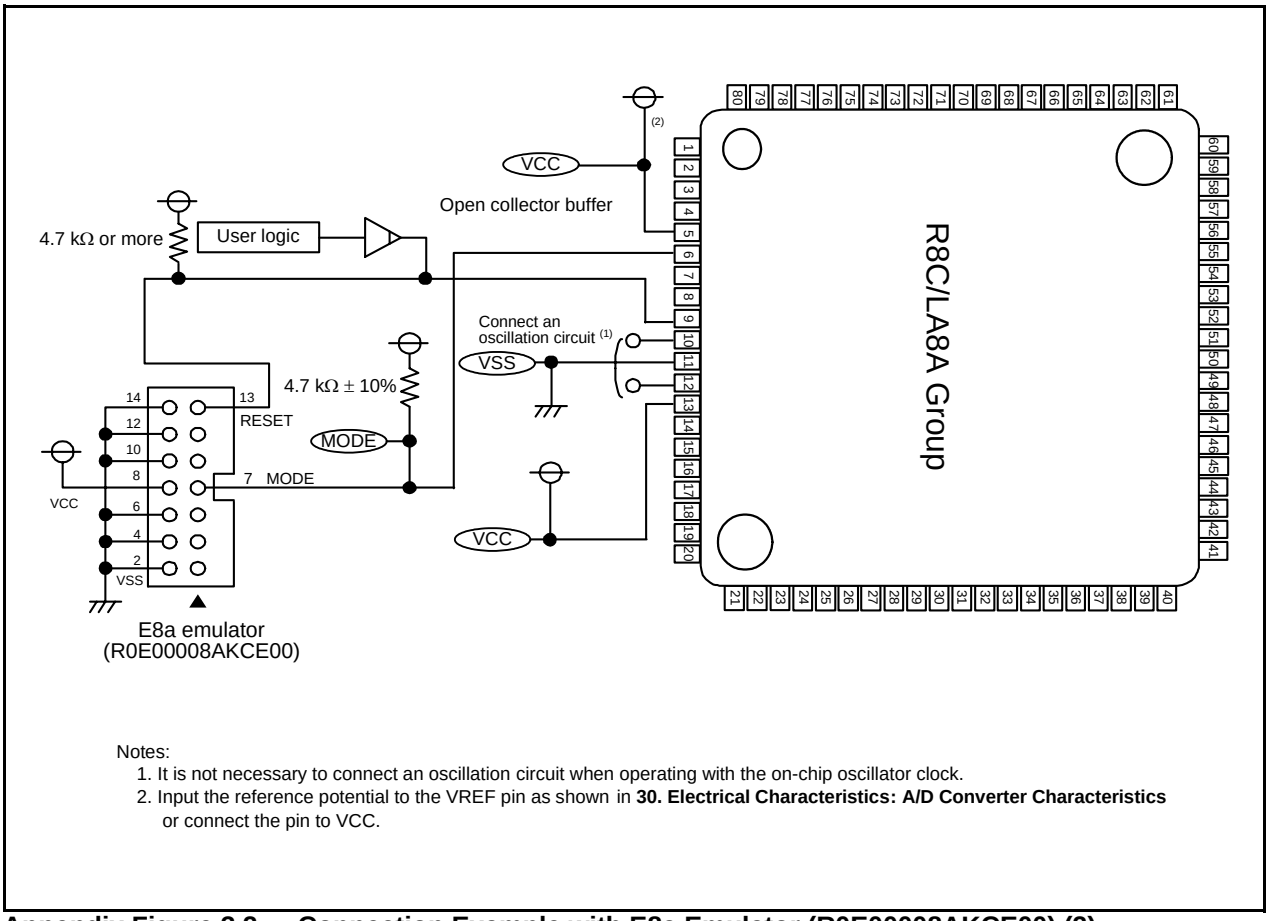
Appendix 3. Connection Examples with E8a Emulator

Appendix Figures 3.1 and 3.2 show connection examples with the E8a Emulator (R0E00008AKCE00).



Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **30. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 3.1 Connection Example with E8a Emulator (R0E00008AKCE00) (1)



Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **30. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 3.2 Connection Example with E8a Emulator (R0E00008AKCE00) (2)

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		Page	Summary
0.10	Sep 18, 2009	—	First Edition issued
0.20	Dec 07, 2009	—	Revised Edition issued
0.30	Jan 15, 2010	all	"low-consumption-current" → "low-current-consumption"
		—	How to Use This Manual revised
		B-1	Address: 0008h, 0029h, and 002Ah revised
		B-4	Address: 018Dh revised
		2	Table 1.1 revised
		3, 63, 520	Tables 1.2 and 7.2 revised, Tables 1.3 and 28.1 revised
		4 to 6	Tables 1.4 to 1.6 revised.
		7	1.2 revised, Table 1.7 revised
		8	Table 1.8 revised
		9	Figure 1.3 revised
		11	Figure 1.5 revised
		12	Figure 1.6 revised
		14	Table 1.10 revised
		17	Table 1.13 revised
		21	3. Memory revised
		22	4. SFRs "The description offered ... on the R8C/LA8A Group." added Table 4.1 Address: 0024h, 0029h, and 002Ah revised
		38	5.2 "Figure 5.2 CPU Register ... Table 4.10 SFR Information" added
		42	5.5 revised
		44	6.1 "As a detection target, ... for voltage detection 2 only." deleted, Table 6.1 revised
		45	Figure 6.1 revised, the last Table 6.2 deleted
		46	Figure 6.3 revised
		47	Figure 6.4 revised
		48	6.2.1 Notes 1 and 2 added
		50, 138	6.2.4 and 10.2.6, After Reset and b4 revised
		52	6.2.6 After Reset revised
		53	6.2.7 Note 2 revised, Note 6 added
		54	6.2.8 b7 and Note 2 revised, Note 6 added
		56	6.3.3 "(1) Set the VCA24 bit ... (LVCMP2 pin input voltage)." deleted
		60	Table 6.3 and Notes revised
		61	Figure 6.7 revised
		65 to 67	Figures 7.1 to 7.3 revised
		80	The last 7.5.11 "Timer RH Second Interrupt Control Register (TRHICR) in Real-Time Clock" deleted
		82, 454	7.5.12 and 25.2.3 b3 revised
		82	7.5.13 Notes 2 and 4 revised.
		87 to 109	Tables 7.5 to 7.76, the order of Pin, Register, and Bit revised
		87	Tables 7.5 and 7.6 revised
		88	Table 7.7 revised
		89	Table 7.12 revised
		92	Tables 7.29 and 7.30 revised

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		Page	Summary
0.30	Jan 15, 2010	93	Tables 7.31 to 7.35 revised
		94	Table 7.36 revised
		97	Tables 7.52 and 7.53 revised
		98	Tables 7.54 and 7.55 revised
		99	Table 7.56 revised
		100	Table 7.57 revised
		101	Table 7.58 revised
		102	Tables 7.59 to 7.61 revised
		103	Tables 7.62 and 7.63 revised
		104	Tables 7.65 and 7.66 revised
		105	Tables 7.68 and 7.69 revised
		106	Tables 7.70 and 7.71 revised
		107	Tables 7.72 and 7.73 revised
		108	Table 7.74 revised
		116, 133	9.2.1 and 10.2.1 Note 5 "To use the VL1 ... above setting." deleted
		117, 134	9.2.2 and 10.2.2 Note 7 added
		118, 135	9.2.3 and 10.2.3 Note 5 deleted
		120	9.2.6 After Reset revised
		123	9.3 "When switching ... (XIN clock stops)." added
		125	9.5 "To use the VL1... above setting." deleted
		130, 602	9.8.3 and 31.1.3 "To use the VL1... above setting." deleted
		141	10.3.2 and 10.3.4 revised
		142	10.4.2 revised
		146	10.5.1 revised
		153	10.7.11 revised, Figure 10.9 Notes 1 and 2 revised
		154 to 155, 603 to 604	10.8.1 to 10.8.3 revised, 10.8.4 added, 31.2.1 to 32.2.3 revised, 31.2.4 added
		156	11.1.1 b2 revised
		174, 515	12.4.3 and 27.2.2 Note 2 revised
		175	12.4.4 b6 and Note 2 revised
		187, 606	Figures 12.12 and 31.1 Note 3 revised
		200	15.2.5 After Reset revised, Note 1 deleted
		209	17.1 "Timer RB has ... with an 8-bit prescaler." added
		211, 284, 329	17.2.1, 19.2.1, and 20.2.1 revised
		213	17.2.5 Note 3 added
		229, 609	17.7 and 31.6 "• To use the underflow ... measurement mode." added
		234, 351, 374, 421, 453, 489, 523	18.2.1, 21.2.1, 22.2.1, 24.2.1, 25.2.1, 26.2.1, and 28.2.1 revised
		280, 612	18.9.5 and 31.7.5 revised
		282	Figure 19.1 revised
		287 to 290	19.2.4 to 19.2.7 After Reset by RTCRST Bit in TRHCR Register revised

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		Page	Summary
0.30	Jan 15, 2010	295	19.2.10 b4 to b6 revised
		297	19.2.12 After Reset by RTCRST Bit in TRHCR Register revised
		298	19.2.13 revised
		301 to 303	19.2.16 to 19.2.18 After Reset by RTCRST Bit in TRHCR Register revised
		304	INTF Bit revised
		305	Figure 19.3 revised
		306	Figure 19.4 revised
		307	Figure 19.5 revised
		308	19.2.20 revised
		309	Figure 19.7 revised
		315	19.2.22.3 revised, 19.2.23 "When bits OS2 to OS0 ... is output." deleted
		316	Figure 19.7 Note 2 added, Table 19.5 revised
		317	19.3.2 "Do not write ... in the TRHCR register is set to 1." added
		319	19.3.4 Note added
		320	Table 19.6 added
		321	19.3.5 After Reset by RTCRST Bit in TRHCR Register revised
		322	19.3.7 After Reset by RTCRST Bit in TRHCR Register revised
		323	Figure 19.17 revised
		324	Figure 19.18 revised
		327	20.1 "Timer RJ has three timers ... 16-bit timers (timer RJ0, timer RJ1, and timer RJ2)." added, Figure 20.1 Note 3 added
		331	20.2.4 Note 1 revised
		341	20.5.1 Notes 1 and 4 added
		347	Figure 20.4 revised
		350	Figure 21.2 revised
		351	21.2.1 MSTCR added
		355	21.2.7 Note 1 revised, Note2 added
		364	Table 21.5 Note 2 added
		372	Figure 22.1 revised
		374	22.2.1 MSTCR added
		379	22.2.7 b9 to b10 revised, Note 1 revised
		392	Table 22.5 Note 2 revised
		394	Table 22.7 revised
		395	Figure 22.7 revised
		402	Table 22.10 revised
		417, 616	The last 22.7.2 and 31.11.2 deleted
		423	24.2.3 Note revised, "To set the SSBR ... (transmission disabled)." added
		424	24.2.6 Note 1 revised
		489	26.2.1 MSTCR added
		503	Table 26.4 Note 1 revised
		504	Table 26.5 Note 1 revised
		512, 617	26.10 and 31.14 revised

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		Page	Summary
0.30	Jan 15, 2010	521	Table 28.2 revised
		523	28.2.1 MSTCR added
		530	Table 28.3 revised
		531	Table 28.4 revised
		539	28.5.3 and Figure 28.13 title revised
		546	Table 29.3 revised
		551	29.4.3 FMR13 Bit revised
		552 to 553	29.4.4 Note 3, FMR27 Bit, 29.4.5, and 29.4.6 revised
		554	Table 29.4 revised, Note 4 deleted
		555	Figures 29.3 and 29.4 revised
		556	Figure 29.6 Note 2 deleted
		564	Figure 29.12 Note 1 revised
		565	Figure 29.13 Note 1 revised
		568	Figure 29.16 revised
		572	Figure 29.18 revised
		577, 620	Tables 29.10 and 31.2 revised
		578, 621	29.7.1.6 and 31.16.1.6 "Do not enter stop ... FMR27 bit is 1 (low-current-consumption read mode enabled)." added 29.7.1.9 and 31.16.1.9 revised
		579	Table 30.1 revised, Note 2 added
		580	Table 30.2 revised
		582	Tables 30.3 and 30.4 revised
		583	Table 30.5 revised
		584	Table 30.6 revised
		585	Tables 30.7 and 30.8 revised
		586	Tables 30.9 and 30.10 revised
		587	Tables 30.11 to 30.13 revised
		588	Tables 30.14 and 30.15 revised
		589	Table 30.16 revised
		590	Table 30.17 revised
		591	Table 30.18 revised
		592	Table 30.19 revised
		593	Table 30.20 revised
		594	Table 30.21 revised
		600	Table 30.24 title and Figure 30.8 revised
		628	Appendix 2 title revised
0.40	Apr 23, 2010	B-3	011Ch to 011Eh revised
		B-4	195h, 197h revised
		B-5	"0FFDBh" → "FFDBh", "0FFFFh" → "FFFFh"
		2	Table 1.1 revised
		3, 521	Tables 1.3 and 28.1 Note 1 revised, Note 2 added
		7	Table 1.7 revised
		8	Table 1.8 revised

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		Page	Summary
0.40	Apr 23, 2010	9	Figure 1.3 revised
		11	Figure 1.5 Note 2 revised
		12	Figure 1.6 Note 2 revised
		17	Table 1.13 "Common output" and "LCD power supply" revised
		26	Table 4.5 011Ch to 011Eh revised
		58	Table 6.2 Note 3 revised
		60	Table 6.3 Note 3 revised
		73, 334	7.5.3 and 20.2.7 b4 to b5 revised
		75, 243	7.5.5 and 18.2.14 revised
		76, 244	7.5.6 and 18.2.15 Notes 1 and 2 deleted
		82	7.5.13 Note 4 revised
		87	Table 7.6 revised
		88	Table 7.7 revised
		95	Table 7.44 revised
		100	Table 7.57 revised
		101	Table 7.58 revised
		113	Table 9.1 Note 2 revised
		117, 134	9.2.2 and 10.2.2 Note 5 revised
		120, 137	9.2.5 and 10.2.5 Note 3 added
		139	10.2.7 Note 2 deleted
		141	10.3.4 revised
		143	Table 10.3 revised
		148	10.6.2 and 10.6.3 revised
		156	11 revised
		160	Table 12.1 revised
		207	Table 16.1 revised
		209	Figure 17.1 revised
		211, 285, 330	17.2.1, 19.2.1, and 20.2.1 revised
		232	Table 18.2 revised
		234, 352, 375, 422, 454, 490, 524	18.2.1, 21.2.1, 22.2.1, 24.2.1, 25.2.1, 26.2.1, and 28.2.1 revised
		284	Table 19.2 revised
		296	19.2.10 b7 revised
		309	19.2.20 revised
		328	Figure 20.1 Note 3 revised
		333	20.2.6 revised
		342	20.5.1 Note 4 revised
		348	Figure 20.4 revised
		351	Figure 21.2 revised
		365	Table 21.5 Note 1 revised
		370	Table 21.8 Note 1 revised

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		Page	Summary
0.40	Apr 23, 2010	393	Table 22.5 Note 1 revised
		522	Table 28.2 "LCD drive timing" and "Interrupt according to the LCD display period" revised
		523	Figure 28.1 revised
		525	28.2.3 revised
		526	28.2.5 b5 revised
		529	28.2.10 b7 revised, Note 1 added, 28.2.11 b0 to b3 revised, Note 1 added
		532	Table 28.4 revised
		535 to 539	Figures 28.4 to 28.12 revised
		539	Figure 28.12 revised
		540	Figure 28.13 Note 1 added
		541, 618	28.6.1 and 31.15.1 revised
		548	29.4.4 Notes 1 and 2 revised
		551, 552	CMDRST Bit, BSYAEIE Bit, RDYSTIE Bit revised
		578, 621	Tables 29.10 and 31.2 revised
		579, 622	29.7.1.6 and 31.16.1.6 revised
		580	Table 30.1 revised
		585	Table 30.6 revised
		586	Tables 30.7 and 30.8 revised
		587	Table 30.9 revised
		590	Table 30.16 revised
		591	Table 30.17 revised
		592	Table 30.18 revised
		593	Table 30.19 revised
		594	Table 30.20 revised
		595	Table 30.21 revised
		623	31.17.1 revised
		625 to 628	Package Dimensions revised
		629	Appendix.2 and Appendix Figure 2.1 revised
		630	Appendix Figure 2.2 revised
1.00	Jun 30, 2010	—	TN-R8C-A011A/E reflected
		—	TN-R8C-A014A/E reflected
		—	TN-R8C-A015A/E reflected
		—	"Module Standby Control Register" → "Module Standby Control Register 0" "MSTCR" → "MSTCR0"
		All	"Preliminary" and "Under development" deleted
		2	Table 1.1 revised
		4	Table 1.4 revised
		5	Table 1.5 revised
		6	Table 1.6 revised
		7	Table 1.7 revised
		8	Table 1.8 revised
		12	Figure 1.6 revised

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		Page	Summary
1.00	Jun 30, 2010	16	Table 1.12 revised
		22	Table 4.1 0020h "After reset" and Note 3 revised
		32	Figure 5.1 revised
		35	5.1.2 Notes 1 and 4 revised
		43	5.7 and 5.8 revised
		50, 138	6.2.4, 10.2.6 Note 2 revised
		70	Figure 7.6 revised
		71	7.5.1 "To use peripheral function ... 1 (output mode)." added
		104	Table 7.67 revised
		105	Tables 7.68 and 7.69 revised
		106	Table 7.70 revised
		110	Table 7.77 Note 3, Figure 7.7 Note 2 revised
		113	Table 9.1 Note 1 revised, Note 2 deleted
		116, 133	9.2.1, 10.2.1 b0 and Note 2 revised, Notes 6 and 7 added
		117, 134	9.2.2, 10.2.2 b0, Notes 2 and 5 revised, Note 8 added
		118, 135	9.2.3, 10.2.3 b2 to b4, b6 to b7, and Notes 2 to 4 revised
		123	Figure 9.3 revised
		125	Figure 9.4 revised
		130, 610	9.8.2 and 31.1.2 revised
		131	10.1, Table 10.1 revised
		132	Figure 10.1 revised
		139	10.2.7 revised, Table 10.2 added
		144	Figure 10.2 revised
		145	Figure 10.3 revised
		146	10.5.1 revised
		147	Figure 10.4 revised
		148	10.6, 10.6.1 to 10.6.3, Figure 10.5 revised
		149	10.6.4, Tables 10.6 to 10.7, Figure 10.6 revised
		150	10.7, Table 10.8, 10.7.1 to 10.7.2 added
		151	10.7.3, Figure 10.7 added
		152	10.8.2 revised
		153	Figure 10.8 revised
		154	10.8.10, Figure 10.9 revised
		155	10.8.11, Figure 10.10 revised
		156, 611	10.9.1 and 31.2.1 revised
		157, 612	10.9.3 to 10.9.4 and 31.2.3 to 31.2.4 revised
		186	Table 12.10 revised
		215	17.2.5 Note 3 revised
		227	17.5.3 revised
		231, 617	17.7, 31.6 revised
		236, 354, 377, 424, 456, 492, 528	18.2.1, 21.2.1, 22.2.1, 24.2.1, 25.2.1, 26.2.1, 28.2.1 Note 6 revised

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		Page	Summary
1.00	Jun 30, 2010	244	18.2.12 b7 revised
		251	18.3.4 revised
		286	Table 19.2 revised
		298	19.2.10 Notes 1 to 3 added
		300	19.2.12 b3 revised
		301	Table 19.4 "• The IR bit ... to 1 (periodic interrupt requested)." → "• The IR bit ... to 1 (interrupt requested)."
		310	Figure 19.5 revised
		327	Figure 19.18 revised
		330	Figure 20.1 revised
		334	20.2.4 Note 1 revised
		335	20.2.6 b0 to b15 and Note 3 revised
		344	20.5.1 b6 to b7 revised, Note 5 added
		360	Table 21.2 Note 2 revised
		388	Table 22.2 Note 2 revised
		402	22.4.6 "The output level goes high ... of the CLK2 pin." deleted
		459	25.2.6 Note 7 added
		460	25.2.7 Note 5 added
		463	25.2.10 Note 7 added
		472	25.4.3 (6) revised
		489, 625	25.9.1 to 25.9.2, 31.13.1 to 31.13.2 added
		490	26 and Table 26.1 revised, Note 4 added
		491	Figure 26.1 revised
		493	26.2.2 Note 1 revised
		495	26.2.4 Note 2 added
		498	26.2.7 Note 1 revised, the last Note 5 deleted, Notes 5 and 6 added
		499	26.2.8 Note 3 revised, Notes 4 and 5, "Due to the characteristics ... of the gain." added
		500	Figures 26.2 and 26.3 revised
		501	Table 26.3 "+ 1 to 3 fAD cycles" added
		502	26.3.3.2 revised
		503	26.3.3.4 revised
		504	26.3.6 revised
		506	26.4 and Table 26.4 revised
		507	26.5 and Table 26.5 revised
		508	26.6 and Table 26.6 revised
		514	26.9, Table 26.9, Figure 26.10 added
		515	26.9.1, Figure 26.11 added
		517, 626	26.11.1, 31.14.1 added, 26.11.2, 31.14.2 revised
		533	28.2.10 Note 1 revised
		538	28.4.5, Table 28.5, 28.4.6, Table 28.6 revised
		546	Table 29.1, Notes 1 and 3 revised
		564	29.4.10.1 revised

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		Page	Summary
1.00	Jun 30, 2010	566	Figure 29.9 revised
		567	Figure 29.10 revised
		568	"When the FMR22 bit ... in EW1 mode.", Figure 29.11 added
		571	Figure 29.13 Figure title revised
		572	Figure 29.14 Figure title revised
		573	"When the FMR22 bit ... in EW1 mode.", Figure 29.15 added
		584, 628	Tables 29.9 and 31.1 revised
		585, 629	Tables 29.10 and 31.2 revised
		588	Table 30.2 revised
		590	Table 30.3 revised, Table 30.4 added
		591 to 595	Tables 30.6 to 30.14 revised
		596 to 603	Tables 30.16 to 30.23 revised
		608 to 609	Tables 30.25 to 30.28 revised
		631	31.18 added
1.01	Jul 08, 2010	637	Appendix Figure 2.1 revised

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